High-Performance Control in Radio Frequency Power Amplification Systems

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High-Performance Control in Radio Frequency Power Amplification Systems

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Preface

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Contents

Abstract

This thesis presents a broad study of methods for increasing the efficiency of narrow-band radio transmitters. The study is centered around the base station application and TETRA/TEDS networks. The general solution space studied is that of envelope tracking applied to linear class-A/B radio frequency power amplifiers (RFPAs) in conjunction with Cartesian feedback (CFB) used to linearize the overall transmitter system.

On a system level, it is demonstrated how envelope tracking is particularly useful for RF carriers with high peak-to-average power ratios, such as TEDS with 10dB. It is also demonstrated how the envelope tracking technique introduces a number of potential pitfalls to the system, namely in the form of power supply ripple intermodulation (PSIM), reduced RFPA linearity and a higher-impedance supply rail for the RFPA. Design and analysis techniques for these three issues are introduced and demonstrated.

On subcomponent level, solutions for implementing the envelope tracking power supply are proposed and demonstrated. A number of buck-type DC-DC converter topologies are investigated and compared, with the objective of showing the trade-offs involved between switching frequency, control bandwidth and ripple voltage. It is found that the simple fourth-order filter buck converter is ideal for TETRA and TEDS envelope tracking power supplies.

The problem of extracting maximum control bandwidth from a given power topology is given particular attention, with a range of, arguably new, insights resulting. It is clearly shown that single-phase switch-mode control systems based on oscillation (controlled unstable operation) of the whole power train provide the highest possible control bandwidth.

A study of the limitations of Cartesian feedback is also included. It is shown that bandwidths in excess of 4MHz can be achieved for a 400MHz carrier frequency using readily available discrete components. Even higher CFB bandwidths are the key to flexible RFPA system capable of transmitting multiple RF carriers simultaneously. A number of key problem areas are identified and shown to need further research.

Practically demonstrated is a high-efficiency 25W TEDS transmitter capable of meeting all base station adjacent channel power ratio and wideband noise specifications with ample margins. Efficiency is improved from 23% to 44% by application of envelope tracking - almost a doubling - at the cost of a single-phase buck converter and without any penalties in RFPA output spectrum purity.

Remsumé (in Danish)

Nærværende afhandling præsenterer et bredt studie af metoder til effektivitetsforørgelse i smalbånds-radio-sendere. Den centrale anvendelse er basestationer til TETRA/TEDS-netværk. I hovedsag studeres løsningsrummet bestående af en lineær klasse-A/B RF-effektforstærker udstyret med en "envelope tracking" spændingsforsyning og linearisering ved hjælp af "Cartesian feedback"-teknikken.

På systemniveau demonstreres "envelope tracking"-teknikken at være særdeles effektiv i forbindelse med RF-signaler med høj spids/middel-effekt, såsom TEDS med 10dB. Det demonstreres også, hvorledes teknikken kan introducere en række potentielle problemer i form af forsyningsintermodulation (PSIM) og reduceret linearitet i RF-effektforstærkeren. Endvidere understreges indvirkningen af "envelope tracking" spændingsforsyningens udgangsimpedans. Til trods for en høj reguleringsbåndbredde kan denne ikke samtidig kan have en meget lav udgangsimpedans.

På blokniveau foreslås og demonstreres løsninger til implementering af "envelope tracking" spændingsforsyninger med fokus på buck-topologier. En række af disse undersøges og sammenlignes med henblik på at illustrere de afvejelser, der skal foretages imellem båndbredde, skiftefrekvens og ripple-spænding. Det vises, at den simple en-fasede buck-topologi med fjerde-orders udgangsfilter er ideel til TETRA -og TEDS -anvendelser.

Det overordnede problem bestående i at opnå maksimal reguleringsbåndbredde, givet en bestemt konvertertopologi, behandles dybdegående. En mængde sandsynligvis ny viden på området præsenteres. Det vises, at selvsvingende reguleringsteknikker udgør vejen til den højest mulige reguleringsbåndbredde.

Også inkluderet er et studium af de begrænsende faktorer i effektiviteten af "Cartesian feedback" (CFB.) Det vises, at reguleringsbåndbredder på over 4MHz kan opnå ved 400MHz bærebølgefrekvens ved brug af let-tilgængelige diskrete komponenter. Højere CFB-båndbredde er nøglen til et fleksiblt RF-effektforstærkersystem, der kan transmittere flere bærebølger samtidig. En række kritiske områder i reguleringssystemet identificeres.

I praksis demonsteres en høj-effektiv 25W TEDS radiosender, som møder alle nabokanaleffekt (ACPR) -og bredbåndsstøjs (WBN) -specifikationer. Effektforstærkerens virkningsgrad forøges fra 23% til 44% - næsten en fordobling - til den beskedne pris af en en-faset buck-konverter og vel at mærke uden væsentlig forringelse af renheden af det afsendte RF-signal.

1 Introduction

In a world that employs wireless (radio based) communication in an increasing number of applications, the utilization of electrical energy in such systems is becoming an issue of economical importance. Many wireless communication systems (including the widespread GSM[1] and IS-95[2] cellular telephony networks) are constructed from a relatively small number of central, stationary nodes (the base stations) that communicate and coordinate data traffic from a large number of smaller, often mobile nodes (the subscribers.) In a GSM network, base stations are well hidden pieces of equipment connected to antennas as seen on the roofs of many high-rise building today while the subscribers are the familiar mobile telephones that we all use. An illustrative example is given in figure 1.

Electrical power consumption of the wireless communication electronics directly affects the battery lifetime or battery bulk of a subscriber. In a base station, power usage is a factor in the operating cost of the equipment. Additionally power losses in electronics circuitry add to the problem of maintaining the internal temperature of the equipment at acceptable levels. All in all, it is therefore desirable for any wireless communication electronics to use as little electrical energy as possible to perform its intended function. In most wireless communication devices (be it base stations or subscribers), the dominant source of power consumption is the transmitter power amplifier, which performs the critical function of driving the antenna with enough signal to allow reliable reception at the desired range. Historically, power amplifiers in wireless ("radio") equipment use somewhat exotic electronics due to the high signal frequency and are therefore known as "radio frequency power amplifiers", abbreviated RFPAs. For a mobile telephone, a typical antenna drive power level could be 200mW, whereas a base station could be driving 100W to its antenna since it has to communicate with many subscribers simultaneously. In modern wireless communication systems (including GSM and CDMA) that utilize digital modulation schemes for converting data into a transmittable radio signal, it is technically very difficult to design an RFPA that both consumes relatively little electrical power and is able to output a radio signal of acceptable fidelity. Signal fidelity is important since the information contained in the transmitted signal must be preserved. Additionally, distortion of the transmitted signal generally leads to the generation of unwanted signal components that may interfere with and disrupt other radio services.

Radio frequency power amplifiers with both high efficiency (to minimize power consumption and waste) and high linearity (to minimize distortion of the radio signal) is therefore a topic that currently attracts a lot of research. It is generally accepted that this area presents a number of technically very challenging issues, as well as a high number of possible but not well explored solutions.

In addition to the GSM and CDMA many other types of network exist. TETRA[3] networks are designed for professional use, e.g. by fire, police and other emergency services. Operating at different frequency bands from GSM and CDMA, TETRA networks are specifically designed to provide a higher degree of connection security and reliability. For Motorola in Copenhagen, the industrial

[1] Global System for Mobile communications, used all over Europe
[2] Interim Standard 95, a.k.a. "cdmaOne" or just "CDMA", used mainly in North America
[3] Terrestrial Trunked Radio

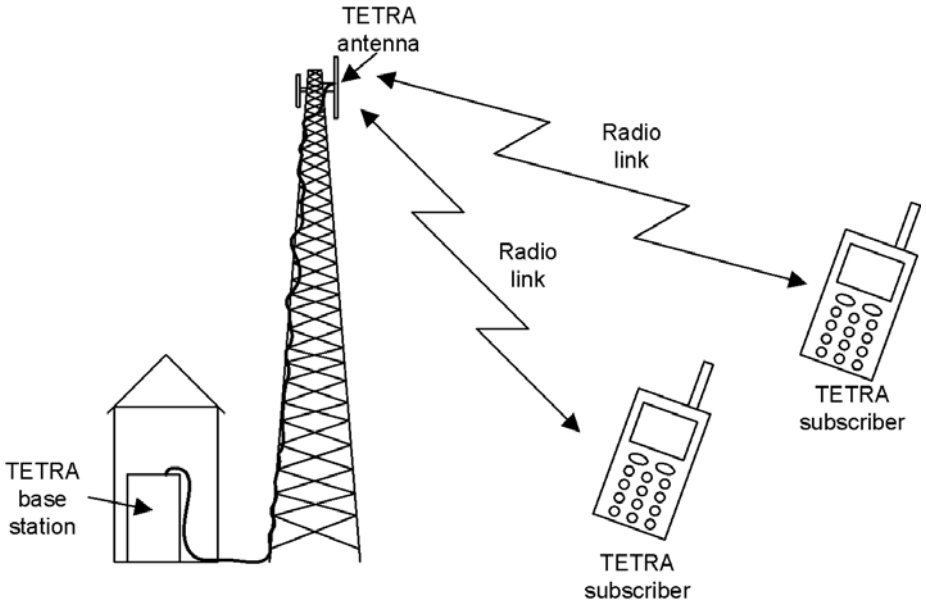


Figure 1: Base station and subscribers in a typical wireless communication system. Base station handles many subscribers and thus has to transmit much more power than a subscriber. Base station is always active since new subscribers may pop up at any time. Example applies for both TETRA as well as GSM and IS-95 cellular telephony networks.

sponsor of this project, business is centered around development and sale of base stations for TETRA networks. As such, this thesis is also centered around TETRA base stations and in particular the reduction of power consumption in these.

It was the combination of business opportunity (arising from potential reductions in base station power consumption) and the technical difficulties in reducing power wastage in the main power consumer, the RFPA, that motivated the start-up of the presented Industrial Ph.D project.

2 The thesis

This section contains a breakdown of the contents of the thesis as well as previously published material. Also found here is a chart linking technical topics to publications and guides for different reader groups on how to approach the presented material.

2.1 Thesis contents

This thesis is divided into a number of sections, each focusing on a particular aspect of the overall problem of reducing power consumption of the base station RF power amplifier. In order to reduce the report writing workload, the report is heavily based on material published in peer-reviewed technical papers as part of the project. These papers are therefore frequently referred to, particularly for detailed technical discussions.

- Section 1 is a general introduction to the issue of power consumption in communication equipment.
- Section 2 is this section. Intended as a thesis navigation aid.
- Section 3 gives a technical introduction to the TETRA base station transmitters and the specifications for these. Section illustrates why the TETRA standard extension TEDS leads to a significant increase in RFPA power wastage.
- Section 4 outlines a number of overall RFPA solutions including the one mainly considered in this project; the combination of linear power amplifier with envelope tracking power supply and cartesian feedback linearization.
- Section 5 introduces the technicalities of one of the main items of research interest in this project; the envelope tracking power supply. The section includes an analytical comparison of buck-based envelope tracking power supply topologies.
- Section 6 demonstrates general methods for classification and modeling control systems for buck converters. The section extends beyond published material.
- Section 7 is a detailed technical study of the interfacing of envelope tracking power supplies and the power amplifier. Analysis is supported with experimental results.
- Section 8 provides a late-hour update on cartesian feedback system performance. The opportunities and limitations in control system bandwidth are explored analytically and experimentally.
- Section 9 concludes this thesis. Scientific contributions are summed up with the base station transmitter application in mind.
- Section 10 presents an outlook on further research possibilities and opportunities by extrapolating from achieved results.

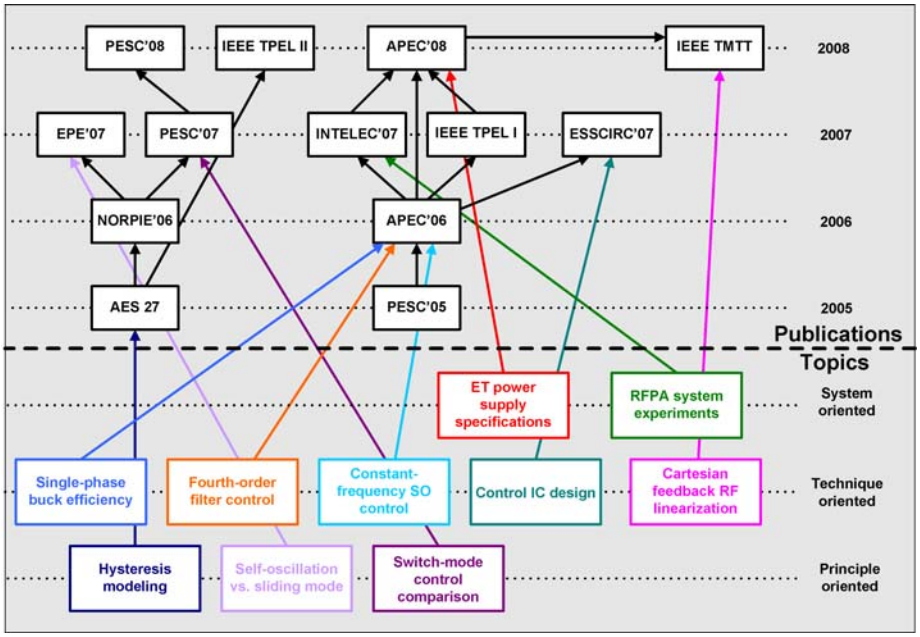


Figure 2: Subtopics and related publications (identified by conference or journal) in the presented work.

2.2 Publications and technical subtopics

The chart in figure 2 provides an overview of the studied technical topics and the related publications made during the Ph.D project as well as two from before the formal project startup (which was January 1, 2006.) The publications are identified by the associated conference or journal and are cross-referenced with citation indexes and titles in table 1.

2.3 Reading suggestions

Assuming that the introduction has just been read, the reader now faces the issue of choosing what to read next. Since the thesis is composed from original text and published material, a logical one-way page-by-page flow does not exist, i.e. reading the thesis sequentially from first to last page makes for a bad and confusing experience. Hence the following reading guides are provided, based on a non-scientific classification of potential readers:

1. Formal reviewer - the reader whose task is to formally evaluate the quality of the presented work. Assumed to be a busy person who does not want to read every sentence and paragraph.

2. Power electronics specialist - seeks the low-level details on power and control circuitry and its performance.

3. Control specialist - has an interest in the application of feedback-based control.

Table 1: Publications considered part of the presented Ph.D study, listed chronologically. Use table to cross-reference with figure 2 and reference numbers used in this thesis. All publications except PESC'08 have M.C.W. Høyerby as first author.

Reference, figure 2	Reference, throughout	Title	Type
PESC'05	[42]	*High Bandwidth, High-Efficiency Envelope Tracking Power Supply for 40W RF Power Amplifier Using Paralleled Bandpass Current Sources*	Conference
AES 27	[55]	*Derivation and Analysis of a Low-cost, High-performance Analogue BPCM Control Scheme for Class-D Audio Power Amplifiers*	Conference
APEC'06	[36]	*Envelope Tracking Power Supply with fully controlled 4th order Output Filter*	Conference
NORPIE'06	[44]	*A small-signal model of the hysteretic comparator in linear-carrier self-oscillating switch-mode controllers*	Conference
IEEE TPEL I	[39]	*Ultrafast Tracking Power Supply with 4th order Output Filter and Fixed-Frequency Hysteretic Control*	Journal
PESC'07	[45]	*A Comparative Study of Analog Voltage-mode Control Methods for Ultra-fast Tracking Power Supplies*	Conference
EPE'07	[47]	*Accurate Sliding- Mode Control System Modeling for Buck Converters*	Conference
ESSCIRC'07	[46]	*A 0.35 μm 50V CMOS Sliding-Mode Control IC for Buck Converters*	Conference
INTELEC'07	[37]	*Self-Oscillating Soft Switching Envelope Tracking Power Supply for Tetra2 Base Station*	Conference
APEC'08	[38]	*Optimized Envelope Tracking Power Supply for Tetra2 Base Station RF Power Amplifier*	Conference
PESC'08	[48]	*A Versatile Discrete-Time Approach for Modeling Switch-Mode Controllers*	Conference
IEEE TPEL II	[52]	*Carrier Distortion in Hysteretic Self-Oscillating Class-D Audio Power Amplifiers: Analysis and Optimization*	Journal
IEEE TMTT	[33]	*High-Efficiency TEDS Base Station Power Amplifier using Low-Noise Envelope Tracking Power Supply*	Journal

4. RF specialist - an RF engineer who wants to know about envelope tracking and power consumption reduction.
5. Class-D audio specialist - has an interest in the side-topic of class-D audio power amplifiers.
6. Envelope tracking specialist - already knows about the application and the problems and just wants to see "what's new".
7. Any other electronics engineer - seeks an introduction to the general technical issues in the application of envelope tracking.
8. Business executive - has an interest in the financial implications of the new technology.

The different reader groups are recommended to approach the material as described in the following, which is of course only a qualified suggestion. Any reader is recommended to read the introduction and conclusion sections.

2.3.1 Formal reviewer

Get an impression of the topics covered from figure 2. For an introduction to the TETRA radio system see section 3. Paper [39] provides an overview of the power electronics side of the TEDS envelope tracking problem. Paper [38] gets closer to system level and [33] makes the full plunge into the RF domain. The overall system level considerations are summed up in section 7. Skim [45] and [46] to see the width of technical issues considered. Go to section 5 for a wider outlook on the power electronics problem. See section 6 for a very general approach to buck converters and their control circuitry. Jump to section 8 for a last-minute study of the opportunities and limitations in the application of cartesian feedback.

2.3.2 Power electronics specialist

Read section 5 for the reasoning behind the focus on fourth-order filtered buck converters for envelope tracking. Read papers [39] and [38] for a demonstration of an effective overall power solution. See paper [37] for a short adventure with soft switching and more complicated control.

2.3.3 Control specialist

Skim paper [39] for an introduction to the power electronics control problem at hand. Try reading [45], [44] and [48] to see why switch-mode controller modeling is an interesting topic. See section 6 for the latest update on this thread. For a sliding mode approach to self-oscillating control see [47]. Look at section 8 to see the return of the identified head villain: delay.

2.3.4 RF specialist

For overall efficiency improvements when using envelope tracking, see paper [33]. For a follow-up on cartesian feedback effectiveness see section 8. The power electronics technology used is documented in [39] and [38]. For a power electronics specialist's outlook on the interfacing of the RFPA and the envelope tracking power supply see section 7 which somewhat overlaps with [33].

2.3.5 Class-D audio specialist

Paper [52] might be of interest. For advanced modeling techniques that should be useful (with additional work) for computing any feedback based switching amplifier's rejection of power supply and dead time induced errors see [48]. The scope of this study is widened in section 6.

2.3.6 Envelope tracking specialist

The not-very-widespread envelope tracking power supply technique that is the fourth-order filtered buck, is presented in [39]. See section 5 for an overview of alternative solutions. For full-system results see [33]. Section 7 provides a take on how to specify the envelope tracking power supply that is conspicuously absent from prior art.

2.3.7 Any other electronics engineer

Section 3 provides a general introduction to the TETRA radio communication system. Section 4 lines up a number of radio frequency power amplification solutions including the one studied. Section 5 similarly shows a range of solutions for the envelope tracking power supply. Paper [39] is a fully detailed dive into a particular envelope tracking power supply solution. The practical effects of applying an envelope tracking power supply to an existing RFPA is demonstrated in [33].

2.3.8 Business executive

Business implications of the technology discussed in this thesis are mainly addressed in the "Motorola Confidential" business report that was written as part of the Industrial PhD project requirements.

For those short of access to this report, the power savings enabled by the use of envelope tracking is illustrated in paper [33]. The cost and complexity of the envelope tracking power supply can be assessed from [39]. A degree of technical knowledge is required for these assessments.

3 TETRA/TEDS Wireless Transmitters

This section provides a short introduction to TETRA and TEDS with focus on the Radio Frequency Power Amplifier (RFPA) in the base station application. Examples of signal waveforms handled by the RFPA are given as well as an outline of the limits imposed by the TETRA standard on unwanted signal emissions.

3.1 TETRA

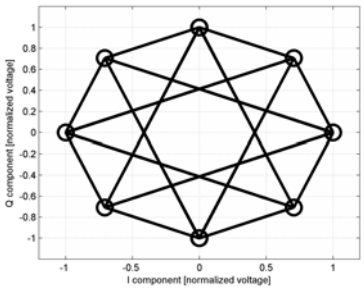
The acronym "TETRA" stands for "TErrestrial Trunked RAdio" or formerly "Trans-European Trunked Radio". The shift between acronym definitions reflects the business success of TETRA; it was originally conceived for European use in 1995 but has since spread to other parts of the world. TETRA is in its basic form intended for operation in UHF frequency bands (25kHz bands in the 400MHz area) generally occupied by Professional/Private Mobile Radio (PMR) systems. There are many types of PMR systems (digital types include iDEN, EDACS and APCO25, analog systems exist as well), with TETRA being one of them. A main business case for TETRA systems is therefore replacement of older PMR equipment with TETRA equipment. Note that the need for operation alongside with other PMR systems leads to quite harsh restrictions on emissions outside the 25kHz transmission bands for PMR systems. Basic TETRA employs Differential Quaternary Phase Shift Keying (DQPSK) with $\pi/4$ phase steps, typically labeled $\pi/4$-DQPSK. Information (data bits) is encoded as phase jumps in the carrier signal, with possible four phase jumps ($\pm\pi/4$ and $\pm 3\pi/4$) so that two bits can be encoded per transmitted symbol. The avoidance of transitions that force the I/Q trajectory through the I/Q plane origin as well as the placement of constellations points on a unit circle lead to a fairly low peak-to-average power ratio on the TETRA carrier of around 3.4dB. As an example, this allows a 200W (peak) RFPA to output a 90W TETRA carrier. The RFPA efficiency can therefore be relatively good (40% area) with standard (class A/B) RFPA techniques.

3.2 TEDS

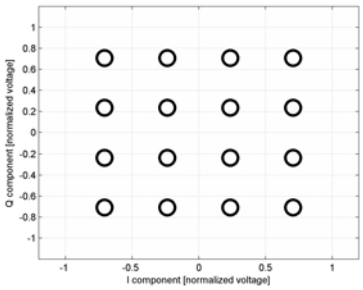
TEDS stands for "TETRA Enhanced Data Service" and covers extensions to the original TETRA standard. On the hardware side, TEDS adds additional modulation forms to the system, namely Quadrature Amplitude Modulation (QAM) based forms and $\pi/8$-D8PSK. Higher overall carrier bandwidths are allowed with TEDS. An example is the 50kHz mode where two adjacent PMR bands are occupied by a single TEDS carrier. Also specified in the standard are 100kHz and 150kHz modes. The TEDS carrier is split into a number of sub-carriers (8 carriers per 25kHz), each of which carries a QAM modulated data stream. The use of QAM and the many sub-carriers generally lead to a much-increased peak-to-average power ratio for TEDS carriers. A typical peak-to-average power ratio of a TEDS carrier is 10dB. This means that a 200W (peak) RFPA is needed to produce 20W of average RF output. As such, the average RFPA efficiency will be significantly lower (20% area) than for a TETRA carrier of the same peak power with standard class-A/B RFPA technology. On a technical level, this observation was the prime motivating factors for the launch

of the presented Ph.D project. As such, the presented work is heavily focused on increasing RFPA efficiency with TEDS carriers. To maximize the chance of success, primary focus was set on the 50kHz bandwidth TEDS application.

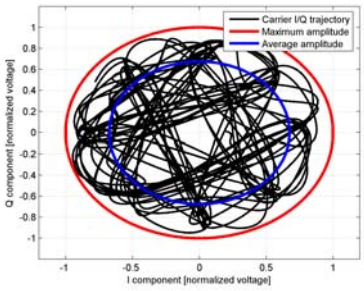
TETRA and TEDS carriers are compared in the I/Q domain and in the time domain in figure 3.



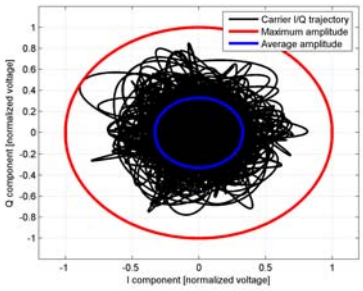
(a) TETRA $\pi/4$-DQPSK constellation points and possible transitions.



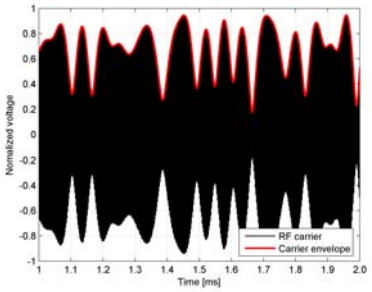
(b) TEDS 16-QAM constellation points (for each sub-carrier.) Any transition is allowed.



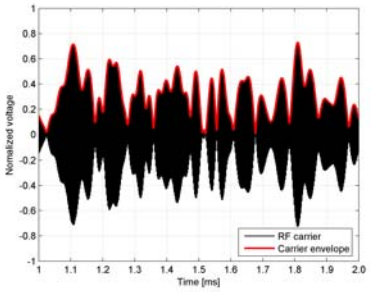
(c) TETRA I/Q trajectory. Peak-to-average ratio is around 3.4dB.



(d) TEDS I/Q trajectory. Peak-to-average ratio is around 9.6dB.



(e) TETRA RF carrier and envelope.



(f) 50kHz TEDS RF carrier and envelope.

Figure 3: TETRA and 50kHz TEDS RF carrier examples. TEDS envelope moves faster and TEDS carrier has much higher peak-to-average power ratio, degrading RFPA efficiency.

3.3 Out-of-band Emission Limits

Of major importance in the design of TETRA and TEDS transmitters is the allowable power outside the transmission band. This is specified in Adjacent Channel Power Ratio (ACPR) and WideBand Noise (WBN) numbers as illstrated in figures 4 and 5. As an example, a TETRA base station transmitting a 40W (+46dBm) carrier is allowed to produce (46dBm-60dB = -14dBm) of unwanted power in the two directly neighboring PMR channels. Power is here defined looking through a TETRA receiver input filter which is an 18kHz wide root-raised cosine (RRC) filter. The same filter is used to shape the transmitted TETRA carrier from the non-differentiable trajectory of figure 3a to the smooth, band-limited trajectory of figure 3c. Note that adjacent channel power is specified at particular (six in all) frequencies whereas WBN is defined for any frequency offset of more than ±100kHz. For TEDS, ACPR and WBN is still measured through the 18kHz RRC and numbers are still relative to the carrier power.

Further specifications exist for ensuring the quality of the TETRA/TEDS base station output. One such is error vector magnitude (EVM) which refers to the ability of the transmitter to reproduce the correct constellation points. Practically, if the baseband modulation is correctly implemented, EVM is likely to be good enough if ACPR is also good enough.

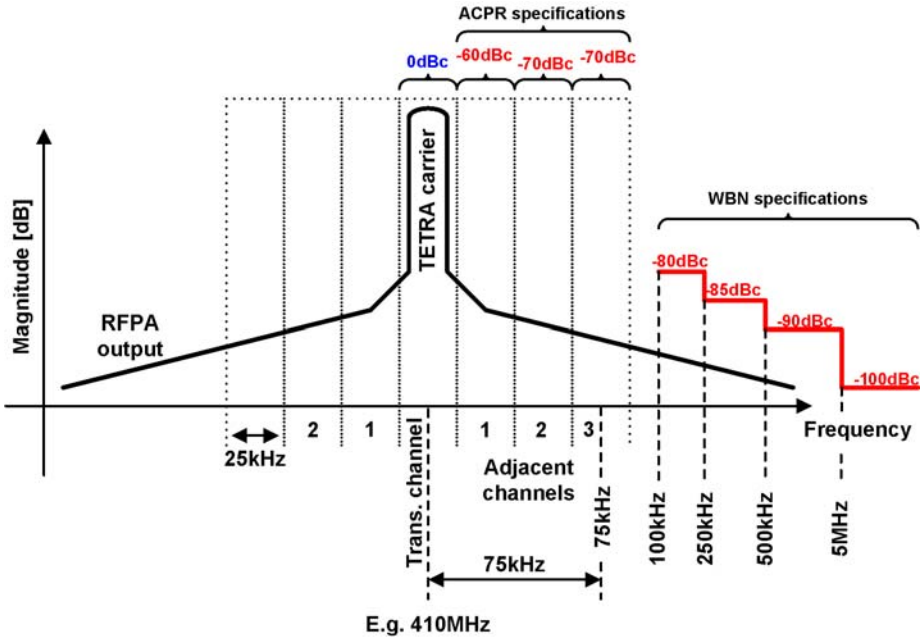


Figure 4: Specifications for adjacent channel power ratio (ACPR) and wideband noise (WBN) for TETRA base stations. All powers are measured through the 18kHz root-raised cosine (RRC) band-pass filter also used to shape the TETRA carrier.

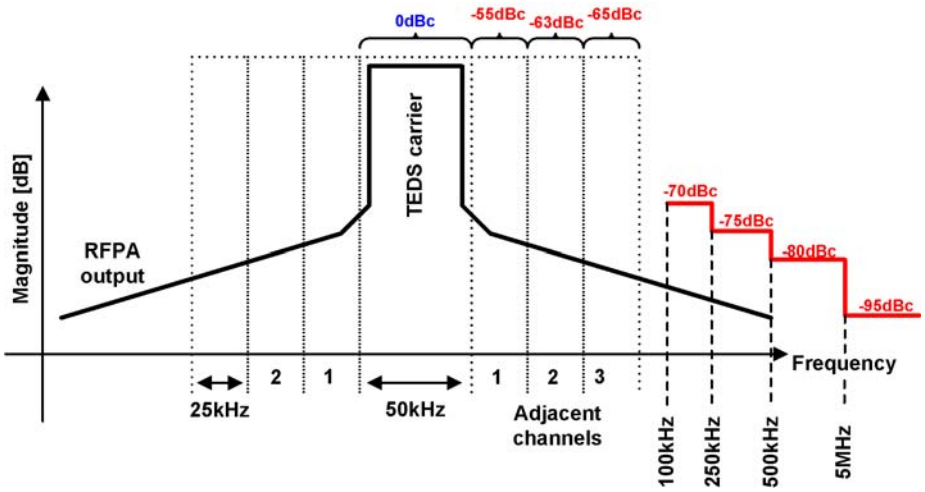


Figure 5: ACPR and WBN specifications for 50kHz QAM TEDS base stations. Total carrier power defines 0dBc, other powers are measured through the 18kHz TETRA RRC.

3.4 Summary

This section has introduced the general characteristics of TETRA and TEDS radio signals. It has been illustrated that the TEDS signals exhibit much higher peak-to-average power ratios (10dB area) than the original TETRA signal (3.5dB area), undermining class-A/B RFPA efficiency. The issue of allowable RFPA non-linearity has been introduced based on the specifications for allowable out-of-band emissions, in the form of Adjacent Channel Power Ratio (ACPR) and WideBand Noise (WBN) limits.

4 Overview of Radio Frequency Power Amplification Systems

This section introduces and reviews a number of complete solutions for implementation of radio frequency power amplifiers (RFPAs.) In its simplest form, an RFPA can be a simple one-transistor common-source/collector amplifier as illustrated in figure 6. The shown amplifier circuit is very similar to any textbook common-source amplifier circuit, with only the input/output matching networks revealing its RF purpose. An input matching networks ensure that the circuit will function in a high-frequency environment where input ports should present a well-defined impedance (typically 50Ω) to driving circuitry connected through electrically long (several wavelengths) transmission lines. The output match is typically designed for an acceptable trade-off between power, efficiency and linearity, with output port input impedance being of less concern.

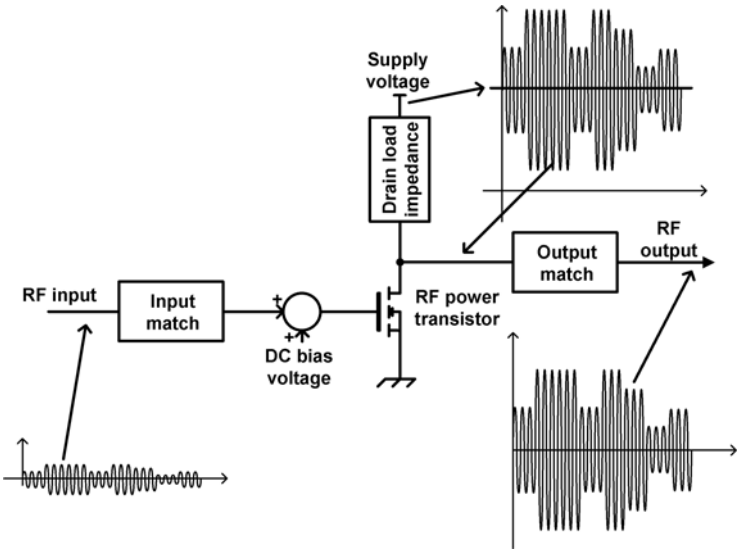


Figure 6: Simple linear common-source RFPA, capable of being biased into class-A/AB/B/C operation.

In most practical applications, especially including TETRA, this type of amplifier alone will be inadequate for power amplification duty due to limited linearity and/or poor efficiency. Therefore, a practical RFPA solution will often be a larger system, where the physical power amplifier is only a building block. For this discussion, systems/solutions for radio frequency power amplification are represented on block diagram form, comprising the following types of elements:

- A basic radio frequency power amplifier, capable of adding significant power to an input signal. This may be a basic RFPA using class-A/AB /B/C/D/E/F operation of the main power device(s) or a compound RFPA solution such as a Doherty design. In any case, the RFPA is either largely linear (e.g. class-A/AB/B) or decidedly non-linear (e.g. class-C/D[4]/E.)

[4]Class-D RF power amplifiers are non-linear; the PWM class-D amplifier used for audio is

- A power supply for the RFPA, capable of delivering either a stiff DC rail or a variable supply to the RFPA.

- A baseband linearization system for correcting inevitable RFPA non-linearities using feedback, error feed-forward/pre-distortion or a combination of the two.

It is important to note here that only *baseband* linearization systems are considered. RF-level linearization methods such as feed-forward or Chireix (outphasing) are considered to be encapsulated in the RFPA block. It is taken as given that it is possible to further apply base-band linearization on these compound amplifiers if desired. The application of various variable-supply schemes is also probably possible although rarely exploited in open literature.

4.1 RFPA and power supply combinations

Starting with the RFPA and power supply, a total of four possible basic combinations exist. One of the basic combinations, that of a linear RFPA and a variable power supply in itself presents a large solution space since system functionality can principally be assured with any choice of power supply bandwidth (BW.) Here, this solution space has compressed into two basic approaches [10]; that of envelope tracking (ET) and that of envelope following (EF.) The combination of a non-linear RFPA and a variable power supply here refers to the envelope elimination and restoration (EER) approach proposed by Kahn in 1952 [4]. It is generally accepted [9], [3] that the requirement on power supply bandwidth is not quite as elastic here as with ET/EF, since it must be on the order of at least twice the RF carrier bandwidth. The EER solution generally provides excellent efficiency since the RFPA is operated in saturation and can be a non-linear and efficient type such as class-D or class-E. A drawback is that zero output is difficult to achieve due to feed-through [5]. The combination of a fixed power supply with a non-linear RFPA mainly refers to the type of solutions typically used for FM broadcast, i.e. a saturated class-C or class-D RFPA amplifying a constant-envelope carrier where the lack of amplitude control is of no consequence. Practically, the supply may still be varied slowly to control output power. A very different class of variations of the non-linear RFPA and fixed supply combination relies on pulsed RFPA operation and sigma-delta modulation for producing output the levels between zero and full power. An excellent example is given in [60] where a class-D RFPA with a fixed supply rail produces a WCDMA-type carrier with good fidelity. Difficulties exist in implementation (pulsed RFPA operation with precise timing) and extra noise (delta-sigma modulators are noisy.) Nonetheless, this is probably a solution space with the future ahead of it.

The combination of linear RFPA and a fixed supply is a currently very widespread solution since this allows amplification of today's digitally modulated carriers without the complications arising from introducing a variable power supply.

The discussion above is summed up in table 2.

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logically very linear and referred to as class-S in RF terminology [2]

Table 2: Simplified overview of RFPA/supply schemes.

RFPA	Supply	A.K.A.	Supply BW	PSRR	Linearity	Efficiency
Linear	Fixed		Very low	Excellent	Excellent	Poor
Linear	Variable	ET	Medium	Fair	Fair	Good
Linear	Variable	EF	Low	Good	Good	Fair
Non-linear	Fixed		Very low	Poor	Poor/Good	Excellent
Non-linear	Variable	EER	High	Poor	Fair	Excellent

4.2 Baseband linearization methods

For the baseband linearization part of the overall RFPA solution, five options are considered.

Digital pre-distortion [17], [16], [15], [14] (DPD) is and has been a subject of intense research judging by the volume and publication time of prior art. This solution has the huge advantage of being capable of operating on very high (multi-MHz) bandwidth RF carriers, as also evident from the frequent choice of the W-CDMA[5] application for DPD papers. Difficulties exist in the form of predicting RFPA behavior and tracking this of variations in temperature, aging, etc. Accuracy of the pre-distortion algorithm and data ultimately limits the achievable linearization with DPD. Feedback based on a Cartesian (real/complex or I/Q) representation of the RF carrier is another commonly adopted linearization scheme. Since most digital modulation schemes operate directly in the I/Q domain and since it is easy to translate between baseband I/Q signals and an RF carrier, it is principally also straightforward to close a control loop around the RFPA in the I/Q domain. As a feedback method, Cartesian feedback (CFB) effectiveness is limited by the nature of the plant, in this case the I/Q modulator and demodulator and the RFPA along with interconnect wiring. More specifically, each introduces a delay from input to output which ultimately limits the achievable control bandwidth [1]. This problem was examined in this project [33] (see also section 8) and it was found that achievable bandwidths lie in the area of 1-10MHz decade for a discretely constructed 400MHz RFPA system. Bandwidths far above 10MHz have been reported for fully integrated implementations [23]. Given enough bandwidth, the ultimate linearity limit with CFB is set by the linearity of the I/Q demodulator since [25] this is the only potential non-linearity in the feedback path of the control system. A significant nuisance with CFB linearization is the requirement for *synchronous demodulation* [25], [34] i.e. to have an exact phase relationship between the RF signal being demodulated and the demodulator LO. Failure to observe this potentially leads to instability, particularly in high-bandwidth designs where phase margin is limited.

Feedback based on the polar representation (amplitude and phase) of the RF signal is a potential solution that is not often adopted in prior art. This can probably be attributed to the typical preference for having the baseband reference signals in Cartesian (I/Q) form, as well as a polar modulator not being a standardized block like an I/Q modulator. Polar feedback (PFB) is still principally very suitable for isolated applications, such as in EER-based RFPA system. Here the variable power supply provides a natural amplitude modulation input while a variable phase shifter or delay can function as the phase

[5]Wideband Code Division Multiple Access

modulation input. Obtaining the amplitude of the RFPA output is possible using simple circuitry. Phase comparators are likewise standard circuitry blocks. Note that hybrid solutions between pre-distortion and CFB/PFB are principally possible [12], [13], [35]. In standard feedback theory nomenclature, it is always an option to try to estimate or measure an error and compensate for it by feed-forward of the estimate to the appropriate point in the control loop. DPD can as such be considered a variant of error feed-forward, where the error is estimated and compensation injected at baseband and no feedback loop is closed. Keeping a DPD-style error lookup table at digital baseband level, it is thus principally possible to estimate and inject the baseband error that the feedback system is going to have to correct for. This can be thought of as a means of reducing the open-loop distortion of the RFPA, hereby also reducing the closed-loop distortion. Hereby it can also be argued that CFB/PFB bandwidth (not in a "crossover frequency" sense of course) is increased since less loop gain is required for a given linearity requirement. One practical implementation relies on the closure of the feedback loop in the digital domain [12], [13], in order to allow the use of a series look-up-table for pre-distortion. Alternatively, as proposed in a Motorola patent application spun off from this project, the CFB loop can be closed in the analog domain with parallel-style error feed-forward [35] (see figure 7) in order to avoid AD/DA conversion delays. Literature focusing on the combination of feedback and feed-forward/DPD is generally quite scarce, probably a reflection of the mainstream requirement for both linearity *and* high bandwidth, e.g. for WCDMA.

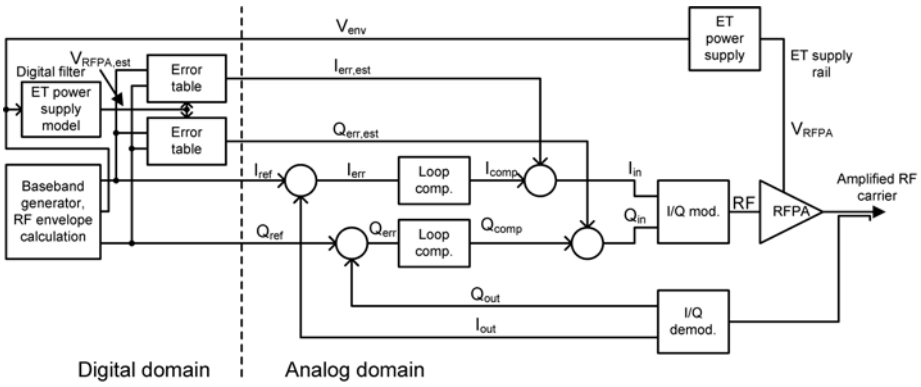


Figure 7: Combination of envelope tracking with CFB and error feed-forward proposed in [35].

Avoiding baseband linearization altogether has finally been shown to be potentially possible, notably in EER systems where the RF carrier has a variable but always non-zero envelope like in EDGE [5], [30]. An interesting option for TETRA due to the non-zero envelope property of the $\pi/4$ DQPSK modulation, the solution is not suitable for TEDS carriers which may have zero envelope. As such, it is not considered an option to avoid a baseband linearization system in a power-efficient TEDS power amplifier.

Table 3: Simplified overview of baseband-referred RFPA linearization schemes.

Method	Improvement	Bandwidth	Complexity	Compatibility
DPD	Moderate	High	Medium	ET, EF, EER
CFB	High	Low	Medium	ET, EF
PFB	High?	Low	Medium	EER
CFB+FF	High(er?)	Medium?	High	ET, EF
PFB+FF	High(er?)	Medium?	High	EER

4.3 Discussion and Summary

This section has superficially shown that there exists a very high number of possible schemes for implementing an RFPA system, when supply and linearization methods are taken into account as system parts. However, given the TETRA/TEDS application, the solution space shrinks somewhat. For the RFPA, current Motorola TETRA base stations are based on linear class-A/B designs, making this the easier RFPA route to try from a practical point-of-view. Further given the particularly difficult ACPR and WBN specifications for TETRA and TEDS, it is reasonable to prioritize PSRR (Power Supply Rejection Ratio) in the RFPA to increase immunity to power supply noise. Additionally, with a 50kHz target bandwidth for the TEDS carrier, the required power supply bandwidth for an EER-based amplification system is getting difficult at 100-250kHz. Therefore, as a compromise between technical difficulty and potential efficiency improvement, envelope tracking (ET) was the path of choice in this Ph.D project. For linearization, both DPD and CFB are directly compatible with ET. Given the tough ACPR specifications for TETRA and TEDS, Cartesian feedback (CFB) is the most direct path forward, this is again well-tested Motorola technology.

As such, the overall RFPA system solution mainly studied in this project was, arguably sensibly enough, the combination of a *linear class-AB* RFPA with a *medium-bandwidth variable power supply* operated in *envelope tracking* mode and *Cartesian feedback* linearization.

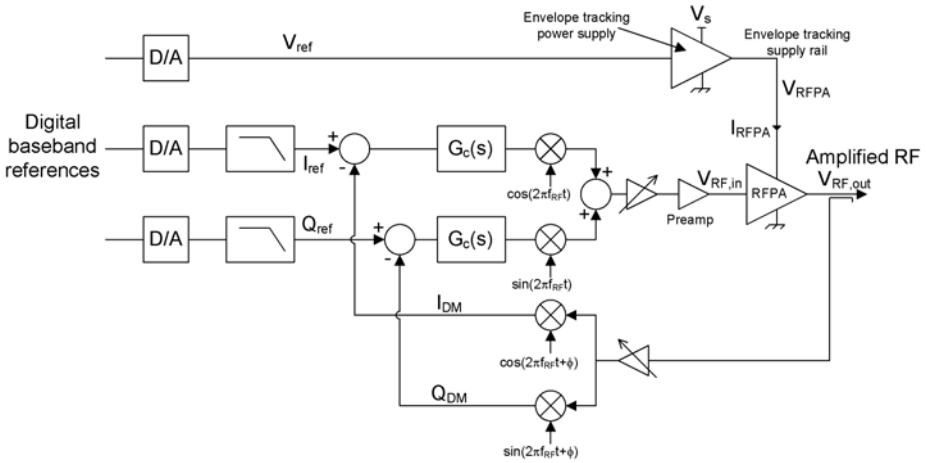


Figure 8: RFPA system solution mainly considered in this work.

5 Envelope Tracking Power Supplies

Only a subcomponent in a class of high-efficiency RF power amplification systems, the envelope tracking (ET) power supply is nonetheless worthy of a thorough study in its own right. This section provides an overview of candidate approaches for implementing such power supplies along with partial analytical comparisons.

5.1 Envelope Tracking Power Supplies in General

As a start, figure 9 shows a principal model of an ET power supply with sufficient details for this discussion. Note that $s = j2\pi f$ where f is frequency.

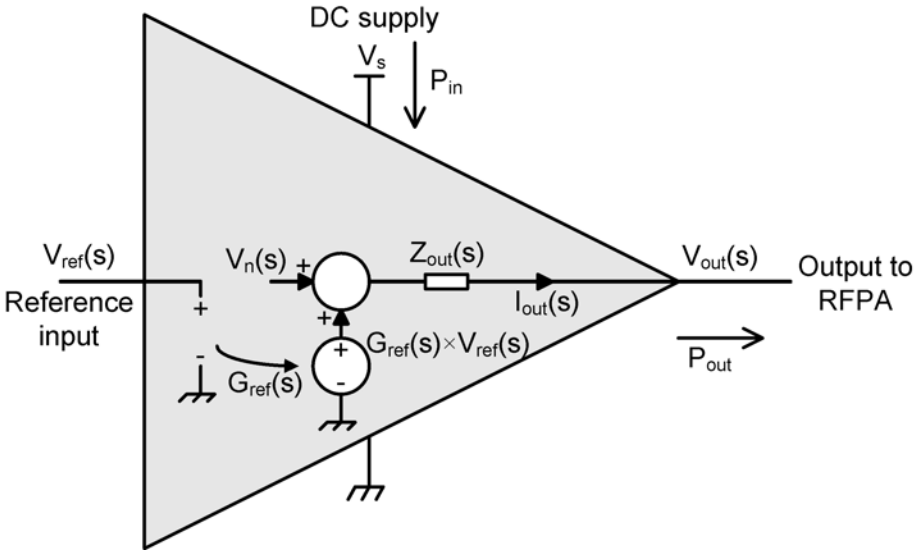


Figure 9: Generalized view of an envelope tracking power supply.

Referring to figure 9, any ET power supply is basically a power amplifier that is characterized by the following ports and properties:

- A DC supply input port.
- A reference input port.
- An output port that is partially controlled by the reference input port, generally with significant of voltage and power amplification.
- An input/output power efficiency P_{out}/P_{in} that should be as close to 100% as possible.
- A reference-to-output transfer function $G_{ref}(s)$ that is generally of low-pass nature.
- A non-zero, frequency dependent output impedance $Z_{out}(s)$ that makes V_{out} dependent on load current I_{out}.

- A noise source v_n that adds undesired components (e.g. switching ripple with switch-mode technology) to the output voltage.

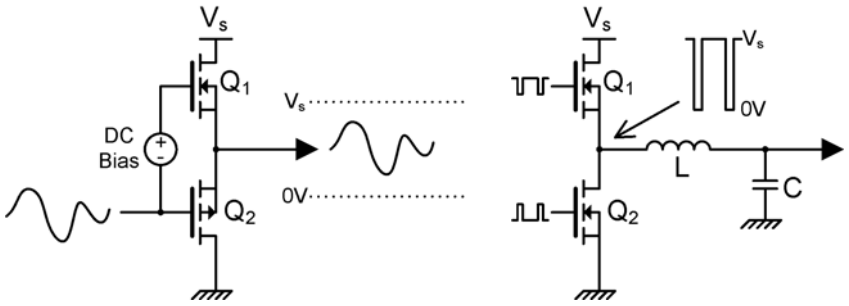
Getting closer to the application, the ideal ET power supply would have 100% efficiency, a constant for $G_{ref}(s)$ and zero $Z_{out}(s)$. It should of course also have zero implementation cost. With the real world currently providing only solutions that fall well short of this ideal, it is obvious that the ET power supply design problem is riddled with compromises.

5.2 Power Electronics for ET Power Supplies

Staying within mainstream electronics, it is generally valid that there are only two basic approaches available for powering the ET power supply output port:

- Transistors operated in the linear region, i.e. typically with both voltage and current present on drain/source (or collector/emitter) terminals. Power lost equals voltage times current.
- Transistors operated in the switched mode, so that simultaneous voltage/current on terminals is avoided, principally eliminating power loss.

For the ET power supply application, a typical linear transistor power stage would be a class-B push-pull pair (as illustrated in figure 10a) capable of both sinking and sourcing current from/to the output port. This is generally accepted to lead to poor efficiency [61] and should be avoided if possible. As demonstrated in audio power amplifiers, efficiency of linear power stages can be decent when multiple supply rails and power devices are used, like in the class-G configuration [61]. Linear power amplifiers can provide fast dynamics, depending only on the characteristics of the power devices. Noise from linear power amplifiers is likewise dominated by semiconductor noise which is often of "white" (constant spectral power density) nature.



(a) Linear class-A/AB/B (b) Switch-mode (buck-type)

Figure 10: Example transistor-based power stages.

Switch-mode power electronics is the application that most modern power transistors are geared toward, which is due to the ideally loss-less power conversion. A typical switch-mode power converter is the buck converter[6] shown in

[6]The buck converter is sometimes referred to as a "class-S modulator" in RF literature.

Table 4: Basic properties of linear and switching power amplifiers

Parameter	Linear	Switch-mode
Efficiency	Low-medium	High
Noise	Low	High
Bandwidth	High	Low

figure 10b. The main challenges with switch-mode technology are that switching introduces significant noise (mostly concentrated at the switching frequency) and that the switching rate and output filter impose limits on the dynamics of the output voltage.

These well-known basic properties of linear and switching power amplifiers are summed up in table 4.

It is important to note that linear and switching power sources may be combined in any number of ways. Practical examples include the effective stacking of linear voltage sources ("class-G" amplifier) or switching voltage sources ("multi-level" amplifier/inverter), the paralleling of phase-shifted switching power stages ("multi-phase"/"interleaved") or even paralleling of linear and switching power stages.

For any low-bandwidth power supply or amplifier, switch-mode power conversion will generally be able to provide far superior efficiency to that of linear power conversion at the expense of extra output noise. In the ET application, significant bandwidth is generally required along with low enough output noise. In general, bandwidth is potentially proportional to switching frequency. Power losses associated with the switching process are also proportional to switching rate, meaning that at some bandwidth, a linear power converter will have better efficiency than a switching power converter. In this project, given the 50kHz TEDS application target, it was assumed (and experimentally confirmed [36], [37], [38], [39]) that switch-mode technology could be stretched far enough to avoid the use of any linear power sources. For this reason, the following section focuses exclusively on switch-mode power conversion.

5.3 Switch-mode ET Power Supplies

Even though an infinite number of switch-mode power converters are possible, most can be considered derivatives of three fundamental topologies:

1. The buck topology, principally capable of converting V_s into any voltage in the range of $[0V, V_s]$.

2. The boost topology, principally capable of converting V_s into any voltage in the range of $[V_s, \infty]$.

3. The buck-boost topology, principally capable of converting V_s into any voltage in the range of $[0V, \infty]$.

All of these topologies have seen application in prior art ET power supplies. The early, often-cited work by Hannington [6] used the boost topology in discontinuous conduction mode (DCM). Another often-cited publication [10] proposed the buck-boost topology in continuous conduction mode (CCM) for use in slow peak-power tracking schemes. In both cases, battery-powered CDMA

equipment operating in the 1-10W output range was considered. Due to the limitations in battery voltages (3.6V for a typical Li-ion cell), the ability to provide an output above the input voltage is valuable in such applications. The difference between CCM and DCM operation is of importance for system dynamics in the boost and buck-boost topologies, since CCM operation in both cases is accompanied by a right half-plane (RHP) transmission zero [40]. Practically, RHP zeros limit the bandwidth of control loops to frequencies below that of the RHP zero. The buck topology notably has no RHP zero, and its dynamics are largely dominated by those of the output filter, which approximately is a simple pole pair. In the base station ET power supply application, it is reasonable to assume that the input voltage to the ET power supply can be more or less freely chosen, so that up-conversion capability of the ET power supply is not required. This, along with the fact that the buck converter has the simplest dynamics of the basic topologies, means that boost and buck-boost topologies are of little interest for the base station application. The reader should note however, that the ET power supply solution space is still large even though only buck-based converters are considered.

5.4 Buck-based switch-mode ET Power Supplies

With a large but manageable power conversion solution space at hand, it is now possible to divide this into a number of sub-spaces based on a number of key parameters[7]:

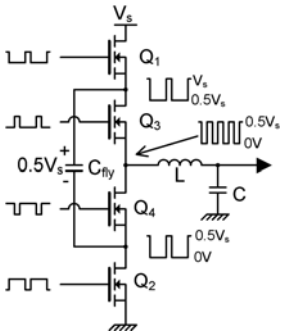
- The number of switching stages, a switching stage here by definition being capable of providing two voltage levels, $0V$ or V_s.
- Switching stage implementation - straight-forward "hard-switched" or "soft-switching" by addition of extra auxiliary power components?
- The connection of switching stages - parallel or series? A combination?
- The switching strategy of multiple switching stages. Same or different switching frequencies? Synchronous or phase-shifted if same frequency?
- The filtering strategy - normal second-order output filter or higher-order? Extra options available for converters with multiple switching stages.

With this parameter set, it is possible to categorize a lot of prior art along with the solutions generated in this project. This is done in table 5. The key contributions to the raw power topology selection offered by this Ph.D project are the "parallel buck" using different switching frequencies on the two power stages [42] and the 4th order filtered single-phase, soft-switching buck [37]. Much of the application-oriented research conducted has also been centered around the hard-switching 4th order filtered buck [36], [38], [39] with the 2nd-order filtered buck filling in for more theoretical and principal studies [44], [45], [46], [47], [48].

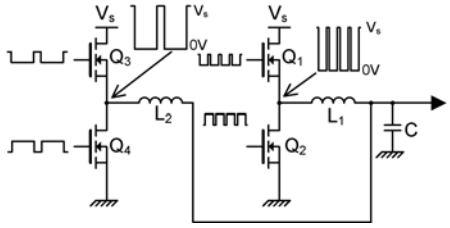
[7]This parameter list is sufficient for the following discussion but the author humbly acknowledges that it is probably possible given enough effort to find power topologies that will not "fit in".

Table 5: Buck-based ET power supply topologies proposed in open literature.

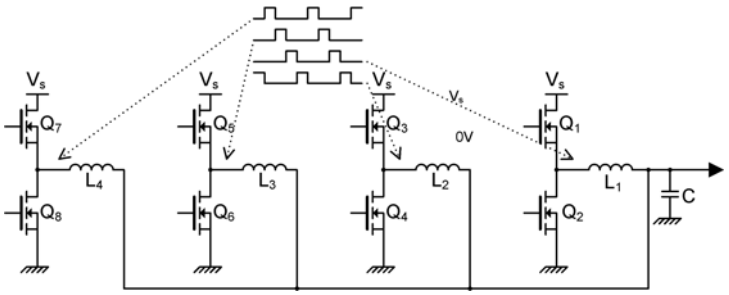
Topology, reference	Switching stages	Switching impl.	Stage connection	Switching strategy	Filtering strategy
Buck [30]	1	Hard	-	-	2nd order
3-level [41]	2	Hard	Series	Phase-shift	2nd-order
Par. buck [42]	2	Hard	Parallel	2-freq.	2nd-order
4-phase [43]	4	Hard	Parallel	Phase-shift	2nd-order
4th-order [20]	1	Hard	-	-	4th-order
4th-order s.s. [37]	1	Soft	-	-	4th-order



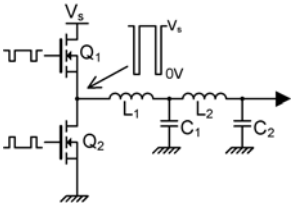
(a) Three-level buck [41]



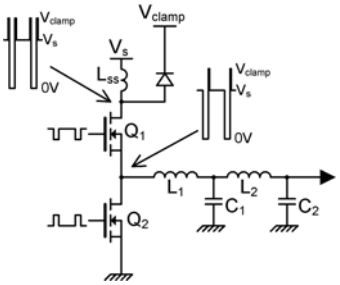
(b) Parallel buck [42]



(c) Four-phase buck [43]



(d) Fourth-order filtered buck [20]



(e) Soft-switching buck [37]

Figure 11: Considered buck-based ET supply topologies in addition to one-phase buck.

With this sorted out, the real question of interest is how the different topologies compare in the ET application and in particular in the 50kHz TEDS base station case. In order to do a proper comparison, it is prudent to have some basic specifications and assumptions to work from. Borrowing from later sections in this report, these are:

- The lowest corner frequency of any pole pair in the output filter equals the tracking bandwidth, i.e. 50kHz.
- Supply voltage V_s is 40V in order to accommodate a 10-30V output range.
- An output ripple of less than 10mVpp must be maintained in the 500kHz-5MHz range. Below 1MHz there is a "discount" of 6dB ripple per decade, i.e. 40mVpp is allowed at 250kHz. Further loosening follows the TEDS wideband noise spectral mask.

With regards to the frequency dependent ripple specifications, this is simply a result of having a CFB system that has integrator-style behavior at high frequencies as well as the frequency dependency of the TEDS WBN mask. In the case at hand, exploitation of this frequency dependency was not found to be of use. Drawing on the analysis presented in [39], a single-phase buck converter fitting the considered specification would need a switching frequency of at least

$$f_{sw,buck} = f_{filter} \cdot \sqrt{\frac{4}{\pi} \frac{V_s}{\Delta V_{out,pp}}} \tag{1}$$

where f_{filter} is the output filter cut-off frequency and $\Delta V_{out,pp}$ is the peak-peak ripple voltage allowed. In this case, the switching frequency ends up at an impractical and probably inefficient 3.6MHz.

Going to the three-level buck, this topology applies half the amplitude of switching harmonics to the filter, at twice the per-stage switching frequency. As a result, output ripple is reduced by a factor of 8 for the same output filter and per-stage switching frequency as the buck. Hence, for maintaining the ripple specification with a given filter we need (as also stated in [41]) a switching frequency of

$$f_{sw,buck3lvl} = \frac{1}{2\sqrt{2}} \cdot f_{sw,buck} \tag{2}$$

which means 1.3MHz in the considered case. This substantial and useful reduction comes at the cost of extra power semiconductors and higher control complexity.

With regards to the parallel two-frequency buck topology, this is superficially more difficult to analyze since there are different but interacting power stages, filter cut-offs and control loops and as such also a non-punctual solution space. The ripple point-of-view was never considered in [42]. However, looking at the waveforms in this topology (see figure 12) it is clear that it will produce a high-frequency ripple equal to that of the single buck converter, with an added lower-frequency ripple produced by the low-frequency converter. Therefore, even if we generously give this topology the benefit of doubt with regards to the low-frequency ripple, it will still be as bad as the basic buck with regards to the fast

converter switching frequency:

$$f_{sw,parbuck} = f_{sw,buck} \tag{3}$$

Efficiency of this topology can still be better than that of the single-phase buck since DC and slow AC current loads are diverted to the more efficient, slower switching power stage. In the ET application, this could be of marginal use since linear RFPAs will have significant DC components in their load currents due to RF power device bias currents.

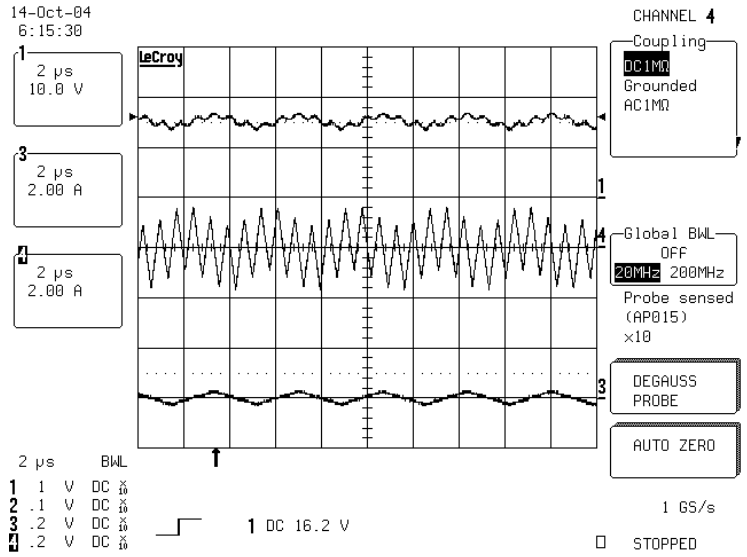


Figure 12: Ripple waveforms in parallel buck [42]; V_{out} (top), I_{L1} (mid), I_{L2} (bottom).

Multi-phase buck topologies are characterized by reduced overall output ripple in comparison with single buck converters. In order to simplify output ripple analysis, it is easiest to consider the multi-phase interleaved buck converter looking into the N phase inductors from the filter capacitor. From here, it is impossible to tell the difference between N paralleled buck switching stages driving each their inductor of $N \cdot L$ and an $N+1$-level switching stage driving an inductance of L. An $N+1$-level switching stage produces an output in V_s/N steps, so the maximum peak-peak switching frequency fundamental component is:

$$v_{fund,pp}(N) = \frac{4}{\pi} \cdot \frac{V_s}{N} \tag{4}$$

The effective switching frequency is $f_{sw} \cdot N$. Thus, in comparison with the single buck converter, the multi-phase interleaved buck produces an effective PWM signal that has N times the per-phase switching frequency and with a maximum switching frequency AC content that is N times lower. With a second-order output filter this leads to a ripple reduction of N^3 due to the second-order slope of the filter magnitude response. Hereby, the normalized switching frequency requirement is:

$$f_{sw,N-phase} = f_{sw,buck} \cdot \sqrt{N^3} = f_{sw,buck} \cdot N^{\frac{3}{2}} \tag{5}$$

For the two-phase (or three-level) buck we get the already found reduction factor of $2\sqrt{2}$. In the four-phase case, the reduction factor improves to 8.

For the fourth-order filtered single-phase buck converter, the second filter stage adds extra ripple attenuation [39] leading to:

$$f_{sw,buck4th} = \sqrt{f_{p1} \cdot f_{p2}} \cdot \sqrt[4]{\frac{4}{\pi} \frac{V_s}{\Delta V_{out,pp}}} \tag{6}$$

$$f_{sw,buck} = f_{filter} \cdot \sqrt{\frac{4}{\pi} \frac{V_s}{\Delta V_{out,pp}}} \tag{7}$$

where f_{p1} and f_{p2} are the output filter corner frequencies, one of which has to equal f_{filter} (50kHz) with the other frequency substantially above this. Setting $f_{p1} = f_{filter}$ and $f_{p2} = \alpha \cdot f_{filter}$ we have:

$$f_{sw,buck4th} = \sqrt{f_{filter} \cdot \alpha f_{filter}} \cdot \sqrt[4]{\frac{4}{\pi} \frac{V_s}{\Delta V_{out,pp}}} \tag{8}$$

re-arranging leads to

$$f_{sw,buck4th} = \sqrt{\alpha f_{filter}} \cdot \sqrt{f_{filter} \cdot \sqrt{\frac{4}{\pi} \frac{V_s}{\Delta V_{out,pp}}}} \tag{9}$$

Here it is possible to insert the expression for $f_{sw,buck}$, leading to:

$$f_{sw,buck4th} = \sqrt{\alpha f_{filter}} \cdot \sqrt{f_{sw,buck}} \tag{10}$$

Using an α value of 7 (rounding up on numbers from published designs [36], [38], [39], [37]) results in a switching frequency of 1.1MHz. Using a more difficult filter design with $\alpha = 4.57$ as published in [37]) reduces this to 910kHz. Although no formal proof is offered in this thesis, it has been found that designing filters for low values of α requires a high difference in impedance level between the two LC stages and hence either ripple current (controlled by L_1) or output impedance (mostly controlled by the sum of L_1 and L_2) will be high. Hence, "high" values of α are pessimistic whereas "low" values of are optimistic.

The derived switching frequency equation for the fourth-order filtered buck is structurally different from the other equations derived in that the reduction factor is dependent on f_{filter}. Upon closer inspection this equation reveals the major advantage and application area of the fourth-order filter buck topology - namely ultra-low ripple designs where the switching frequency can be maintained well above the required bandwidth. This is a logical result of the fourth-order slope of the magnitude response of the filter.

Figure 13 shows how the ripple specification affects the switching frequency requirement in the studied topologies, given the 50kHz bandwidth requirement and 40V supply.

It is clearly evident that the fourth-order filtered buck is the superior to three-level solution as long as relatively low ripple is required. The four-phase buck is superior to both of these in the whole ripple area of interest. However, this comes at the a significant increase in power component count. Since the single-phase buck with a fourth-order filter is capable of delivering the desired

level of ripple performance with reasonable switching frequencies (1-2MHz) there is reason in examining this topology.

The three-level and multi-phase buck topologies should be capable of better efficiency for a given switching frequency, and both can be upgraded with an extra output filter LC section. The class of multiphase series/parallel-connected buck power stage based converters equipped with higher-order output filters are a little-explored, promising part of the solution space. However, as the next section will show, the single-phase buck converter has a substantial advantage in comparison with the multi-phase converters: It is receptive to self-oscillating (a.k.a. sliding mode) control methods. This property can be put to good use when an unwieldy fourth-order output filter needs to be controlled with speed and accuracy.

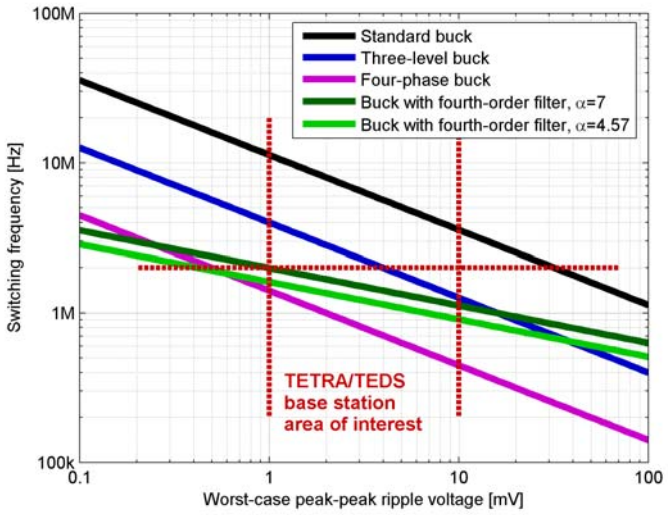


Figure 13: Switching frequencies for different buck topologies; $BW = 50kHz$, $V_s = 40V$.

Figures 14 and 15 are included as validation of the performed analysis and in particular the results in figure 13. For the typical choice of 1MHz switching frequency, the simulation models predict the same worst-case ripple (over 0-100% duty cycle variation) as the analysis. The start-up responses (where the output filter models converge from initial condition of zero on all state variables toward steady-state) show that the different filters have been scaled correctly so that the lowest cut-off frequencies and impedance levels are the same.

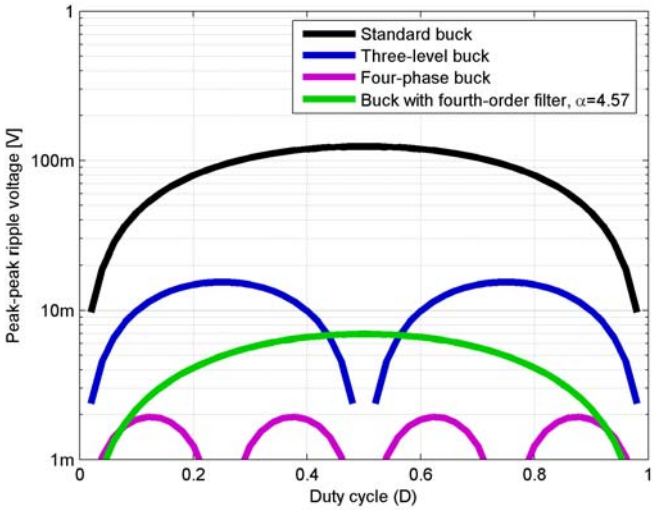


Figure 14: Simulated (time domain with switching waveforms) output ripple of different buck topologies; $f_{fw} = 1MHz$, $BW = 50kHz$, $V_s = 40V$. Worst-case ripples correspond with figure 13.

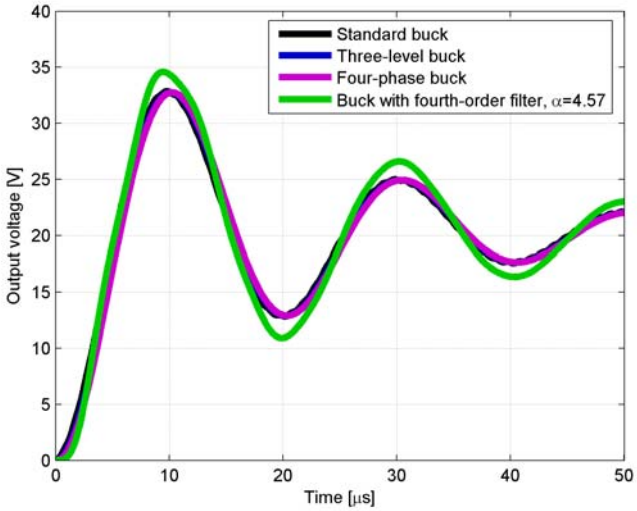


Figure 15: Start-up responses of simulation models used for figure 14. All models have the same $50kHz$ eigenfrequency ensuring a fair comparison.

A rough comparison of the properties of the studied buck-based power topologies is given in table 6. Complexity is evaluated weighing the amount of control circuitry, high-side MOSFET drivers, power devices and filter components. Ripple evaluation is based on results in figure 13. Efficiency is likewise based on figure 13, with low switching frequency and interleaving assumed to promote higher efficiency. Cost is based on the number of power components, assuming

Table 6: Comparison of buck-based ET power supply topologies.

Topology	Complexity	Ripple	Efficiency	Cost
Buck [30]	Low	High	Low	Low
3-level [41]	Medium	Medium	Medium	Medium
Par. buck [42]	Medium/high	High	Low/medium	Medium
4-phase [43]	High	Very low	High	High
4th-order [20]	Low/medium	Low	Medium	Low/medium
4th-order s.s. [37]	Medium	Low	Medium+	Medium/high

that MOSFET drivers, power MOSFETs and output filter L/C components are of similar cost per item. The reasoning behind the focus on the fourth-order filtered single phase buck is again evident; this topology is capable of providing low ripple for a relatively simple, low-cost power circuit. Adding soft-switching circuitry increases overall cost and potentially adds a little to efficiency [37].

5.5 Summary

This section has shown a hierarchical descent into the solution space for envelope tracking power supplies, in the process removing all but switch-mode buck-type solutions. Low-noise power conversion with transistors operating as linear transconductances is more than counterbalanced the associated low efficiency. Likewise, the input voltage flexibility of non-buck switch-mode topologies is not worth the dynamic trouble that follows. Among the buck-based solutions, several candidates have been demonstrated, with the single-phase, fourth-order filtered buck identified as offering a good compromise between ripple, efficiency and cost for the 50kHz TEDS envelope tracking application. In particular, output ripple in the 1-10mV (peak-peak) area from a 40V supply has been shown to be achievable with this topology with reasonable switching frequencies (1-2MHz) and an output filter with its lowest corner frequency at 50kHz. For substantially higher bandwidths, only a vastly more complex multiphase converter or a switching/linear combination can deliver the same ripple performance if the 1-2MHz per-phase switching frequency is to be maintained.

6 Controllers for buck-based ET power supplies

In addition to the power converter topology, an ET power supply is characterized by the control scheme used to get linear amplifier behavior from the power components. Numerous control methods have been proposed in the literature along with different classification systems. This section presents a comparison of some of these methods along with the proposition that almost all of these can be described as systems made up of linear time invariant (LTI) networks, comparators and external stimulus signals. This basic point-of-view has often been adopted in prior art, but not for all the control topologies considered here.

6.1 Common control system classifications

Common examples of binary classifications in various areas of the solution space relevant for buck converters include:

- Voltage-mode <=> current-mode
- Fixed-frequency <=> variable-frequency
- Linear <=> non-linear
- Clocked <=> self-oscillating
- Analog <=> digital
- Single-phase <=> interleaved

The classifications above lead to the impression that the set buck converter controllers is big and segmented. A slightly more general but still common set of parameters that allow classification of many ET power supply control schemes is:

- Switching frequency source - external clock/carrier or self-oscillation (SO)?
- Signals fed back - current(s), voltage(s)?
- Compensator(s) in control system - PI/PID/PD/$(PI)^2$-lead/?
- Number of power converter phases controlled.
- Phase/frequency strategy for different phases.

Note that this simplified parameter set is inadequate for considering digital and mode-switching controllers since these types of control were not considered to be of interest. The term "mode-switching controllers" here refers to schemes that use a stable and predictable control strategy for steady-state operation and another, usually faster but less predictable/ideal strategy for transient conditions. Examples include the digital PWM/switching surface controller.

The main reasons for disregarding digital and mode-switching controllers are:

- Control bandwidth is hampered by ADC delays in digital controllers. Control bandwidth is here considered important due to the dynamical nature of the ET application.

Table 7: Classification of proposed analog control techniques for buck-based ET power supplies.

Ref.	A.K.A.	Osc.	FB	Compensation	Phases	Ph./freq. strategy
[30]	Voltage mode	Ext.	V	PID	1	N/A
[41]	Open-loop	Ext.	None	N/A	2	Phase-shift
[42]	Sliding	Int.	V/I	PI	2	2-frequency
[43]	Current mode	Ext.	V/I	PI	4	Phase-shift
[36]	Sliding	Int.	V	PID + PD	1	N/A
[37]	Sliding	Int.	V	D + PID-lead	1	N/A

- Output noise is increased with digital PWMs due to limited DPWM resolution or the use of noise shaping to counteract this. Limited ADC resolution adds to this. ET power supplies for TETRA and TEDS need to have low output noise over a wide bandwidth.

- Mode-switching controllers are good for load steps in VRMs - but probably not in systems that feature continuous, fast, noise-like variations in output voltage and current.

Additionally, most ET power supply literature considers some form of analog control. Proposed/used analog control solutions for ET power supplies include those listed and categorized in 7. An exhaustive listing of possible schemes is near-impossible due to the number of parameters and attainable values for each, as well as the limitations of this parameter set.

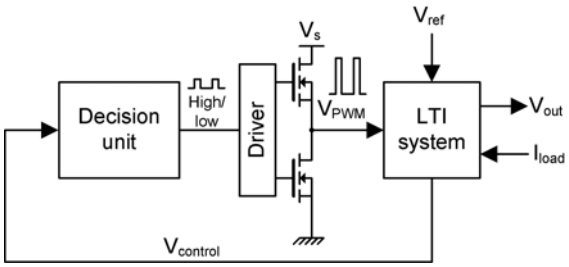
The next section introduces an abstraction that allows all of the control solutions in table 7 (among others) to be represented using two simple parameters. This abstraction notably leads to a much-simplified view of the buck converter control systems, allowing some of the more fundamental differences between solutions to be observed.

6.2 The LTI network and decision unit abstractions

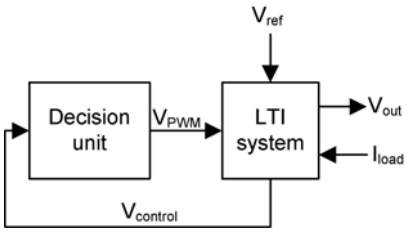
A common feature of all the considered control schemes and many others is that the PWM voltage from the switching stage is fed to circuitry which can be reasonably described as linear and time-invariant (LTI.) This includes the output LC filter and feedback compensation circuits. Outputs of the LTI circuitry include the output voltage and a number of control voltages. In any switch-mode feedback based control system, control voltages are fed to what is here called "decision units" that generate the high/low switching command for the switching stage. An example of a "decision unit" is the standard pulse-width modulator that converts a modulating voltage into a pulse width modulated high/low sequence that can drive the buck switching stage. The "LTI and decision unit" system abstraction is illustrated in figure 16a for single-phase buck converters. Assuming that the buck converter input voltage V_s is constant, it is easy to see that the buck switching stage is really only a pulse amplifier, effectively boosting (and perhaps level shifting) the output of the decision unit. As such, it is reasonable to place the gain of the switching stage in the decision unit and the delay, if relevant, in the LTI system as illustrated in figure 16b. If multiple buck switching stages exist in the system, each has its own decision unit but the LTI system is still common as illustrated in figure 16c. By feeding the

PWM signals into each their phase inductor in the LTI system, any multiphase interleaved buck can be described. Similarly, by instead adding (and scaling down by N) the PWM signals inside the LTI block, multilevel buck topologies can be handled.

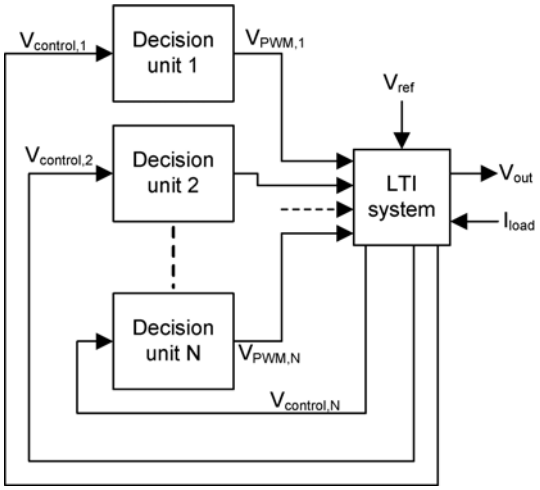
Adopting the generalist "LTI and decision unit" point-of-view, it is easy to see that otherwise "very different" control schemes like PID voltage mode and average current mode (figure 20) only differ in the make-up the LTI-part of the system since the same decision unit is used. Comparing PID voltage mode and peak-current-mode control we have different LTI structures as well as different decision units.



(a) Basic view with switching stage shown.

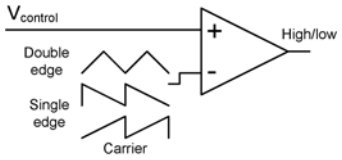


(b) Simplification by incorporation of switching stage into decision unit and LTI system.

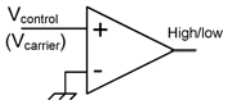


(c) Extension to multi-phase system, usable both on interleaved and multi-level configurations.

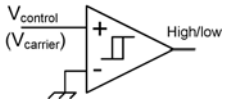
Figure 16: Generalized views of buck-based power supplies with feedback control.



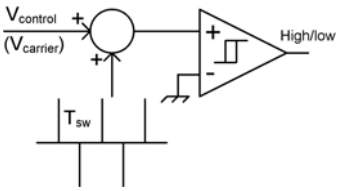
(a) Standard PWM



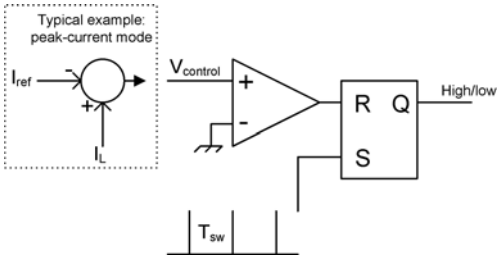
(b) Comparator



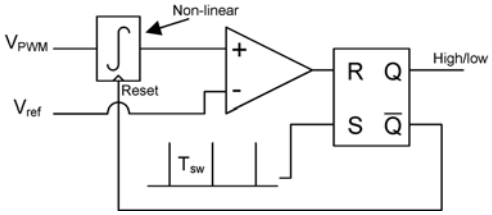
(c) Comparator with hysteresis



(d) Comparator with hysteresis and "spike" synchronization



(e) "Peak-mode" and its typical application



(f) One-cycle. Not compatible with most LTI structures since loop filter has to be reset in every decision (switching) cycle.

Figure 17: Examples of decision units used for control of buck power stages.

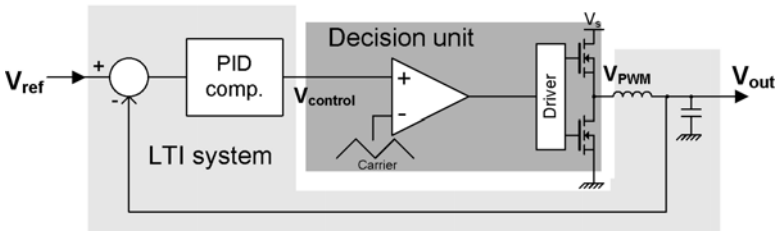


Figure 18: Voltage-mode

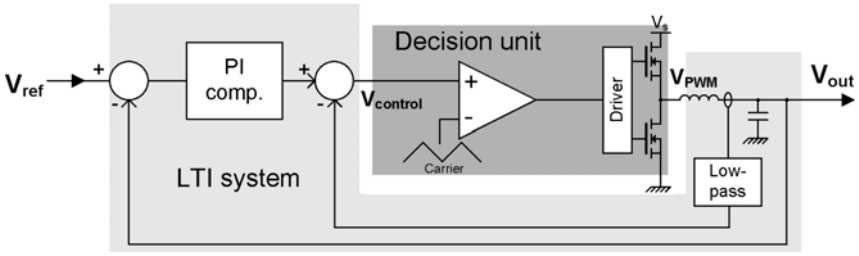


Figure 19: Average current-mode

Figure 20: Examples; decision units and LTI system in "voltage-mode" and "average current-mode" controlled buck converters.

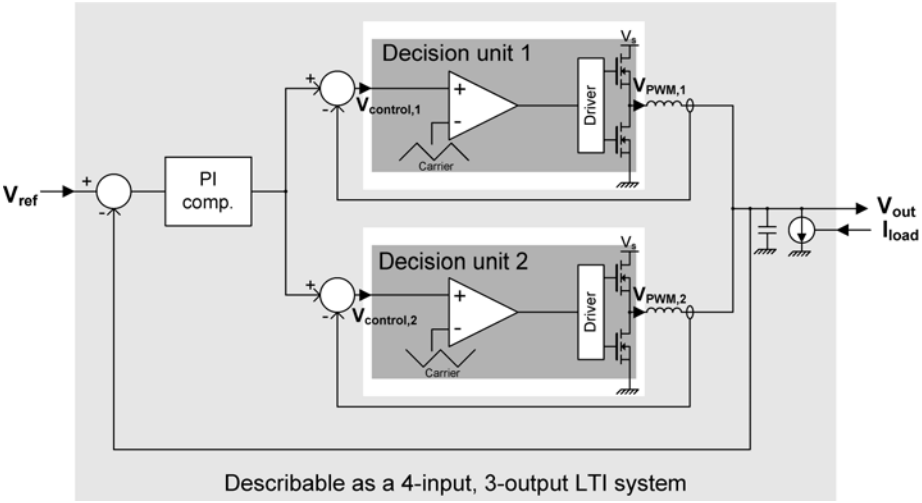


Figure 21: Example; decision units and LTI system in a two-phase interleaved buck converter with current feedback and PI voltage control loop.

6.3 System models based on LTI system and comparators

Due to the availability of promising modeling techniques for comparators in single-phase buck switching converters [48], [51], it is worthwhile to try to re-compose the decision units of the previous section into behavioral models containing only LTI components and a comparator. Doing this brings us close to

something that can be modeled and, as will be apparent, allows some (somewhat unexpected) overlaps between decision units to be illustrated. It is taken as granted that any LTI blocks in the decision units can be incorporated into the already existing LTI system that describes compensators, filters and switching stages.

Figure 22 shows the basic comparator/LTI model of a buck converter control system adopted in [51], which turns out to be a concept with a long history [62], [63]. The value added by [51] is the inclusion of external "synchronization" signals to let this system structure describe control systems that are not self-oscillating. The well-known pulse-width modulator may as such be modeled as a comparator with a triangle wave added to its input as illustrated in figure 23a. Hysteresis in a comparator is modeled in the same way as hysteresis is sometimes implemented; using positive feedback (figure 23c.) For hysteresis-based controllers using externally generated synchronization pulses for achieving constant switching frequency [32], the synchronization pulses are simply modeled as a two interleaved trains of dirac delta pulses (a postive-going and a negative-going train) added to the hysteretic comparator input (figure 23d.) For the peak-mode decision unit, the latching action of the unit is modeled using hysteresis. Synchronization (turn-on of the power switch at a specific time determined by an external clock) is modeled using an external, positive-going dirac pulse train (figure 23e.) Slope compensation is similarly modeled as an added sawtooth signal. The reader can inspect example waveforms for this model in figure 24 to see that overall operation is identical to that of the usual comparator+latch implementation of figure 17e.

As an off-key comment, it is delightfully tempting to question whether spike-synchronized hysteretic controllers deserve to be called "sliding mode" [32] since this would imply that peak current-mode controllers without slope compensation are also "sliding mode", at least in a limited duty cycle area.

The one-cycle decision unit was unfortunately found to be incompatible with the approach of separating the LTI and comparator parts. This is because the loop filter (integrator) output depends on an external signal (the reset/sync pulse) that in itself is modulated by the loop filter output. More specifically, it *is* possible to reset an integrator to zero by applying a correct-sized delta pulse every cycle, but the delta pulse has to be proportional to the loop filter output at the time of reset. Therefore, the loop filter cannot be considered a stand-alone LTI system. From a practical viewpoint, the ET power supply application benefits from having the buck converter output filter inside the control loop since this lessens the impact of load disturbances. The basic one-cycle control structure offers no direct solutions to this since it is not possible to reset every state in the loop filter when the loop filter contains a physical LC low-pass filter operating at significant power levels. It is therefore mostly a loss at academic level not to include the one-cycle controller in the following. As a final note, it is not to be taken as impossible to apply the comparator/LTI modeling technique to one-cycle control. As a deterministic system, the one-cycle controller has to have a specific impulse response and therefore also a specific transfer function.[8]

For multiphase/level control systems with multiple decision units, the comparator modeling approach used in the next section has yet to be extended to

[8]Since a transfer function by definition is the Laplace transform of the system impulse response [64].

handle systems with multiple comparators. Although a very interesting subject, this has been left out of the thesis due to time limitations. For the special case of a multiphase/level control system using standard PWM decision units, it is guessed that the N decision units can be modeled as a single decision unit operating at N times the frequency of the individual, physical decision units. Further studies along this path were cut off by the project end date.

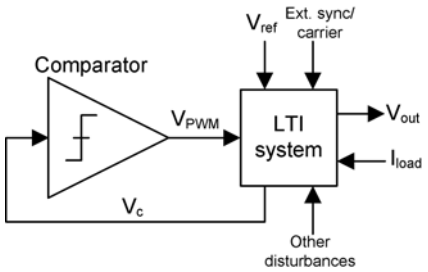
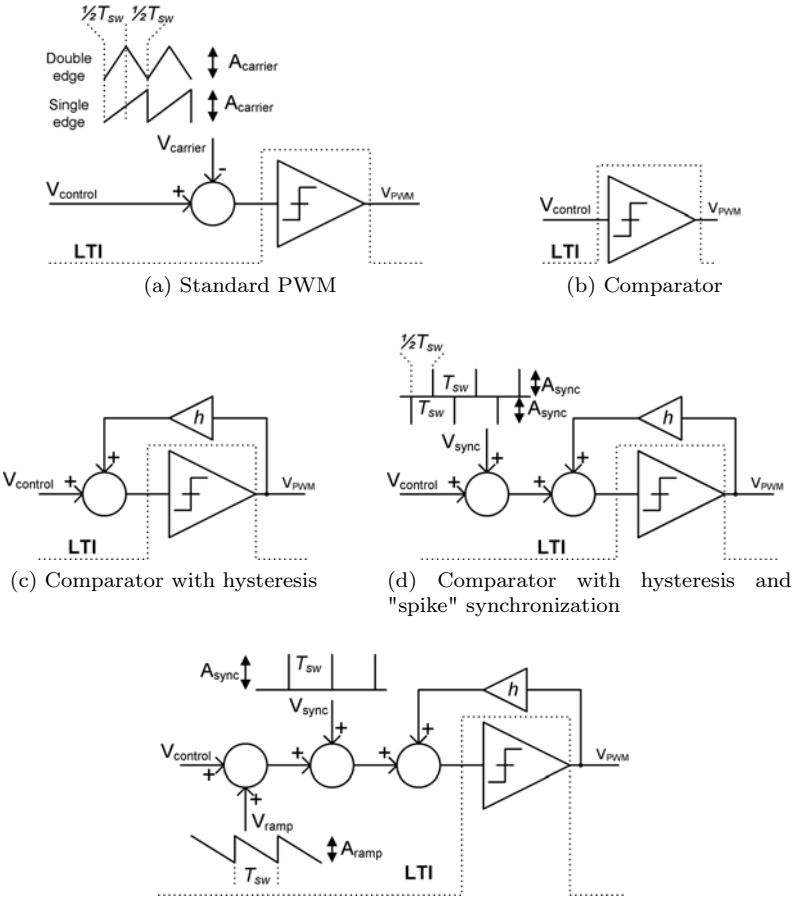


Figure 22: Generic model of single-phase feedback controlled buck converter with comparator as only non-linearity.



(a) Standard PWM

(b) Comparator

(c) Comparator with hysteresis

(d) Comparator with hysteresis and "spike" synchronization

(e) Non-inverting peak-mode

Figure 23: Decision units recomposed into comparator and LTI parts for compatibility with universal comparator modeling technique [51], [48].

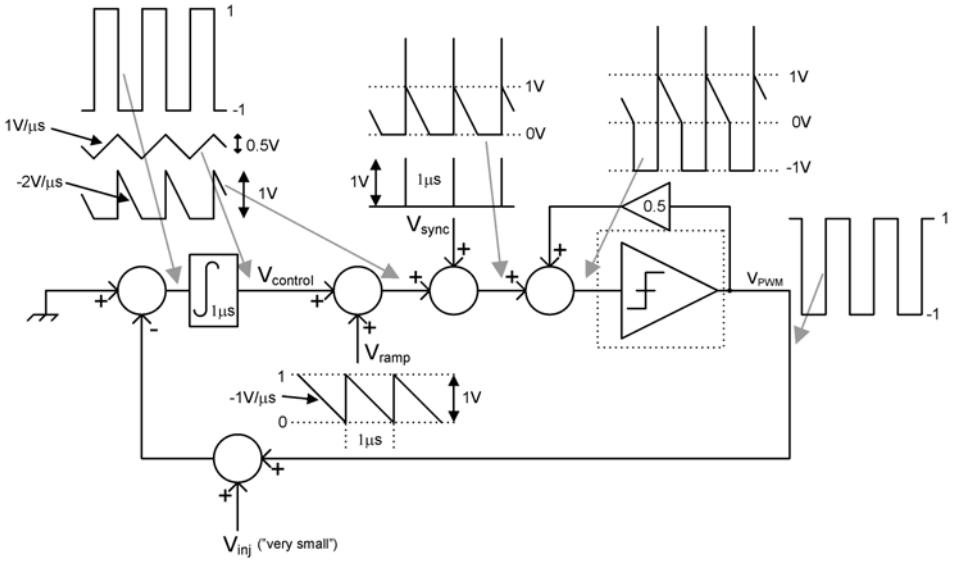


Figure 24: Complete Simulink-style comparator/LTI model (with example waveforms) of peak-mode controlled single-phase buck converter with integrator loop filter as used in next section's comparison.

6.4 Comparator and decision unit frequency responses

Referring to [48] and [51], the comparator in the decision units may be described in the discrete-time domain as a simple gain K_z. This reflects that the result of applying a small perturbation on its input results in a shift in the sampling (switching) time, thus correspondingly shifting the output PWM edge transition, effectively adding a narrow pulse (modeled as a dirac delta pulse of a given magnitude) to the PWM pulse train. Further modeling the LTI part of the control system in the discrete-time domain, we have a complete discrete-time loop model. Since the physical loop filter is analog (or continuous-time) and the discrete-time model passes impulses between blocks, the loop filter impulse response properties must be preserved when transforming it into the discrete-time domain. This is done using the impulse-invariant transform [51]. The net result of this is a model capable of describing the discrete-time response of the PWM control loop to an externally applied sine wave perturbation [51].

For experimental verification of loop gains and individual block frequency responses (not provided in [51]), a gain-phase analyzer is the standard-issue piece of measurement equipment. This instrument injects a small sinusoidal perturbation at a given frequency and compares the signal magnitudes and phases at the perturbation frequency in a given set of nodes. Effectively this results in a measurement of the gain and phase shift from one node to the other at the perturbation frequency. Importantly, the gain-phase analyzer applies a narrow bandpass filter to the measured signals so that no aliasing components (as present in a discrete-time system) are seen. Therefore, in order to verify the discrete-time system model with a gain-phase analyzer, it is necessary to evaluate the narrow-band, continuous-time responses of the considered nodes to the injected perturbation [48]. The frequency response of the PWM node

to the injected perturbation is assumed [51] to be identical in the discrete -and continuous-time domains. This is at least true from DC to twice the switching frequency since the DC/LF and first harmonic sideband components in a modulated PWM signal are of equal magnitude and phase. In order to assert this, consider the sine wave

$$x(t) = M\pi \cos(\omega_s t) + 2\pi k \tag{11}$$

which when he trailing-edge pulse-width modulated has the double Fourier series [54]:

$$\begin{aligned} F_1(t) = &\overbrace{k}^{\text{DC}} + \overbrace{\frac{M}{2}\cos(\omega_s t)}^{\text{DC sideband}} + \overbrace{\sum_{m=1}^{\infty} \frac{\sin m\omega_c t}{m\pi}}^{\text{Square wave harmonics}} \\ &- \overbrace{\sum_{m=1}^{\infty} \frac{J_0(m\pi M)}{m\pi} \sin(m\omega_c t - 2m\pi k)}^{\text{Alteration of square wave harmonics with } M} \\ &- \overbrace{\sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{J_n(m\pi M)}{m\pi} \sin\left(m\omega_c t + n\omega_s t - 2m\pi k - \frac{n\pi}{2}\right)}^{\text{Sidebands - n'th sideband to m'th square wave harmonic}} \end{aligned} \tag{12}$$

where $J_n(x)$ is the Bessel function of order n. Since the analysis here and in [48] and in [51] is constrained to small signals, the argument put into the Bessel functions is always also "small". Further, we only look at the first upper sideband, so $n = 1$. Hence, only the first Bessel function is needed, and for small arguments ($x < 1$), we can approximate [66] that $J_1(x) \approx \frac{1}{2}x$. This means that the first upper sideband ($n = 1$) to the m'th harmonic of the switching frequency can be approximated as:

$$V_{SB1,m}(t) = -\frac{M}{2} \sin\left(m\omega_c t + \omega_s t - \frac{\pi}{2}\right) \tag{13}$$

which may be rewritten to

$$V_{SB1,m}(t) = \frac{M}{2} \cos(m\omega_c t + \omega_s t) \tag{14}$$

Hence it has been shown that the first upper sideband to any harmonic (at least the first couple) of the PWM frequency for small amplitudes (small M) is both of the same phase and amplitude as the DC sideband. This critically means that a gain-phase analyzer cannot tell the difference between the DC sideband and any of the first upper sidebands. Of course, the above is specific for trailing-edge modulation. However, leading-edge modulation only differs in that $F_2(t) = F_1(-t)$ [54] and for the case of the first upper sidebands these are now given as:

$$V_{SB1,m}(t) = \frac{M}{2} \cos(m\omega_c - t + \omega_s - t) \tag{15}$$

which is of course the same as for trailing edge modulation since the cosine function is symmetrical around zero. Going to double-edge modulation, which

may be considered a sum of trailing and leading-edge modulated signals, the relationship between the DC sideband and the first upper sidebands is still preserved. Thus, for any of the modulation forms we have an exact 1:1 mapping from the cyclical spectrum of the discrete-time representation of the PWM signal to the first upper sidebands, as assumed in [48] and in [51].

Now, for comparison of the different decision units, the following system configuration was considered:

- Single-phase buck power stage operating at f_{sw} from rails $+/-V_s$ with overall delay t_d.
- Integrator loop filter with time constant τ_{int} for simplicity.
- Duty cycle $D = 50\%$ to allow accurate modeling.

In order to make the comparison fair and transparent, the same time constant was used for the loop filter in all cases. The s-domain loop filter $H_s(s) = \frac{1}{\tau_{int} s}$ becomes $H_z(z) = \frac{z^{-1}}{\tau_{int} T_s z^{-1}}$ in the z-domain. Here, sampling period T_s has been used explicitly since this is not the same for all the considered decision units.

To extract maximum performance from the PWM decision units, the carrier amplitudes were tuned to exactly avoid ripple instability for all duty cycles while maximizing PWM small-signal gain. This effectively translates to making the minimum carrier slope numerically equal to the maximum feedback ripple signal slope. The latter occurs at $D = 0$ and $D = 1$, where the feedback ripple has a maximum slope magnitude of $\frac{2V_s}{\tau_{int}}$. This means that the carrier slopes should be minimum

$$\frac{dV_{carrier}}{dt} > \frac{2V_s}{\tau_{int}} \tag{16}$$

For the single-edge (SE) PWM, the carrier slope is also given by

$$\frac{dV_{carrier,SE}}{dt} = A_{carrier} \cdot f_{sw} \tag{17}$$

Correspondingly for the dual-edge (DE) PWM we have

$$\frac{dV_{carrier,DE}}{dt} = 2A_{carrier} \cdot f_{sw} \tag{18}$$

This means that the single-edge PWM should have a carrier amplitude of

$$A_{carrier,SE} > \frac{2V_s}{f_{sw} \cdot \tau_{int}} \tag{19}$$

Likewise for double-edge:

$$A_{carrier,DE} > \frac{V_s}{f_{sw} \cdot \tau_{int}} \tag{20}$$

We note that for this comparison the single-edge PWM has twice the carrier amplitude of the double-edge PWM. Also, the slope of the comparator input at the sampling instants in both cases is increased by a factor of 1.5 at $D = 0.5$ over the carrier slope since the feedback signal ripple has half the carrier slope

for $D = 0.5$. Alternatively, this may expressed as the comparator input slope being three times higher than the feedback ripple slope.

For the peak-mode decision unit, slope compensation [40] was used to ensure stability for all duty cycles. Minimum slope compensation (corresponding to maximum loop gain, see figure 9 and equation (13) in [65]) is the slope of:

$$|\frac{dV_{ramp}}{dt}| > max\left\{\frac{1}{2}\frac{dV_{control}}{dt}\right\} \tag{21}$$

Again, the feedback ripple has a maximum slope of $\frac{2V_s}{\tau_{int}}$ so the compensation ramp amplitude must be at least:

$$A_{ramp} > \frac{V_s}{f_{sw} \cdot \tau_{int}} \tag{22}$$

Here the comparator input signal slope is increased by a factor of 2 over the ramp slope.

For the latching behavior of the peak-mode decision unit, hysteresis feedback block h simply has to be large enough to ensure that $V_{control}$ cannot turn the comparator output back on. A_{sync} should then be made large enough to ensure that the hysteresis level is crossed to switch the comparator output back to "high".

For the hysteretic comparator decision unit, the only free parameter is the hysteresis window as set by gain h; this is straightforwardly [52] found as

$$h = \frac{K}{2} \cdot (4f_{sw} - t_d) \tag{23}$$

where K is twice the feedback ripple slope for $D = 50\%$.

For the spike-synchronized hysteretic decision unit, the free-running oscillating frequency was set slightly below the synchronization frequency in order to allow the synchronization spikes to alone determine the timing of one of the switching events per cycle. This was done by setting the hysteresis window 20% higher than for the self-oscillating case.

The model parameters for the considered decision units are summed up in tabel 8. Together with $H_s(s)$, $H_z(z)$ and the expression for continuous time decision unit frequency response $K_s(s)$ from [48], the data of this table allows prediction of the decision unit frequency response. Importantly, none of the studied decision units feature the same combination of comparator input signal slope and sample period. This provides a low-level angle to explaining the difference between these decision unit in place of simply considering the differences in physical implementations and waveforms.

6.5 Overall comparison

The results of evaluating $K_s(s)$ for the considered decision units are shown in figures 25a and 25c for gain and phase respectively. Corresponding swept-sine simulated results are shown in figures 25b and 25d. Simulations made with the swept-sine method are here argued to present a reasonably accurate reflection of reality (as observed with a physical gain-phase analyzer measuring signals on a physical circuit board) based on the experience from papers [44] and [45]. Loop gains are likewise evaluated in figures 26a, 26b 26c and 26d.

Table 8: Comparator model parameters (under given assumptions) with different decision units in a single-phase buck converter switching at frequency f_{sw}.

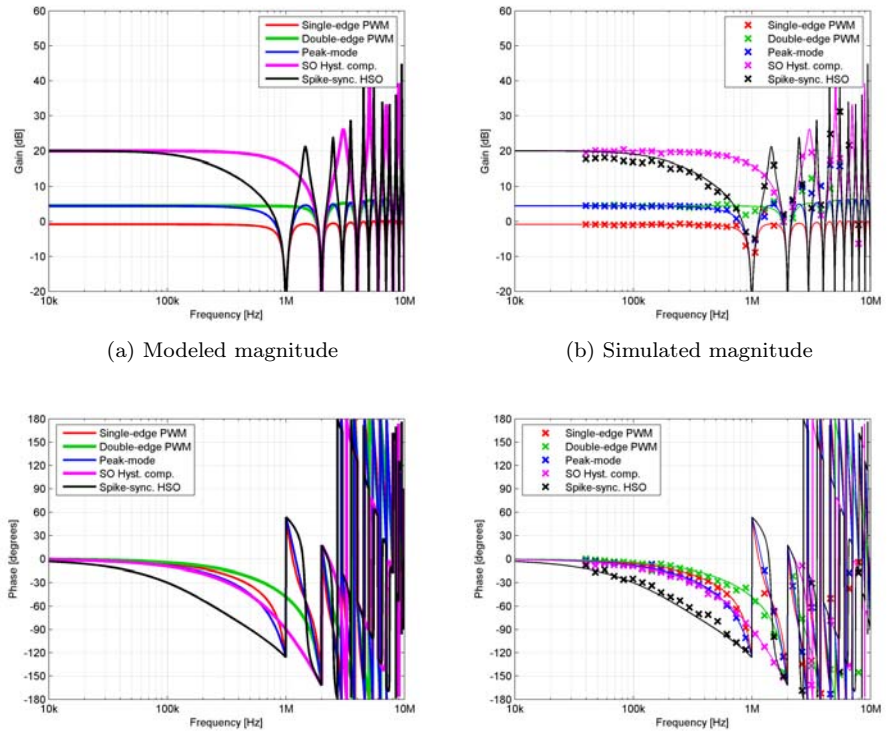
Decision unit	$\lvert\dot{c}_0\rvert$	T_s
PWM - single-edge	$\frac{3V_s}{\tau_{int}}$	$\frac{1}{f_{sw}}$
PWM - dual-edge	$\frac{3V_s}{\tau_{int}}$	$\frac{1}{2f_{sw}}$
Peak-mode	$\frac{2V_s}{\tau_{int}}$	$\frac{1}{f_{sw}}$
Hyst. comp.	$\frac{V_s}{\tau_{int}}$	$\frac{1}{2f_{sw}}$
Spike-sync. HSO	$\frac{V_s}{\tau_{int}}$	$\frac{1}{f_{sw}}$

The comparison results are summed up in a short tabular form in table 9. This very table represents a peak level of insight reached in this Ph.D project - a head-to-head comparison of the ability of various decision units provide loop gain from a given piece of switching hardware. Loop gain in turn directly influences the ability of the control system to reject sinusoidal loop disturbances (or track references). The rejection may be estimated by looking at the crossover frequencies of each configuration and adding the loop filter (viewed in continuous time in this case) magnitude response slope to this. On top of this, the hysteresis-based decision units add extra magnitude response slope at high frequencies due to the single-pole behavior of the hysteretic comparator [44], [45], [48]. *This comparison and the papers published from this project thus prove well beyond reasonable doubt that decision units based on hysteresis (in particular when left free of performance-reducing synchronization pulses) offer the best overall exploitation of the available switching hardware.* Hence, given a single-phase buck power stage and a requirement for maximum-speed control loop dynamics it makes no sense (in the opinion of the author) to use anything else than hysteretic self-oscillating control. *As far as single-vs-double-edge PWM is concerned it is likewise seen that there is no good reason other than laziness to use single-edge PWM over double-edge; bandwidth is higher at an insignificant cost. Peak-mode, often dubbed "fast" in the context of "current-mode control" is seen to have absolutely no advantage over the "voltage mode" methods in contradiction to legacy switch-mode controller design lore*; all of the "fastness" is lost when slope compensation is added to ensure stability over the full duty cycle range. The net result is a loop gain that is exactly the same as for double-edge PWM but with the slight disadvantage that the sampling frequency is halved leading to less loop gain around f_{sw}. It is also seen that the addition of slope compensation is what differentiates peak-mode control from spike-synchronized hysteretic control and that slope compensation evidently reduces loop gain quite dramatically. It should be noted here that the widespread use of current-mode control is of course not without reason. It is very easy to measure the inductor current during the power switch on-period in a forward or flyback converter by using a ground-referred current sensing resistor in series with the switch. The lack of off-period current information is of no consequence since start of the on-period is timed by an external signal. Additionally, in "max 50% duty cycle" topologies (e.g. one/two-switch forward) there is no principal need for slope compensation, effectively making the peak-current mode con-

troller a spike-synchronized hysteretic controller. This leads to a performance advantage over voltage-mode as has been shown. The configuration without slope compensation is likely what earned current-mode the label of "fast".

The most important message of this section remains that the *switch-mode controllers for buck converters can be usefully modeled as LTI systems and decision units, which may in turn be broken down into comparators and more LTI parts.* The input for most decision units should be the same in all cases; a filtered version of the PWM signal where the filter resembles an integrator at high frequencies. It is this viewpoint that gives usefulness to the presented head-to-head comparison of the available decision units. As such, the ever-important and confusing "which control system is the best" discussion may be resolved (at least on an individual, local basis) by deciding, for a given application:

- Which decision unit provides the most suitable set of features?
- Which LTI structure meets performance criteria as well as possible?



(a) Modeled magnitude

(b) Simulated magnitude

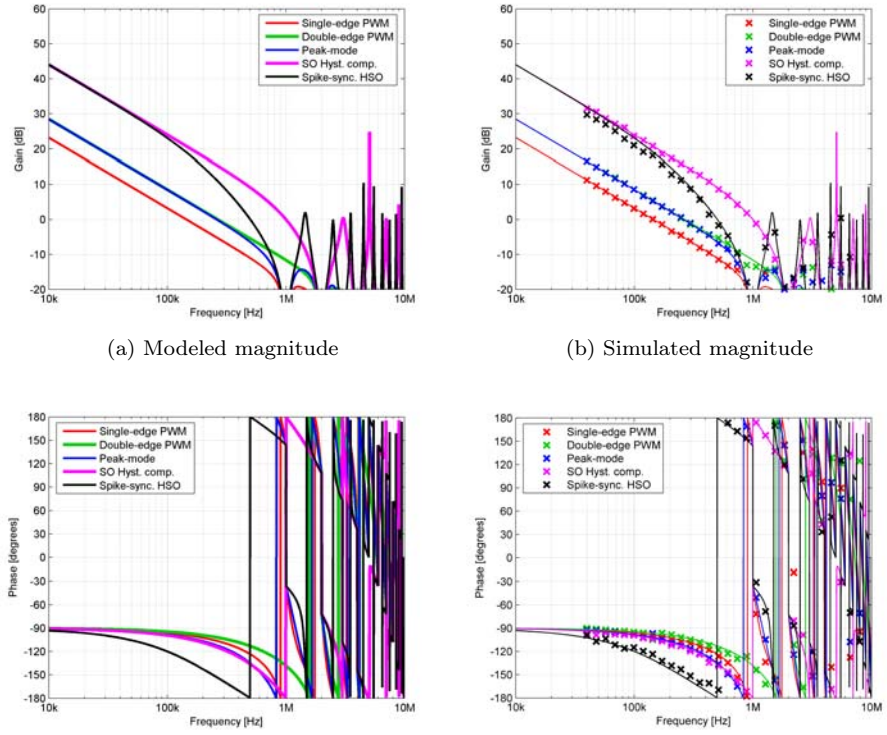
(c) Modeled phase

(d) Simulated phase

Figure 25: Decision unit frequency responses for single-phase buck converter with $f_{sw} = 1MHz$, $t_d = 100ns$ and $\tau_{int} = 1\mu s$ integrator loop filter.

Table 9: Comparison of control loop performance (under given assumptions) with different decision units in a single-phase buck converter switching at frequency f_{sw}.

Decision unit	Crossover freq. f_0	Loop gain at $\frac{1}{2}f_0$
PWM - single-edge	max. $\frac{1}{2\pi}f_{sw}$	6dB
PWM - dual-edge	max. $\frac{1}{\pi}f_{sw}$	6dB
Peak-mode	max. $\frac{1}{\pi}f_{sw}$	6dB
Hyst. comp.	always f_{sw}	6-12dB
Spike-sync. HSO	max. $\frac{1}{2}f_{sw}$	6-12dB



(a) Modeled magnitude

(b) Simulated magnitude

(c) Modeled phase

(d) Simulated phase

Figure 26: Open-loop frequency responses for single-phase buck converter with $f_{sw} = 1MHz$, $t_d = 100ns$ and $\tau_{int} = 1\mu s$ integrator loop filter.

6.6 Single-phase conversions of published controller design

A number of fourth-order filter single-phase buck ET power supply control designs have been published. Given the claims made in the above that the LTI system and the decision unit may be considered separate and independent, then it is natural to present some examples. The LTI system from [38] was therefore

combined with a single-edge PWM decision unit as well as a peak-mode decision unit. Using the above derived maximum loop bandwidths, it follows that for the same crossover frequency in the control loop around the decision units, the single-edge designs has to switch 2π times faster and the peak-mode π times faster than the hysteretic design. This is illstrated in figure 27. Step responses were simulated in Simulink using the same style of approach as used successfully in [36] and results are shown in figure 28. It is evident within reasonable doubt that the PID+PD compensation structure is also usable with other decision units than the hysteretic comparator. Switching frequencies well below those used lead to excessive overshoot since the Bessel optimization routine [38] relies on a notionally infinite small-signal gain of the decision unit. Since the transfer function of the LTI system $G_{ctrl}(s)$ resembles an integrator from an octave or two below the hysteretic controller switching frequency [36] then half the switching frequency also requires half the decision unit gain in all cases. Sooner or later this will of course reduce the decision unit gain to the point where closed-loop poles become sensitive and the Bessel-style pole placement falls apart. An open end exists here since it could be possible to re-place the poles for a lower decision unit gain and get good performance from the lower-bandwidth decision units. Of course, the system would now be fourth-order (since the decision unit gain is no longer infinite and sliding mode therefore does not exist [26]) and as such more difficult to work with.

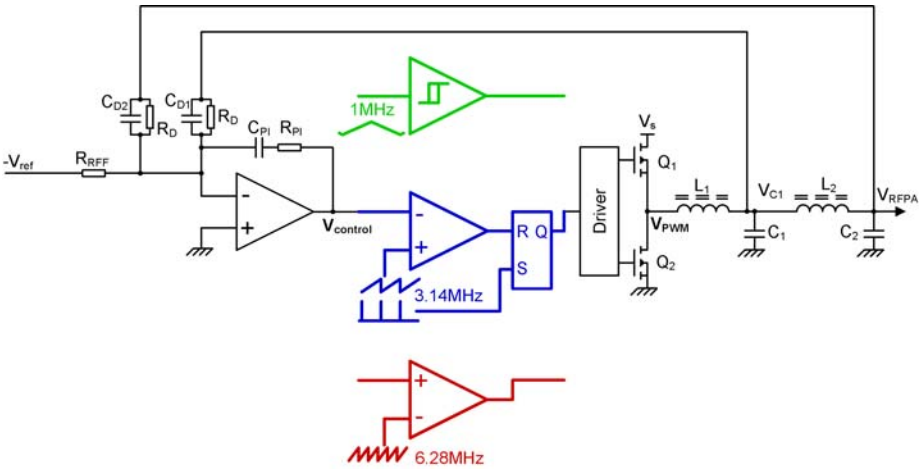


Figure 27: Published [38] control system for fourth-order filtered buck along with decision units that achieve the same 1MHz overall loop bandwidth. Non-colored parts constitute the LTI system.

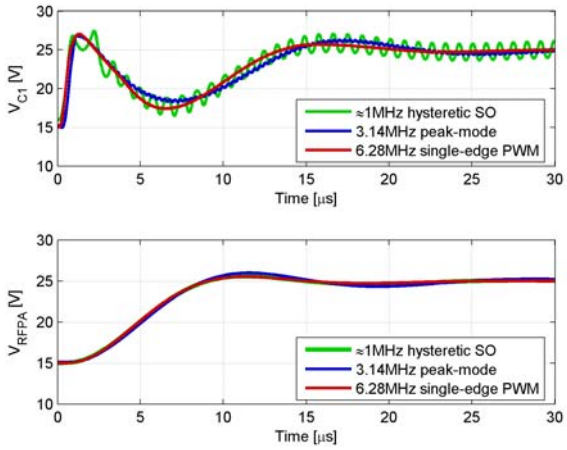


Figure 28: Simulated step responses of systems in figure 27. LTI structure and Bessel response optimization method is usable with multiple decision units.

6.7 Summary and discussion

This section has shown that a very diverse set of buck converter control systems may be represented and compared using only two variables - the LTI system and the decision unit. For the special case of the single-phase buck converter, as studied in all publications from this Ph.D project, it has been shown that using a hysteretic comparator for the decision unit can lead to performance advantages. The drawbacks of hysteretic self-oscillating control systems have been studied in published material [39], these revolve around the limited freedom of choice with regards to switching frequency. However, for the case where the desired switching frequency can be obtained with any decision unit, the hysteretic self-oscillating control solution will outperform all others in terms of loop gain. For the feedback structure (LTI system), a large task that remains incomplete is the identification of the optimal LTI structure. This is the solution that minimizes sensitivity to external disturbances while providing the desired response to the injected output voltage reference. It is likely that the optimal solution is found outside of the "current mode"-type structures since these lead to higher output impedances [47]. Using load current feed-forward techniques, this disadvantage is negated, and performance will be similar to that of voltage-feedback structures [47]. The optimal solution will probably also rely on placing maximum loop gain in the feedback loop that governs the output node of the ET power supply, since it is the effect of load current changes that needs to be minimized. Note that the sliding mode control theory notion of "invariance to disturbances" [26] is merely [47] a reflection of assigning infinite small-signal gain to the hysteretic comparator, a condition that will never be satisfied for a real-world implementation. Practically, the gap between theory and reality can be viewed as the simple result of sliding mode control theory not evolving specifically to solve switch-mode amplifier-type control problems.

Although short of being provably *optimal*, a few candidates for *good* LTI structure solutions have been published [36], [37], [38], [39]. Non-published (in academic context) candidates include those described in filed patent applications

[57] and [58] which are included as appendices.

7 The RFPA and ET power supply boundary

In the ideal case, an ET power supply would deliver exactly the voltage requested regardless of loading, and the RFPA would be unaffected by the applied supply voltage as long as clipping was avoided. In the real world, this is not the case, and this section investigates the interactions between the RFPA and the ET power supply on a system level. It will be shown that the following non-ideal properties of the ET power supply and the RFPA need to be considered in the TETRA/TEDS RFPA system:

- RFPA gain varies with supply voltage.
- ET power supply produces unwanted frequency components (switching ripple).
- RFPA demands a non-constant supply current.
- ET power supply has non-zero output impedance.

In practice, the following problems have been observed in the TETRA/TEDS application:

- ET power supply ripple intermodulates with RF carrier causing unwanted frequency components in the RFPA output.
- RFPA linearity decreases due to the continuous variations in supply voltage.
- ET power supply output voltage deviates from the desired value due to variations in load current.

The overall (somewhat empirical) system model in figure 29 has sufficient detail to provide a basis for discussion. The modeling of RFPA power supply intermodulation (PSIM) necessitates the use of a block capable of providing frequency translation, i.e. a mixer, as discussed in [33]. RFPA supply current is generally a function of the output of the RFPA (practically the envelope of this) and the applied supply voltage. This has been modeled by the "supply current function" controlling a current sink. Note that all "normal" distortion generated the RFPA, as often shown in AM/AM and AM/PM graphs has been neglected in this model; given a zero-impedance DC supply the shown RFPA sub-model is perfectly linear.

7.1 Ripple intermodulation

An example of the measurement data that originally gave rise to presented RFPA model is shown in figure 30. It was subsequently found experimentally that the amplitude of the PSIM products were largely frequency and amplitude independent. This property allows the mechanism to be reasonably precisely described using only mixer, gain and sum/difference blocks as done in figure 29.

Constant K_{PSIM} is in the model used to describe the magnitude of the intermodulation spurs and can be easily found from measurements such as the one shown in 30. The formal analysis of the RFPA output can be found in [33]. Of main interest is that the RFPA inputs given in equations (24) and (25) lead

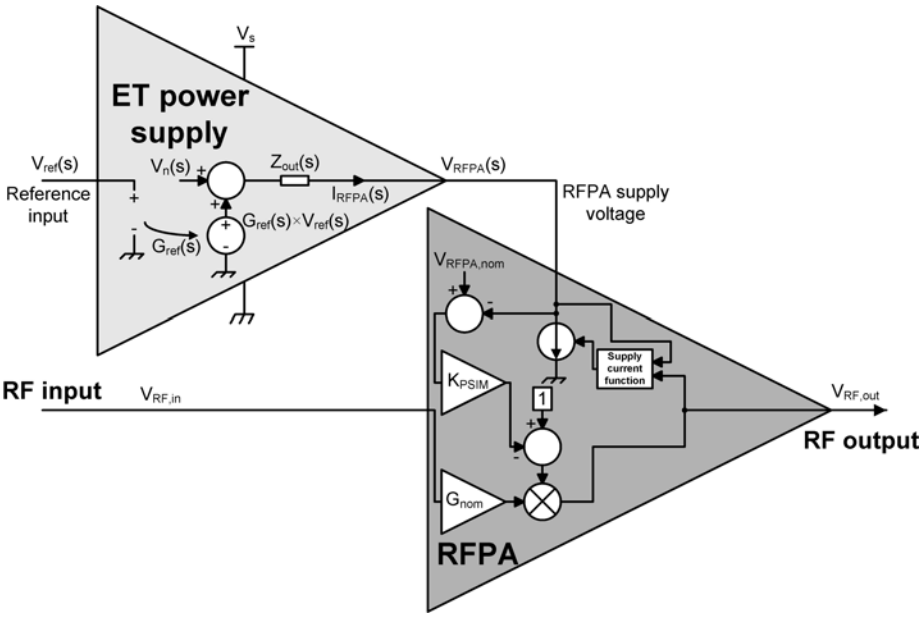


Figure 29: System model for analysis of the ET power supply and RFPA boundary.

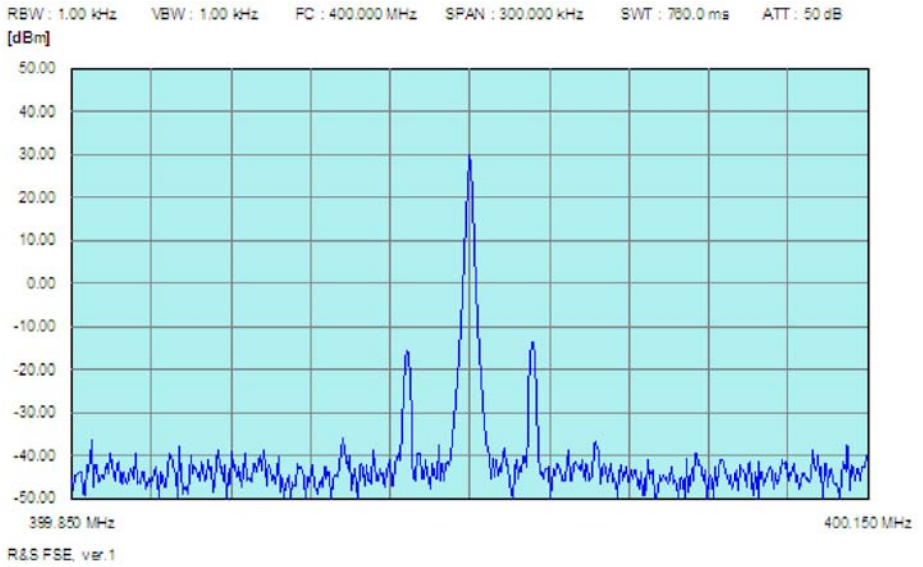


Figure 30: Class-A/B RFPA output with CW input and 20VDC supply with 2Vpp 25kHz sine wave superimposed. RFPA is not clipping but there is still significant PSIM spurs at +/-25kHz.

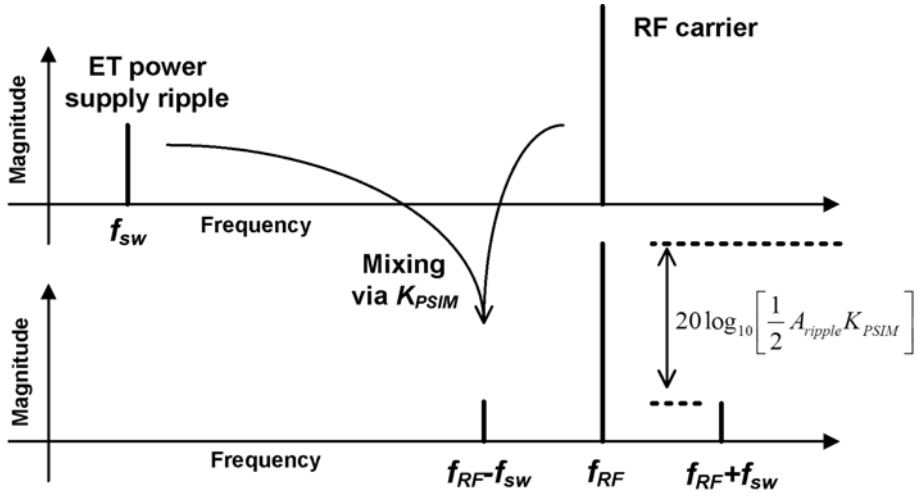


Figure 31: Frequency domain illustration of the power supply intermodulation problem.

to the RFPA output given by equation (26). Figure 31 shows the conceptual view of PSIM adopted.

$$V_{RFPA} = V_{RFPA,nom} + A_{ripple} \cdot \cos\left(2\pi f_{sw} t\right) \tag{24}$$

$$V_{RF,in} = A_{RF} \cdot \cos\left(2\pi f_{RF} t\right) \tag{25}$$

$$\begin{aligned} V_{out,RF} = A_{RF} \cdot G_{nom} \cdot \cos\left(2\pi f_{RF} t\right) + \\ \frac{A_{ripple}}{2V_{RFPA,nom}} \cdot \cos\left(2\pi \left[f_{RF} + f_{sw}\right] t\right) + \\ \frac{A_{ripple}}{2V_{RFPA,nom}} \cdot \cos\left(2\pi \left[f_{RF} - f_{sw}\right] t\right) \end{aligned} \tag{26}$$

Using the presented model and analysis (which is strictly only a shell for defining K_{PSIM}), a representative class-A/B RFPA was characterized for K_{PSIM} at different DC supply levels. Results are shown in figure 32 and are taken from [33]. Different frequencies and amplitudes of supply voltage AC signal was used to verify the frequency and amplitude indifference of the PSIM mechanism. For low frequencies (1kHz/10kHz), an ET power supply was supplied with an AC/DC reference to provide the AC/DC supply rail for the RFPA. For high frequencies, a DC reference was used for the ET power supply, and its actual output ripple frequency and amplitude recorded for use in K_{PSIM} calculations. Variation of switching frequency with output voltage was inevitable since the ET power supply used self-oscillating control. Also shown in the figure is the K_{PSIM} that could be expected from an RFPA driven in EER mode, i.e. full clipping. It can be shown [33] that any RFPA in an EER system has a K_{PSIM} of $1/V_{RFPA,nom}$ since the RFPA in this case is a perfect multiplier from its

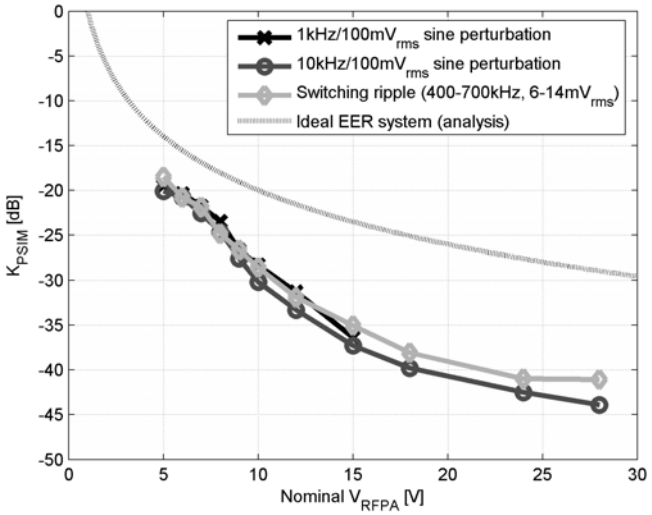


Figure 32: Power supply intermodulation coefficients K_{PSIM} measured on a Motorola 200W (CW) 400MHz class-A/B TETRA base station RFPA. Susceptibility to supply ripple varies non-linearly with supply voltage.

supply input to its RF output. One interesting observation to make from 32 is that the ET system RFPA is relatively sensitive to supply noise/ripple in the sense that it only has 5-15dB better rejection than the lowest possible rejection (the EER case.) In the ideal world, the ET system linear RFPA would show a K_{PSIM} of zero as long as clipping was avoided.

With the empirically determined RFPA PSIM behavior packaged into a single constant K_{PSIM} using superficial analysis, this can now form the basis of a more rigid, design-oriented analysis for determining the amount of ripple allowed on the output of the ET powers supply.

Starting with the ripple IM spurs (in case of CW output from the RFPA) or components (with an actual "box-spectrum" TETRA or TEDS) carrier, these have the relative power of:

$$P_{PSIM,dBc} = 20 \cdot \log_{10}\left(\frac{1}{2} A_{ripple} K_{PSIM}\right) \tag{27}$$

i.e. for $K_{PSIM} = 0.1$ and $A_{ripple} = 0.1V$ ripple IM products will each be of -40dBm power for a 0dBm CW RFPA output. With a 40dBm TETRA output, ripple IM products would each have a power of 0dBm.

In practice, ripple IM products are likely to appear in frequency areas where the RFPA output is restricted by wideband noise (WBN) specifications. For *both* TETRA and all TEDS carriers, WBN is to be measured looking through a TETRA receiver filter [49], i.e. the 18kHz root-raised cosine (RRC) filter specified in [49]. Assuming the ET supply ripple to sinusoidal (and as such to have a constant frequency), then the ripple IM products will have the same shape as the carrier due to the nature of convolution. In particular, ripple IM products will have the same bandwidth as the carrier. Therefore, one must correct for the potential difference in "noise bandwidth" (the 18kHz set by the TETRA

receiver RRC filter) and the "signal bandwidth", i.e. the carrier bandwidth that could be 18, 50, 100 or 150kHz in a TEDS transmitter. All this means that the power of the ripple IM products seen in the measurement bandwidth is reduced for carrier bandwidths above 18kHz, so that the WBN level measured is:

$$P_{WBN,dBc} = P_{PSIM,dBc} - 20 \cdot \log_{10}\left(\frac{BW_{carrier}}{BW_{WBN}}\right) \tag{28}$$

Note that in the case of multiple carriers (e.g. two TETRA carriers) $BW_{carrier}$ in this case has to be the *per-carrier* bandwidth since this is the bandwidth for which carrier power is defined and measured.

Solving for A_{ripple} leads to the useful result of:

$$A_{ripple} < \frac{2 \cdot 10^{\frac{P_{WBN}(f_{ripple})}{20}} \cdot \frac{BW_{carrier}}{BW_{WBN}}}{\max\{K_{PSIM}\}_{V_{RFPA}}} \tag{29}$$

where $\max\{K_{PSIM}\}_{V_{RFPA}}$ is the maximum value of K_{PSIM} over the RFPA supply voltage range and $P_{WBN}(f_{ripple})$ is the WBN limit at the considered ET power supply output ripple frequency f_{sw}. For the one-phase buck ET power supplies used in this project, f_{ripple} is the same as the switching frequency f_{sw}. For the 50kHz TEDS case, key numbers in the ET power supply ripple specification derivation are shown in table 10. For standard TETRA, 150kHz TEDS and dual-carrier TETRA cases, the numbers in table 11 are given as reasonable but non-verified guesses. It was assumed that the same 1MHz switching ET power supply technology that works for 50kHz TEDS could be applied to TETRA but that four 1MHz buck phases would be required for 150kHz TEDS. For dual-carrier TETRA where the carriers could be up to 5MHz apart, 500kHz separation (leading to an overall carrier bandwidth of 500kHz) was assumed along with an 8-phase 2MHz switching buck ET power supply topology which should be capable of 500kHz envelope tracking. The outlook in table 11 suggests that regular TETRA and TEDS envelope tracking is ripple-wise well within reach using switching technology but that multi-carrier TETRA could be quite difficult due to the extremely low ripple required to comply with the -100dBc wideband noise specification. In this case, switching (pun somewhat intended) to the combination of linear and switch-mode power stages as shown in [7] [28] would perhaps be the more sensible option.

For the TETRA case, the ripple specification required for the ET power supply in the ET supply case is compared to that for the EER case in table 12. Although numbers are somewhat approximate, it is clear that the EER scheme leads to a much more difficult ET power supply design job, especially considering that bandwidth has to be significantly higher than in the ET case.

Rounding off this ripple IM study, it is only fair to say that results are heavily influenced by the RFPA that was available for measurements. Other RFPAs may behave differently, and deeper analysis is required for a full overview of the problem. An example of such analysis is [21] which still relies on accurate RFPA device models (BSIM) in addition to intimidating sounding mathematics (Volterra series) for computing the RFPA input/output relation. This section still has value to offer though; it shows a pragmatic approach for using simple low-frequency measurements for obtaining ET power supply ripple specifications in the early design phase. The accuracy of the method is verified in [33].

Table 10: ET power supply ripple specification derivation in the 50kHz TEDS application

Parameter	Symbol	Value
Carrier bandwidth	$BW_{carrier}$	50kHz
Wideband noise measurement bandwidth	BW_{WBN}	18kHz
ET power supply ripple frequency	f_{ripple}	1MHz
WBN specification at ripple frequency	$P_{WBN}\,(f_{sw})$	-80dBc
RFPA supply voltage range	V_{RFPA}	5-28V
Maximum PSIM coefficient	$\max\{K_{PSIM}\}_{V_{RFPA}}$	-18.5dB (=0.12)
Maximum ET power supply ripple amplitude	A_{ripple}	4.6mV

Table 11: ET power supply ripple specification derivation in various TETRA/TEDS base station applications.

Parameter	Standard TETRA	50kHz TEDS	150kHz TEDS	2-carrier TETRA
Carrier bandwidth	18kHz	50kHz	150kHz	2·18kHz
Wideband noise measurement bandwidth	18kHz	18kHz	18kHz	18kHz
ET power supply ripple frequency	1MHz	1MHz	4MHz	16MHz
WBN specification at ripple frequency	-90dBc	-80dBc	-80dBc	-100dBc
RFPA supply voltage range	15-28V	5-28V	5-28V	5-28V
Maximum PSIM coefficient	-35dB	-18.5dB	-18.5dB	-18.5dB
Maximum ET power supply ripple amplitude	3.5mV	4.6mV	13.9mV	0.36mV

Table 12: ET power supply ripple specifications with ET and EER RFPA system schemes. Full-power operation assumed.

Parameter	TETRA - ET	TETRA - EER
RFPA supply voltage range	15-28V	10-28V
Maximum PSIM coefficient	-35dB	-20dB
Maximum ET power supply ripple amplitude	3.5mV	0.62mV

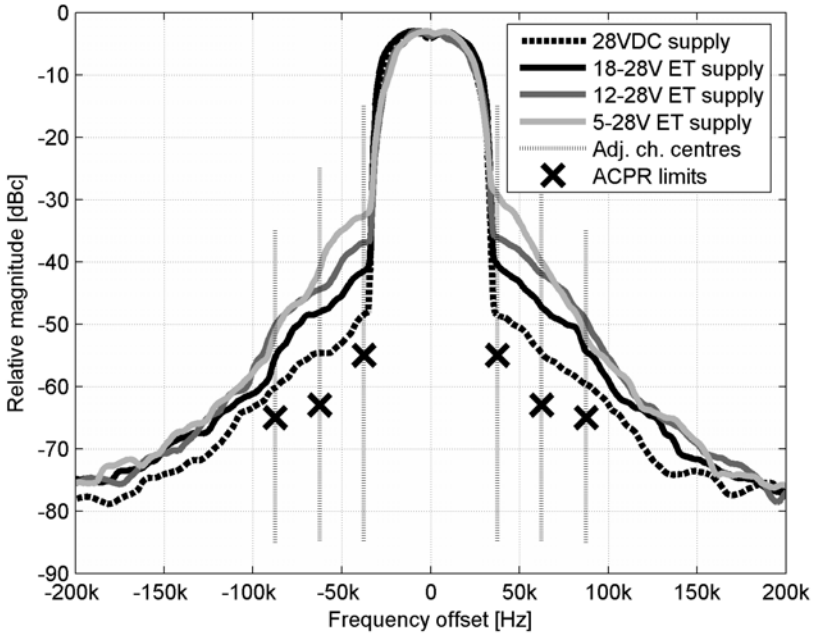


Figure 33: TETRA-spec RRC filtered RFPA output spectra with 44dBm 50kHz TEDS carrier with supply schemes for ACPRC evaluation. Tracking depth has significant effect on ACPRs.

7.2 RFPA distortion increase from ET

Increases in RFPA open-loop distortion with application of the ET supply scheme were often observed in the experimental work performed in this project. A typical example is shown in 33. Given that the reader trusts that ET timing was correctly aligned for these measurements, it is evident that envelope tracking decreases the RFPA linearity. Proper analysis of this would probably require device physics insight beyond the scope of this Ph.D project. A few hints are available though:

- It is given that the RFPA gain and/or phase varies with supply voltage. Otherwise there would be no PSIM. Gain variation is non-linear since K_{PSIM} is not inversely proportional to supply voltage.
- It is well known that MOSFETs and other semiconductors exhibit parasitic capacitances that vary non-linearly with voltage. Variation in C_{DS} affects the matching of the RF power device and hence the overall gain/phase characteristics of the amplifier stage.
- In particular, supply variation has been shown to cause phase distortion in linear class-A/B RFPAs [28].

The consequences of an increase in RFPA distortion due to the use of envelope tracking are not so speculative as the explanation. If we assume that

Table 13: Overview of the 50kHz TEDS ACPR problem when considering 2nd-order CFB linearization with bandwidth well above 50kHz. ACPR3 is the most difficult in all cases, with or without ET.

Parameter	ACPR1	ACPR2	ACPR3
Specification	-55dBc	-63dBc	-65dBc
Frequency (+/-)	37.5kHz	62.5kHz	87.5kHz
Relative octaves	-1.22	-0.49	0 (ref.)
Normalized improvement with 2nd order CFB	14.64	5.88dB	0dB
Meas ACPR - 28VDC	-48dBc	-55dBc	-60dBc
Improvement needed	7dB	8dB	5dB
If CFB applied (norm.)	-7.6	2.1dB	5dB
Meas ACPR - 5-28V ET	-29dBc	-40dBc	-51dBc
Improvement needed	26dB	23dB	19dB
If CFB applied (norm.)	11.4dB	17.1dB	19dB

CFB linearization is used and that loop bandwidth and design allows second-order loop gain slope below 100kHz then it is possible to initially identity the adjacent channel affected the most by envelope tracking by inspection of the slope of the distortion "skirt" in figure 33. In the worst case (5-28V ET) the distortion skirt has a slope of around 18dB/octave, i.e. a third-order slope. This means that second-order CFB can be expected to flatten the skirt slope to first-order. As such, ACPR1 is degraded the most by ET since the distortion skirt steepness increases with the ET depth. However, the ACPR specification varies non-linearly with frequency, hence the tabular presentation of the problem in 13. Since any second-order CFB will provide the same relative distortion reduction at the three ACPR frequencies, the normalized closed-loop ACPRs can be compared to see which one is the highest. An approximation made is that ACPR is improved by 1/(1+[loop gain]) at the ACPR measurement frequency, which is the same as approximating the loop gain to be constant over the ACPR measurement band of 18kHz.

In all cases ACPR3 is highest after the application of second-order CFB, so it is now possible to say with confidence that the RFPA is effectively made 10dB less linear by 5-28V ET. Again given 12dB/ocatave loop gain slope this means that CFB bandwidth has to be almost doubled, not in all cases a desirable requirement since CFB loops are effectively bandwidth limited by loop delay [1] [23] [33] and in some cases demodulator noise [33]. Happily, in the 50kHz TEDS case at 400MHz, sufficient CFB bandwidth is possible [33].

In practice, a 400MHz CFB system can be implemented with more than 1MHz bandwidth, so that second-order loop gain slope is easily achieved below 100kHz. Results are shown in figure 34. Due to limited linearity in the I/Q demodulator in the CFB loop (or possibly measurement equipment) the distortion skirts in all cases end up compressed into the -70-80dBc area. This proves beyond doubt that CFB is sufficient for mitigating the linearity degradation associated with ET for 50kHz TEDS. However, going to just 100kHz TEDS, CFB bandwidth must be doubled for the same closed-loop performance to be obtained. Although maybe possible, the bandwidth limitation of CFB will begin to limit the design space in this case since 2MHz CFB bandwidth at

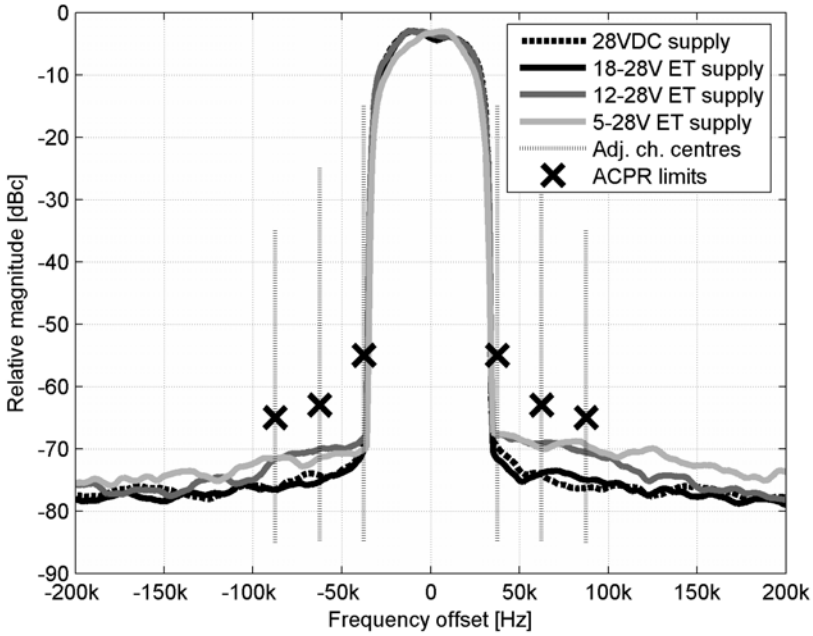


Figure 34: 44dBm 50kHz TEDS ACPRs with 1MHz CFB added.

400MHz (0.5% fractional bandwidth) is on the borderline of difficult [50] as also concluded in [33].

7.3 ET power supply output impedance

An issue not given much attention in prior art, ET power supply output impedance will here be shown to be worthy of at least some consideration. For analysis, the RFPA is assumed to behave as a variable current sink with supply current being a function of the instantaneous output level. Assuming that the RFPA supply current is proportional to output amplitude then we have:

$$I_{RFPA}(t) = c_{scale} \cdot env\{V_{out,RF}(t)\} \tag{30}$$

where the *env* operator refers to the envelope of the signal and c_{scale} is a scaling factor determined by the RFPA design.

Moving into the frequency domain for direct compatibility with the linear, transfer function based ET power supply description in figure 29 then the ET power supply output voltage will be given by:

$$V_{RFPA}(s) = V_{ref}(s) \cdot G_{ref}(s) - I_{RFPA}(s) \cdot Z_{out}(s) \tag{31}$$

where $V_{ref}(s)$ is the reference voltage for, $G_{ref}(s)$ the reference-to-output transfer function of and $Z_{out}(s)$ the output impedance of the ET power supply. Assuming that $V_{ref}(s) \cdot G_{ref}(s)$ is the desired ET power supply output, then the output impedance has introduced the following error on the output voltage:

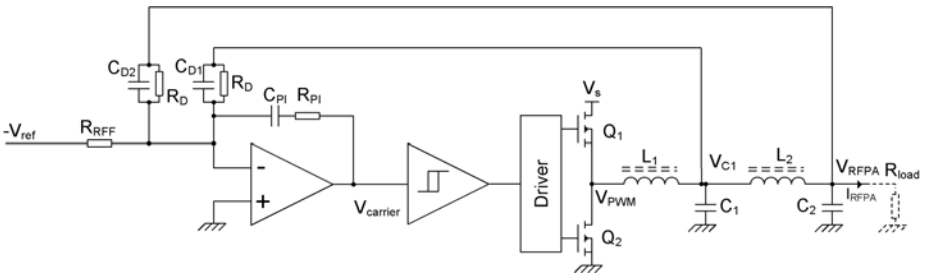


Figure 35: Practical ET power supply example for 50kHz TEDS. Output impedance is approximately $s \cdot 0.5L_2$.

$$\Delta V_{RFPA}(s) = -I_{RFPA}(s) \cdot Z_{out}(s) \tag{32}$$

Going back into the time domain, the error is:

$$\Delta V_{RFPA}(t) = conv\{I_{RFPA}(t), Z_{out}(t)\} \tag{33}$$

where $conv\{\}$ refers to the convolution operator and $Z_{out}(t)$ is the impulse response of the output impedance transfer function. Since $\Delta V_{RFPA}(t)$ is undesirable in that it could lead to clipping in the RFPA, it is of value to be able to estimate its value in the actual application. The problem here is just to identify $I_{RFPA}(t)$ or a worst-case representation of this as well as $Z_{out}(t)$ or a good enough approximation.

One place to start when looking for the worst-case load current is in the expected ET power supply output impedance. Since both the load current and the output impedance are non-scalar quantities, finding the maximum product requires some assumptions. For the ET power supply output filter, it is reasonable to assume (as done in the power topology comparison) that the lowest corner frequency equals the tracking bandwidth which again equals the carrier bandwidth. This means that the open-loop output impedance will be inductive (increasing linearly with frequency) from DC (neglecting various parasitic resistances) to the bandwidth. Adding to this the fact that most feedback system exhibit loop gains that decrease with frequency, it is expectable that ET power supply output impedance will increase with frequency below the tracking bandwidth. As such, it is the fast variations in load current that pose the biggest problem.

As an output impedance example, the ET power supply implementation in figure 35 exhibits an output impedance of [38]:

$$Z_{out}(s) = \frac{sL_2}{s^2 L_2 C_2 + s\left(\frac{L_2}{R_{load}}\right) + 1 + \frac{1+sR_D C_{D2}}{1+sR_D C_{D1}}} \tag{34}$$

which can be approximated as

$$Z_{out}(s) = \frac{sL_2}{2} \tag{35}$$

The ET power supply thus resembles an ideal voltage source with an inductor of $0.5L_2$ in series with its output. Having a model this simple allows the worst-

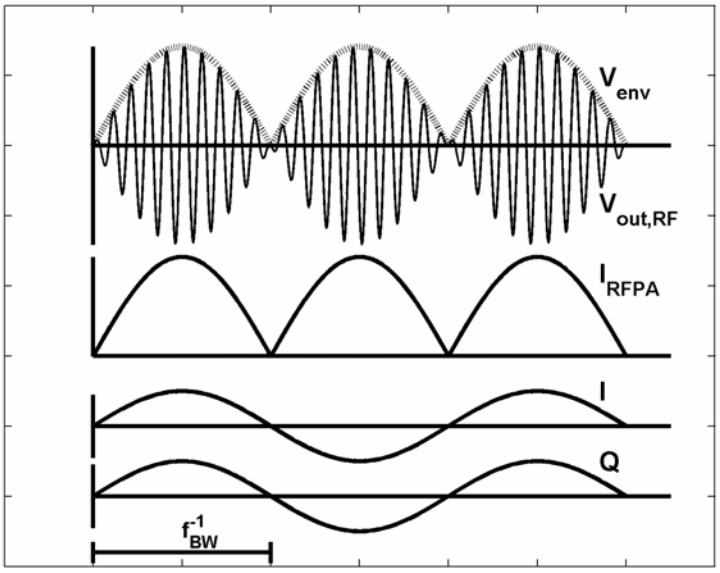


Figure 36: Vector modulated signal that leads to maximum RFPA load current dI/dt; a maximum-bandwidth two-tone signal.

case load current to be determined; since $V = L\frac{dI}{dt}$ for an inductor, then it is the worst-case load current *slope* that is of interest.

Since the RFPA load current was approximated to be proportional to the RFPA output envelope, the maximum load current slope will occur with the maximum output envelope slope. A vector modulated signal generally has the envelope of:

$$E(t) = \sqrt{I^2(t) + Q^2(t)} \tag{36}$$

therefore the envelope slope is given by

$$\frac{dE(t)}{dt} = \frac{2I(t) \cdot \frac{dI(t)}{dt} + 2Q(t) \cdot \frac{dQ(t)}{dt}}{2\sqrt{I^2(t) + Q^2(t)}} \tag{37}$$

Since the I and Q signals are generally filtered by steep low-pass filters (RRC) then the maximum I/Q vector slope will result when the un-filtered I/Q vector is a square pulse train with a frequency just below the filter cut-off frequency. In this case, an ideal low-pass filter will turn the pulse train into a sine wave, so the worst-case I/Q vector is one where both I and Q are maximum-amplitude sine waves with a frequency that equals half the carrier bandwidth. For 50kHz TEDS, the worst-case RFPA load current dI/dt thus occurs when I and Q are 25kHz sine waves and the RFPA reaches its rated peak output power. Waveforms are illustrated in figure 36.

The two-tone signal has a normalized envelope of:

$$E(t) = |\cos(\pi f_{BW} t)| \tag{38}$$

Given that the RFPA has a peak supply current of I_{peak} then the worst-case RFPA supply current waveforms is:

$$I_{RFPA}(t) = I_{peak} \cdot |\cos(\pi f_{BW} t)| \tag{39}$$

The maximum slope of this waveform is:

$$\max\left\{\frac{dI_{RFPA}(t)}{dt}\right\} = I_{peak} \cdot \pi \cdot f_{BW} \tag{40}$$

Since most carriers are in fact not two-tone but rather have their spectral content spread evenly within the bandwidth, the two-tone case might be somewhat pessimistic. In order to provide a practical angle on the dI/dt computation, the slope of the envelope of an actual 50kHz TEDS I/Q vector was calculated and normalized to the found worst-case value. Practically, the I/Q vector was normalized for a peak envelope of 1, so that the corresponding two-tone maximum envelope slope is $\pi \cdot 50kHz$. The distribution of the normalized envelope is shown in figure 37. It is evident that the TEDS carrier almost never exhibits more than half of the maximum two-tone envelope, so a practical worst-case RFPA load current dI/dt would be:

$$\max\left\{\frac{dI_{RFPA}(t)}{dt}\right\} \approx \frac{I_{peak} \cdot \pi \cdot f_{BW}}{2} \tag{41}$$

With a trustworthy estimate of the maximum RFPA load current dI/dt at hand, it is now easy to compute the maximum ET power supply output voltage deviation by combining equations (35) and (41) with the inductor current/voltage relation, leading to:

$$\max\{\Delta V_{RFPA}(t)\} \approx \frac{I_{peak} \cdot \pi \cdot f_{BW} \cdot L_2}{4} \tag{42}$$

In 50kHz TEDS application, given 14A peak RFPA load current and an ET power supply with $L_2 = 2\mu H$, the maximum expected output voltage deviation is around 1.1V. shows a set of measured V_{RFPA} and I_{RFPA} waveforms along with the simulated responses of the ET power supply (with $L_2 = 2\mu H$) to these. The accurate output impedance model of equation (34) was used for computation of the load current effect on the ET power supply output voltage. Looking at figure 38, 1.1V deviation is a very reasonable estimate. Another observation worth pointing out is that the RFPA load current displays no visible dependence on the applied supply voltage, confirming that the current sink model is reasonable. Note that the figure was taken from [38] where "V_{out}" is the same as the "V_{RFPA}" defined in this report.

Summing up, it has now been shown that ET power supply output impedance can have practical influence on the ET power supply output but that the effect can be estimated with good accuracy and therefore controlled by proper design of the ET power supply. A fully sufficient design procedure is to design the ET power supply for driving an infinite load impedance (such as a current sink) but taking into account the deviations in output voltage caused by the variation in load current.

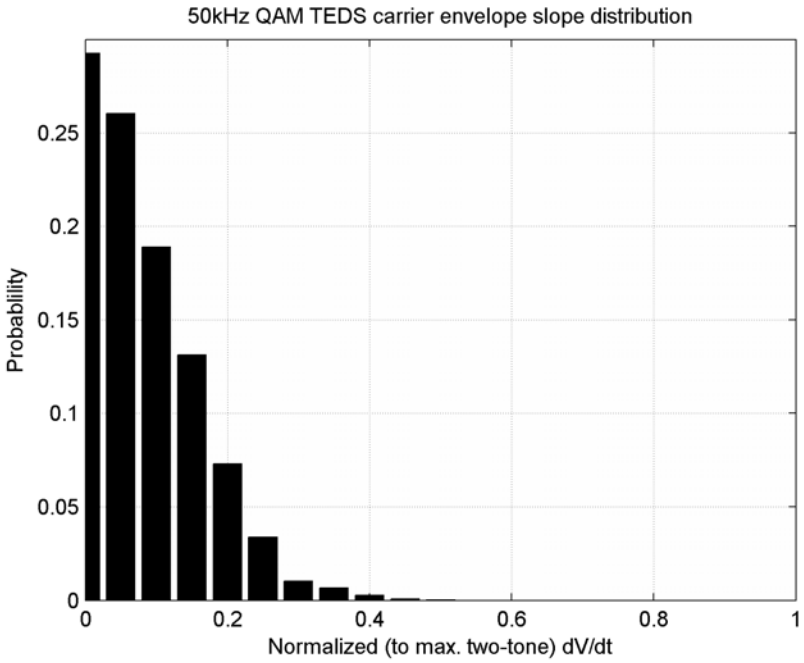


Figure 37: Distribution of 50kHz TEDS carrier envelope slope normalized to worst-case two-tone envelope slope.

7.4 Summary

This section has shown how the non-ideal characteristics of the ET power supply and the RFPA interact to create potential problems. Noise (ripple) caused by the switch-mode power conversion in the ET power supply leads to extra unwanted frequency components on the RFPA output through the process dubbed "Power Supply InterModulation", abbreviated PSIM. An empirical method for practically dealing with this issue was proposed, allowing a ripple specification for the ET power supply to be derived at an early system design stage. The effect of using a variable supply rail on the RFPA linearity was also practically examined and found to be substantially detrimental; modulating the RFPA supply rail between 5 and 28V lead to a 14dB degradation of ACPR3 for a 50kHz TEDS carrier at full output level. The reduction in RFPA linearity was nonetheless found to be possible to counteract through the use of suitable amounts of negative feedback provided by a CFB system. Output impedance of the ET power supply, otherwise a rarely considered topic in prior art, was shown to be a parameter of considerable importance since it governs the effect of RFPA supply current variations on the ET power supply output voltage. A relatively simple method was proposed to allow early specification of the ET power supply output impedance from data on the maximum RFPA supply current and the RF carrier bandwidth.

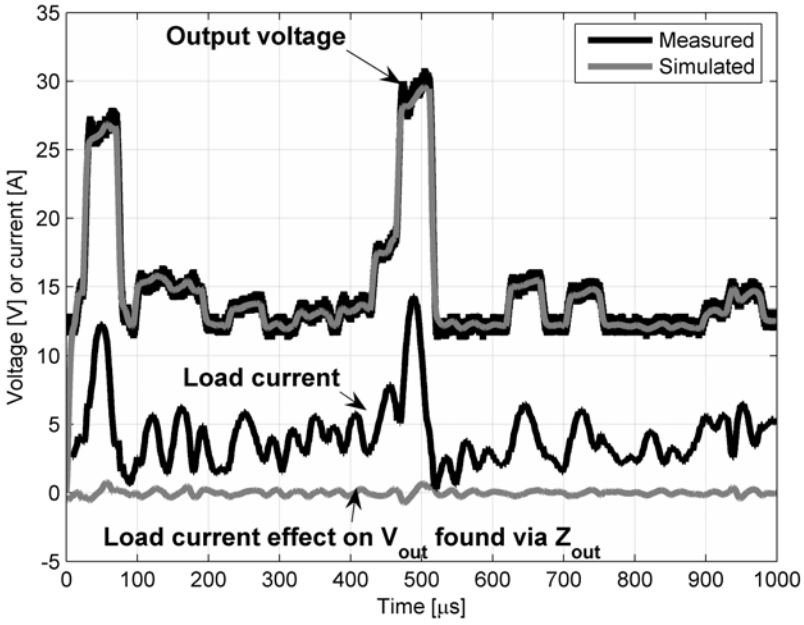


Figure 38: Simulation of ET power supply output response to measured reference and load current waveforms. Non-zero output impedance accounts for sub-optimal tracking. Maximum deviation is around 1V.

8 High-performance Cartesian Feedback

An often-recurring question during the work with the presented Ph.D project was "how much bandwidth and loop gain can we get from the Cartesian feedback (CFB) loop?". This is because the amount of loop gain available for ironing out RFPA non-idealities greatly affects the span of the transmitter design solution space:

- Possible carrier bandwidth - large CFB bandwidth allows large carrier bandwidths.
- RFPA linearity requirement - available output power from a given RFPA, linearity-vs-efficiency trade-off.
- ET power supply ripple spec - if CFB bandwidth exceeds ripple frequency then ripple IM products are reduced.
- Envelope tracking depth - deeper envelope tracking reduces RFPA linearity and ultimately leads to out-of-spec. ACPRs.

It has been shown [33] that a commercially available Cartesian feedback IC and a production model class-A/B RFPA can be combined to form a usable transmitter for TETRA and TEDS carriers with up to 50kHz bandwidth. In this case, Cartesian feedback loop was more than ample at 1MHz (20 times the carrier bandwidth) but stretched close to the limit set by group delays in the RF path and I/Q modulator and demodulator blocks. This section provides an educated guess to the practical limit of Cartesian feedback at 400MHz driven by the much more challenging application of amplifying a 500kHz bandwidth two-carrier TETRA signal. Although no workable solution is offered, pointers on what system parameters to improve are provided.

8.1 CFB bandwidth and group delay

Assuming that the CFB system has loop filters with the ubiquitous integrator-like transfer characteristics at high frequencies (that it, around the loop crossover frequency), then it is straightforwardly obvious than any delay in the loop simply erodes away some of the inherent 90° phase margin. As pointed out in [33], if we specify a phase margin of ϕ_m then given a delay of t_{GD} the crossover frequency is limited to:

$$f_{0,max} = \frac{90° - \phi_m}{360° \cdot t_{GD}} \tag{43}$$

$$f_{0,SO} = \frac{1}{4t_{GD}} \tag{44}$$

As a realistic (on the optimistic side) numerical example, if we could have 20ns of RF path delay then it would principally be possible to realize a reasonably stable 6.25MHz CFB system. Selling out on phase margin, it is principally possible to approach the double of this, i.e. 12.5MHz if large peaks [33] in wideband noise due to inadequate phase margin can be tolerated. This might be the case in a 400MHz TETRA base station where the RFPA output is filtered by an ultra-steep bandpass filter as part of the duplexing scheme that allows the same antenna to be used for both transmission and reception.

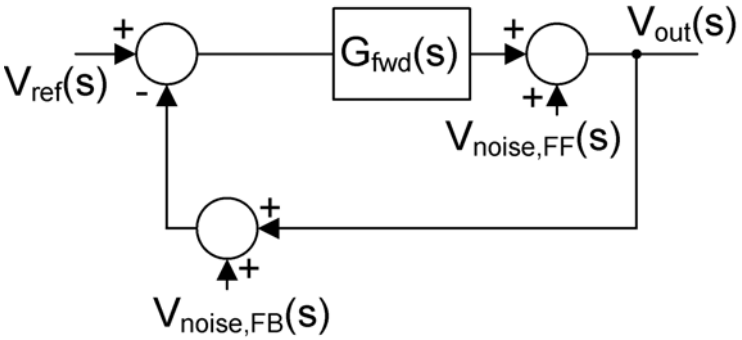


Figure 39: Unity-feedback closed-loop system for simple noise effect analysis.

8.2 Noise considerations

In the TETRA application, relatively little noise is allowable at MHz-size offsets from the transmitted carrier. This means that a very wide-band CFB system needs to have a low-noise feedback path. To illustrate this, consider the system of figure 39, which could very well be extended to model the I and Q feedback loops in a CFB system. It is found that the output $V_{out}(s)$ is given by:

$$\begin{aligned} V_{out}(s) = & \frac{G_{fwd}(s)}{1+G_{fwd}(s)} \cdot V_{ref}(s) \\ & + \frac{1}{1+G_{fwd}(s)} \cdot V_{noise,FF}(s) \\ & + \frac{G_{fwd}(s)}{1+G_{fwd}(s)} \cdot V_{noise,FB}(s) \end{aligned} \tag{45}$$

In all simplicity we hereby see that any noise added by the feedback path, when referred to the point where the reference is added, is indistinguishable from the reference signal. As such, given that the loop tries to make the feedback signal equal to the reference signal, the noise floor of the closed-loop system cannot be lower than the signal-to-noise ratio offered by any blocks in the feedback part of the control loop.

In a CFB system, the feedback path comprises some attenuation of the RFPA output, a power splitter and mixers, probably followed by some baseband gain blocks as illustrated in figure 40.

For noise analysis, a single feedback path (I or Q) is considered, with mixer and baseband gain block being the noise contributors of interest as illustrated in figure 41. By only having noise contributions at baseband-side circuit nodes, any headaches caused by having to consider mixing of noise are avoided. As will be demonstrated later in this section the analysis is still accurate for real-world systems. For analysis of the output signal-to-noise ratio of the model in figure 41, the noise voltages added by the mixer and amplifier need to be known. For the mixer, noise performance is typically specified as "noise figure", which refers to the ratio of total output noise to output noise caused by the source [25]. The source would typically be a 50Ω resistor. Hence, a block

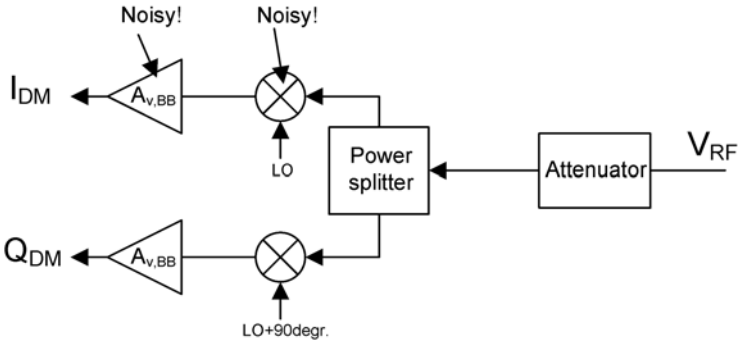


Figure 40: Typical feedback path of CFB system.

that adds the same amount of noise power as that produced by a 50Ω source resistance is said to have a noise figure of 3dB. Here it must be noted that the noise produced by the source resistance is reduced by a non-zero input impedance; in a perfectly impedance matched system (1:1) the noise power produced by the source resistance is reduced by a factor of four.

It is well-known that a resistor can be considered to contain a series voltage noise source that generates white noise with a power spectral density of

$$\bar{v_n^2} = 4kTR\Delta f \tag{46}$$

where k is Boltzmann's constant of around $1.38 \cdot 10^{-23} J/K$, T is the absolute temperature in kelvins, R is the resistance in question and Δf is the noise bandwidth. For computing the RMS noise voltage, we have

$$v_{n,RMS} = \sqrt{4kTR\Delta f} \tag{47}$$

For the case of TETRA and TEDS, the noise bandwidth of interest is 18kHz since this is the wideband noise (WBN) measurement bandwidth. Hence around 120nV_{rms} of noise is produced by a 50Ω resistor within the 18kHz bandwidth. For a device with 50Ω input, the source 50Ω resistance thus contributes with around 60nV_{rms} (or -131.4dBm) of noise.

Given a noise figure NF_{mix} for the mixer, the output-referred RMS noise voltage turns out to be:

$$v_{n,mix} = A_{v,mix} \cdot 10^{\frac{NF_{mix}}{20}} \cdot 60nV \tag{48}$$

where $A_{v,mix}$ is the conversion gain of the mixer. Typical noise figures for double-balanced passive diode-type mixers are on the order of 0.5dB higher than the mixer conversion loss (see Mini-Circuits application note [53].) This type of mixer is generally recognized to be about as low-noise and linear as possible. Given such a mixer with 7dB conversion loss ($A_{v,mix} = 0.447$), noise figure is 7.5dB (factor of 2.37) and hence the total noise at the mixer output is around 63.6nV_{rms} or -131dBm. The output noise is lower than the input noise level due to the conversion loss of the mixer.

For the baseband gain stage, state-of-the-art operational amplifiers are available (e.g. the Texas Intruments OPA846) with around $v_n = 1.5nV/\sqrt{Hz}$ of

input-referred noise when the surrounding resistances are taken into account. Assuming that such an operational amplifier is used in a low-noise non-inverting configuration, the input-referred noise added is:

$$v_{n,BBgain} = v_n \cdot \sqrt{18kHz} \tag{49}$$

which leads to $201nV_{rms}$. Adding the mixer and amplifier noise results in a total of

$$v_{n,tot} = \sqrt{v_{n,mix}^2 + v_{n,BBgain}^2} \tag{50}$$

around 210nV_{rms} of noise at mixer output. Given that mixer noise figures are unlikely to drop much below 7dB and that $v_n = 1.5nV/\sqrt{Hz}$ of operational amplifier input-referred noise is close to state-of-the-art, 210nV_{rms} is probably also close to the minimum possible noise level. Hence, the only way to alter the signal-to-noise ratio at the mixer output node is to change the amount of power put through the mixer. There is a limit to how far this can be taken in that mixer linearity in compromised at high throughput levels. Brute-force parallelization is of course another, but expensive and power-consuming, option.

With a given set of noise contributions, the signal-to-noise ratio at the output of the feedback path is simply:

$$SNR_{FB} = 20\log_{10}\frac{\sqrt{P_{in,mix} \cdot 50\Omega} \cdot A_{v,mix}}{v_{n,tot}} \tag{51}$$

Using the already found noise voltages and assuming 7dB conversion loss ($A_{v,mix} = 0.447$) and a mixer RF input power of -10dBm ($P_{in,mix} = 0.1mW$) we get an SNR of 104dB.

Although we have two parallel loops with this feedback SNR, the signals in these (I and Q) are uncorrelated like also expected for the added noise, so this parallelization does not alter the SNR. For WBN evaluation, assuming that we have two 18kHz TETRA carriers at the same power level, then in all fairness twice the amount of noise should be allowed far from the carriers, i.e. the WBN limit is -97dB referred to the power of a single carrier. Compared to the sum of the carrier powers, the limit would still be -100dB. Defining 0dBc as the total carrier power, for any number of carriers, the same -100dBc WBN limit still applies at more than 5MHz offset from any of the TETRA carrier signals.

Given that sufficient linearity can be obtained from a double-balanced mixer at -10dBm of TETRA input thus seems practically possible to stay within TETRA WBN specifications as long as noise added by inadequate phase margin or self-oscillation is avoided or otherwise dealt with by design.

8.3 High-performance CFB hardware

In order to support some of the many claims made in the above, a semi-discrete CFB linearization PCB was prototyped. In order to cut down the noise floor observed in [33] when using a CFB IC (the CML Microdevices CMX998), a discretely constructed I/Q demodulator was used as illustrated in figure 42. All used RF parts were stock parts from Mini-Circuits. It was found that acceptable ACPRs were achievable with a 10dB peak-to-average 50kHz TEDS carrier by limiting the I/Q demodulator input level to 80mV_{rms} corresponding to -9dBm.

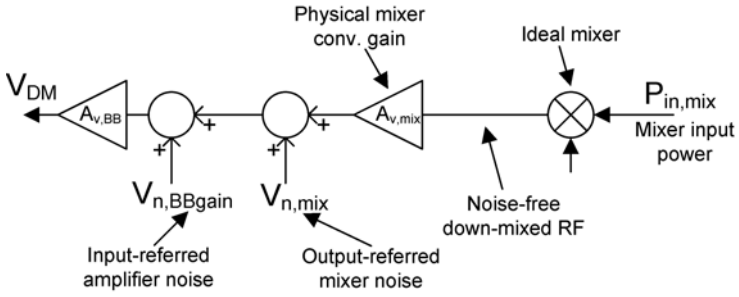


Figure 41: CFB feedback path noise analysis model.

Subtracting 3dB loss by power splitting and the 6dB attenuation average mixer input power was thus -18dBm or 15.8μW. With this mixer input power level, output signal-to-noise ratio computes to 95.5dB. As evident from figure 46 a noise floor of -95dBc is observed in the high-gain, mid-band area of the CFB loop transfer function.

For comparison with the discrete CFB design, the WBN results from [33] are also shown. Here, the I/Q demodulator had a noise figure of 21dB (lumped effect of mixer and amplifier, referenced to I or Q output) and an equivalent conversion gain $A_{v,mix}$ of 24dB. The expected output noise power is 10.67μV_{RMS}. For -23dBm of demodulator input power (or 15.8mV_{rms}), the expected output signal level is 251mV_{rms}. Hence an SNR of 87.4dB is achieved. Measurements indicate a level very close to this, although the noise floor is somewhat obscured by other distortion mechanisms in the system.

As a verification of the numbers above, the noise figure for the discrete CFB system was calculated to 17dB. Given a -131dBm noise floor set by the source resistance, the 17dB noise figure and -18dBm mixer input power, an SNR of roughly 96dB is expectable, as already computed. Similarly for the CMX998 solution, the SNR computes to $131 - 21 - 23 = 87dB$.

The CFB loop gain was measured and is shown in figure 47. It is clear that WBN peaking above 1.5MHz is due to poor phase margin (a somewhat random loop filter design was used); remembering the analysis from [33] a WBN peak of 3dB is very expectable from a CFB system with 40° phase margin. The placement of the noise peak in the WBN measurement is due to the limited number of measurement points.

The bottom line of the analytical and experimental work documented here is that CFB closed loop noise can be predicted and hence manipulated by careful design. For TETRA transmitter systems it has been shown that it close to possible with standard discrete circuitry techniques to extend the CFB bandwidth into the realm of -95/100dBc WBN limited areas. Since an n-carrier TETRA signal presents the same -100dBc WBN limit for any n then it is now valid to claim that standard circuitry techniques lead to WBN results that are 5dB out-of-spec for +/-5MHz and beyond. As such, more work is needed with noise reduction in the I/Q demodulator (around 10dB improvement beyond 1-2-3MHz should do it) in order to make multi-TETRA-carrier, CFB linearized transmitters feasible.

As for the bandwidth limitation of the CFB system due to delay, it has

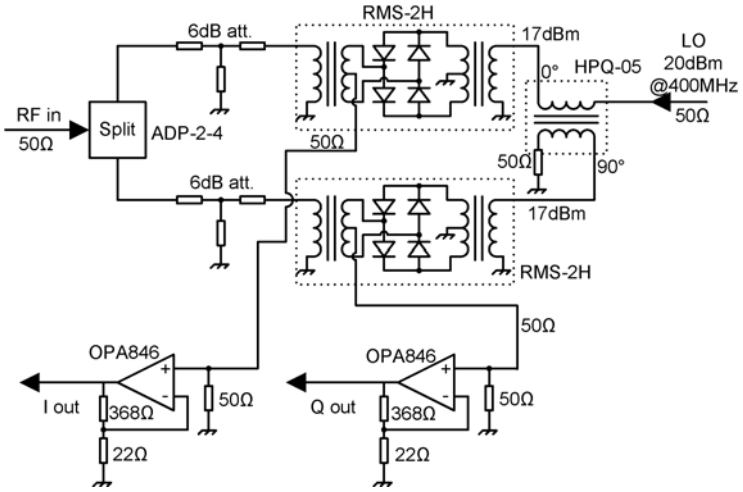


Figure 42: Implemented low-noise, high-bandwidth I/Q demodulation circuitry. Same RF circuitry was used for I/Q modulator block.

been experimentally demonstrated that the modulation and demodulation process can be implemented with around 9ns of delay, a number that by no means represents an absolute limit. It is therefore quite safe to claim that the delay contribution of the RFPA will probably be the limiting factor and this is another area that should be given considerable effort if multi-carrier TETRA transmitters are to become feasible. Since RFPA design is one of the areas that have not been investigated in this project, a qualified guess to the minimum RFPA delay will not be given here.

8.4 Summary

This section documented a late-phase experimental study of noise and bandwidth in CFB systems. It was shown how interconnect wiring may contribute significantly to limiting the achievable CFB system bandwidth and how the use of high-performance discrete parts in the CFB system allows performance barriers imposed in integrated implementations to be beaten. In particular, it was shown for a 200W (CW) class-A/B RFPA that CFB bandwidths in the 2-4MHz area may be readily achieved at 400MHz, with further improvements possible. The CFB system noise floor was shown to be of importance in high-bandwidth (1MHz+) CFB implementations since it may cause problems with the 5MHz+ WBN specification in TETRA and TEDS. In spite of this, a 2MHz bandwidth CFB implementation was demonstrated to allow full WBN compliance in a dual-role TETRA/TEDS (50kHz) RFPA system.

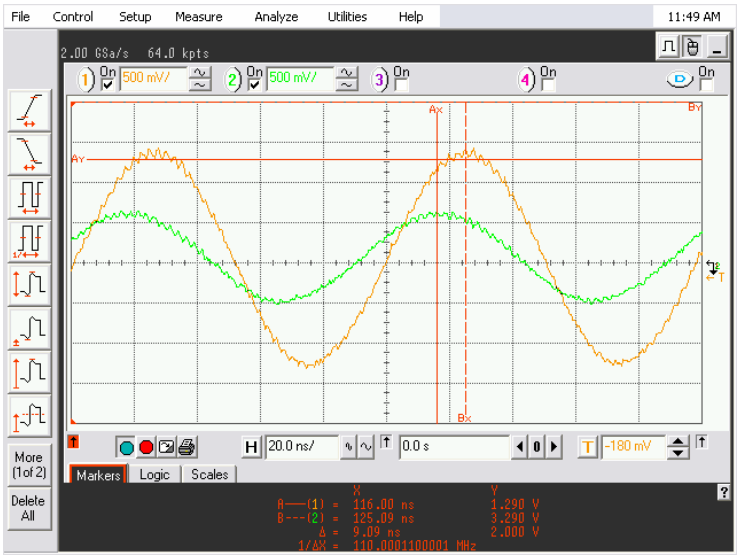


Figure 43: 10MHz sine wave I/Q modulator input and corresponding demodulator output with 5cm wire as RF path. Delay is 9ns, around 2ns of these is PCB track propagation delay.

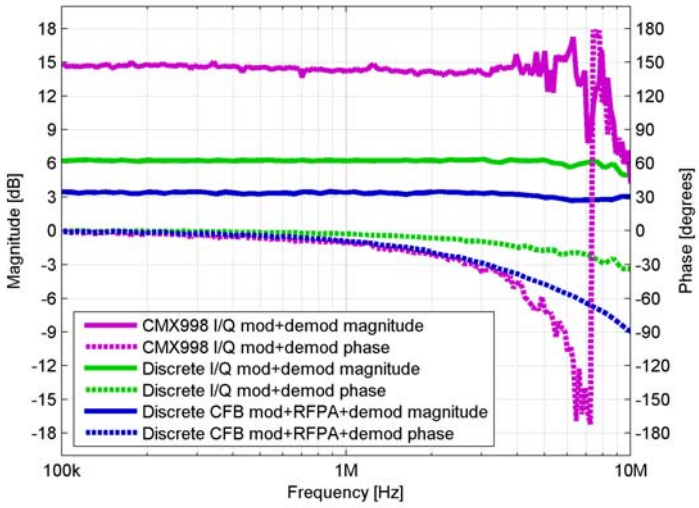


Figure 44: Measured frequency responses of mod/demod/RF path. Commercial CFB IC exhibits 30ns IQ modulator+demodulator delay, discrete design only 9ns. Adding RFPA with minimum-length wires results on 25ns overall RF path delay with discrete CFB.

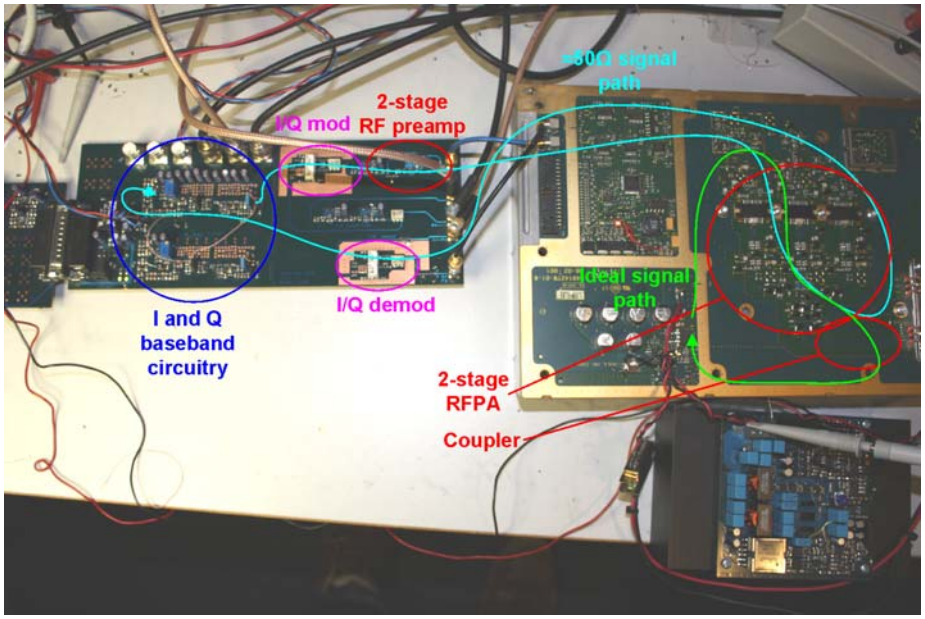


Figure 45: Discrete CFB hardware and RFPA. Implemented CFB loop signal path (cyan) is around 1m long, adding 6-7ns of the overall 25ns loop delay (see fig. 44.) Ideal signal path (green) would add only around 2ns of delay.

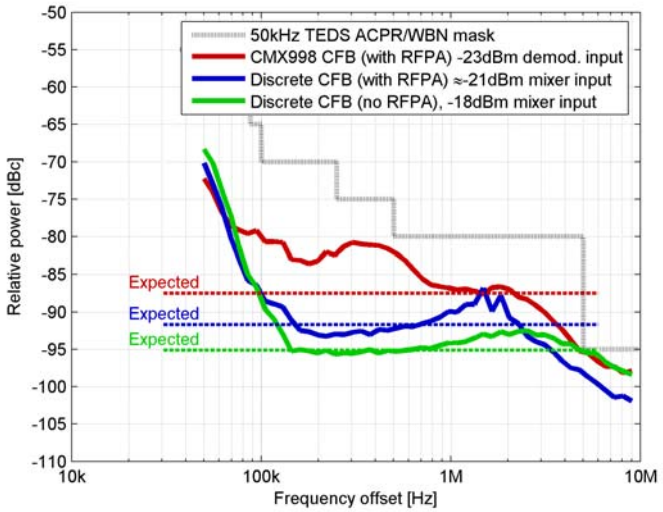


Figure 46: Measured WBN in published CMX998-based CFB system [33] and two discrete-demodulator based designs. In-band WBN floor is predictable and generally lower with discrete circuitry.

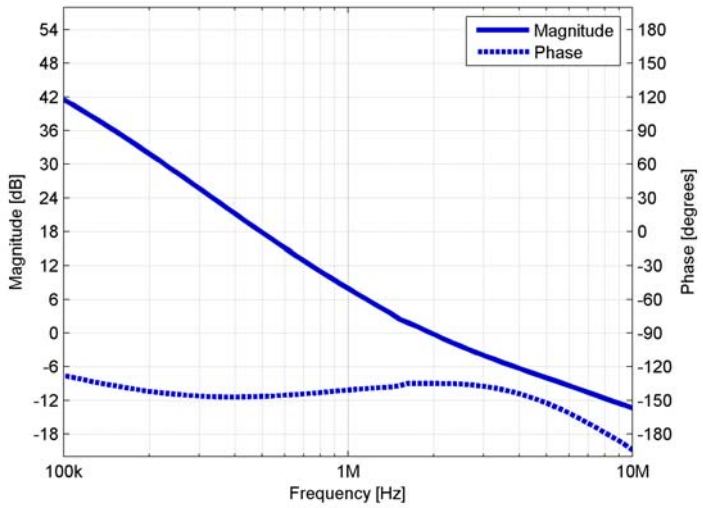


Figure 47: Open-loop frequency response of discrete CFB with RFPA as used for WBN plots in figures 46 and 48. Crossover frequency is 2MHz and phase margin is 45°.

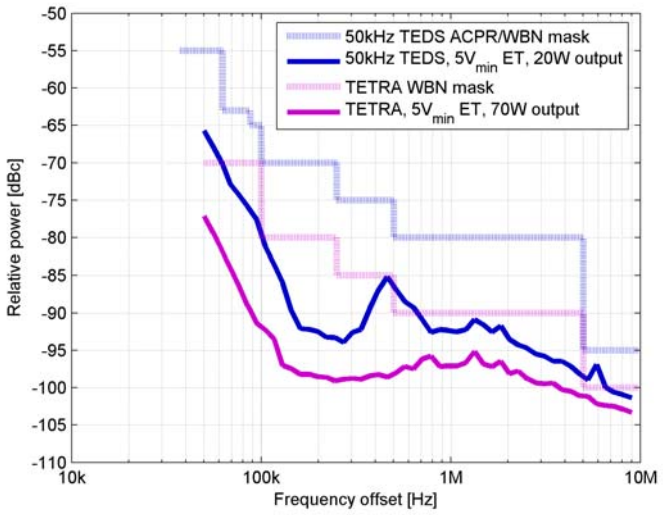
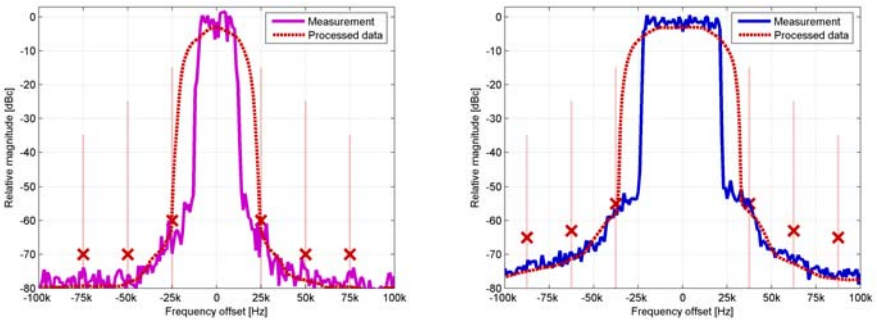


Figure 48: Measured WBN - 20W 50kHz TEDS and 70W TETRA with 5V (min.) envelope tracking. RFPA very close (around 1dB) to clipping and linearized with discrete CFB. Same hardware ensures full WBN compliance in both cases.



(a) 70W TETRA

(b) 20W 50kHz TEDS

Figure 49: Measured RFPA output spectra (RBW=500Hz) and evaluated ACPRs with 5V (min.) envelope tracking. Carrier frequency 420MHz. ACPRs are within limits although with only narrow margins.

9 Conclusion

The work presented in this thesis and the associated publications has approached many facets of the overall problem of increasing TETRA/TEDS base station radio frequency power amplifier (RFPA) efficiency.

The studied solution space has been confined to that consisting of a linear RFPA, with efficiency enhancement provided by the use of a switch-mode envelope tracking (ET) power supply and linearization provided by Cartesian feedback (CFB.) Within these boundaries, the sub-issues below were studied, resulting in solutions, explanations or key numbers where relevant. In the order of direct importance to the goal of increasing TEDS base station efficiency, major sub-issues were:

1. Applicability of envelope tracking to 50kHz TEDS base station application. Doubling of class-A/B RFPA efficiency (from 22% to 44%) has been demonstrated at the cost of adding a relatively inexpensive envelope tracking power supply to the system. Prototype transmitter output demonstrated to be *fully* compliant with base station ACPR *and* wideband noise specifications.

2. RFPA and ET power supply interaction. Frequency conversion of switching ripple, ET power supply effect on RFPA linearity and effect of non-zero ET power supply output impedance. Problems found to be manageable but in need of consideration for production designs.

3. Cartesian feedback. Limitations in noise and loop gain performance studied for the TETRA/TEDS application. High-performance implementation demonstrated. Relatively low-cost IC-based solutions found adequate for 50kHz TEDS application.

4. ET power supply power conversion solutions. Buck converter with fourth-order output filter demonstrated to be ideal for TETRA and 50kHz TEDS. Multi-phase topologies found necessary for significantly higher ET bandwidths.

5. Control strategies for fourth-order filtered buck converters. Hysteretic self-oscillating (sliding mode) control found and *proven* to be optimal for single-phase buck converter given that control loop bandwidth is the primary requirement. Simple linear PID+PD voltage-feedback structure proposed and demonstrated in several papers.

6. Switch-mode control IC design. Practical scope for increasing mileage of self-oscillating control methods by reduction of switching delay reduction examined. Today's control ICs found to be far from as fast as possible.

7. Switch-mode control philosophy. Parallel universes of self-oscillating control and sliding mode control bridged. Major contributions to work on a universal model for buck converter control systems.

8. Switch-mode control loop linearity. Examined on the application of class-D audio amplification. Method for maximizing self-oscillating controlled buck converter input/output linearity proposed and demonstrated.

In addition to the 50kHz TEDS application, the TETRA application was kept in mind throughout. Numbers were added where relevant and it was shown that it is possible to use the same ET power supply and CFB system hardware to transmit either a TETRA or TEDS carrier. For the challenge of transmitting two TETRA carrier simultaneously with the same RFPA, both the ET power supply and CFB system design tasks were found to be a much more difficult. So while it is *safe* to conclude that envelope tracking is *feasible and useful* in a TETRA/TEDS base station RFPA, it is very risky to claim so for dual-carrier TETRA.

10 Perspectives on further research

This thesis demonstrated solutions to a number of practical problems in the application of envelope tracking to TETRA and TEDS base station RFPAs. Additionally, a number of more academic problems were considered under the excuse of the need to solve the practical problems. The width of topics covered is what lead to good overall system results. As a side effect however, many more or less "narrow" sub topics remain unexplored. These include:

- Switching frequency stabilization methods for self-oscillating controllers. Many implementations exist. A comparative study is missing.
- The trade-off between tracking bandwidth and efficiency. Obviously, infinite tracking bandwidth allows maximum RFPA efficiency improvement and zero bandwidth leads to nothing. What about the solutions in between?
- Discrete-time switching controller modeling. The LTI/comparator modeling approach has been demonstrated for single-phase buck converters. What about multi-phase? What about non-uniform sampling systems (D different from 0.5)?
- ET power supplies using multi-phase buck *and* fourth-order filter. The ultimate low-ripple method. Higher effective ripple frequency allows higher bandwidth. What kind of performance is possible?
- ET power supplies using fourth-order filter *and* linear power stage. Fourth order filter has little output ripple so linear power stage does not need to drive a lot of ripple. A possible zero ripple, high-bandwidth concept?
- Envelope tracking with less linear RFPAs. This project used a decently linear class-A/B RFPA. However, the CFB system can provide a lot of loop gain below 100-200kHz. Could we down-bias the class-A/B RFPA? Use a class-C RFPA?
- Envelope tracking with more linear RFPAs. A class-A RFPA is abysmally inefficient with high peak-to-average carriers. An ET power supply would win back a lot of efficiency. A possible route for carriers of high bandwidth?
- Mains-to-RF power efficiency. What counts in the end. How do we get from 90-230VAC to an envelope tracking RFPA supply rail (or the RF carrier) at maximum efficiency? Number of switching power stages? Isolated PFC to 48VDC to ET power supply two-stage concept?
- Self-oscillating control with minimum delay. How fast can we make a buck control IC? A 50ns control/power train would win significant mileage for the hysteretic PID+PD solution...
- Lower-power envelope tracking from a battery rail. We also have TETRA/TEDS subscribers that would benefit from envelope tracking. Could a buck-boost, boost, or buck-or-boost converter deliver the performance of the fourth-order filtered buck?

- Digital implementation of the ET power supply control system. Digital means portable and reconfigurable. Base station hardware has a lot of programmable digital logic gates. Would it be possible to deliver the performance of analog circuitry (hysteretic PID+PD) from a largely VHDL-based digital controller implementation?
- EER RFPA for TETRA. The TETRA carrier avoids zero crossings in the I/Q plane like EDGE (although synchronization symbols lie at the origin.) The EER technique nonetheless sounds possible to match up with the TETRA application. Need an ultra-low ripple (0.5mV area), high-bandwidth (100kHz area) power supply, but overall RFPA efficiency could be very high...

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11 Appendices - published papers and patents

TEDS Base-Station Power Amplifier Using Low-Noise Envelope Tracking Power Supply

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***Abstract*—This paper demonstrates a highly linear and efficient TETRA enhanced data service (TEDS) base-station RF power amplifier (RFPA). Based on the well-known combination of an envelope tracking (ET) power supply and a linear class-A/B RFPA, adequate adjacent channel power ratio (ACPR) and wide-band noise performance is shown to be enabled only by further incorporating high-bandwidth Cartesian feedback (CFB) and using a low-noise ET power supply. It is demonstrated that CFB loop bandwidth is limited by modulator/demodulator/RF path group delay to around 2 MHz in the considered setup, and that there exists a significant tradeoff between the depth of the ET and open-loop RFPA linearity, as well as overall efficiency. An empirical method for determining the permissible amount of switching ripple on the ET supply is presented, showing very good accuracy. Performance of the prototype RFPA system is verified experimentally with a 9.6-dB peak-to-average 50-kHz 16 quadrature amplitude modulation TEDS carrier, the setup providing 44-dBm (25 W) average RF output power at 400 MHz with 44% dc-to-RF efficiency state-of-the-art ACPR of less than −67 dBc, switching noise artifacts around −85 dBc, and an overall rms error vector magnitude below 4.5%.**

***Index Terms*—Cartesian feedback (CFB), envelope tracking (ET), linearization, power amplifiers (PAs).**

I. Introduction

In RECENT years, much research has been targeted at improving the efficiency of RF power amplifiers (RFPAs) while preserving linearity [1]. A major driving force has been the requirement for maintaining a reasonable RFPA linearity in spite of the migration from the relatively constant-envelope phase-shift-keying (PSK)-based modulation schemes (as used in global system for mobile communication (GSM), EDGE, and TETRA) to more spectrally efficient variable-envelope schemes like quadrature amplitude modulation (QAM), as applied in the considered case of the TETRA enhanced data service (TEDS). The technical problem lies in the fact that linear RFPAs (such as class-A or A/B) exhibit much lower efficiencies at less than full output levels [1] in spite of being theoretically capable of providing acceptable peak efficiency levels (50% and 78.5%, respectively.) As a numerical example, a class-A/B power amplifier (PA) that can be expected to provide up to around 45% drain efficiency with a TETRA carrier will, as evident from this paper, provide only 23% drain efficiency with a TEDS carrier due to the increase in peak-to-average power ratio from roughly 3.2 dB to around 10 dB.

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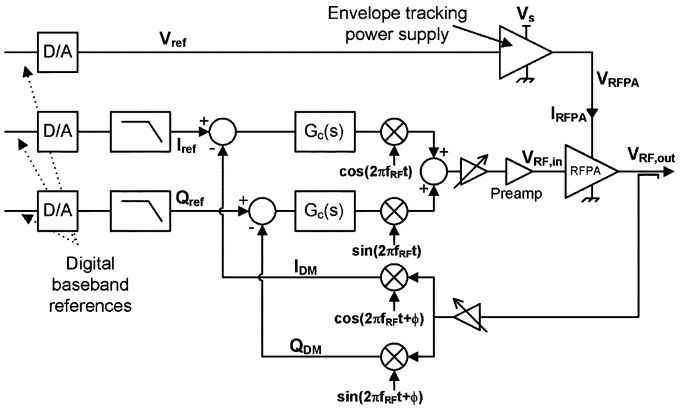

Fig. 1. Solution studied for high-efficiency TEDS RF power amplification.

A broad range of solutions has been proposed and demonstrated for increasing RFPA efficiency based on modulating the drain voltage of the RFPA power device(s), including envelope elimination and restoration (EER) [2], [3] and envelope tracking (ET) [4]–[6]. While EER ensures that the RFPA is operated fully saturated (and therefore, at maximum efficiency) at all times, drawbacks exist in the form of the requirement for high bandwidth in the modulating power supply [7]–[9] and no rejection of supply-line noise since the supply voltage directly dictates the RFPA output. The latter is of importance in TETRA and TEDS systems where very low power leakage (typically from −80 to −90 dBc depending on the carrier type) is allowed at typical switching frequency offsets (1-MHz area) from the carrier [10]. Therefore, this study explores the ET solution to TEDS power amplification, combining a production model LDMOS RFPA designed for TETRA with a state-of-the-art ET power supply solution [11], [12]. It will be illustrated that ET causes an increase in RFPA distortion, hereby necessitating a highly effective linearization system. To this end, Cartesian feedback (CFB) is an appropriate solution [13], [14], due to the limited bandwidth (50 kHz in the case considered) and tight adjacent channel power ratios (ACPRs) (from −55 to −65 dBc) required for a TEDS carrier. For comparison, state-of-the-art reported ACPR figures for wideband code division multiple access (WCDMA) RFPAs [5], [15]–[18] are on the order of 50–60 dBc using digital predistortion (DPD). Hence, current DPD technology is close to useful for TEDS, but CFB still offers greater ACPR margins. The system topology considered is shown in Fig. 1, where the CFB loop is kept in the analog domain to avoid quantization noise problems. Additionally, this prevents A/D and D/A delays from eroding the obtainable loop bandwidth as often seen

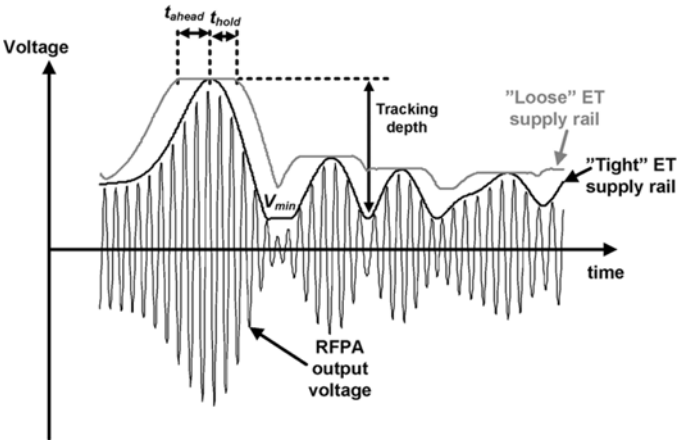

Fig. 2. Basic ET schemes and associated terminology used in this paper.

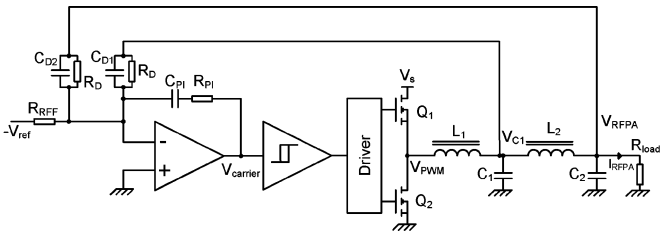

Fig. 3. Considered ET power supply solution [12].

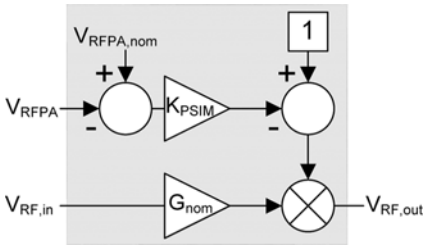

Fig. 4. RFPA model taking into account the effect of varying supply voltage on gain.

in digital controllers for dc/dc converters [19], [20] where typical bandwidths are comparable to (or lower than) those in CFB systems.

II. ET Power Supply

With efficiency being the driving force behind application of the ET power supply, switch-mode dc–dc converter technology forms a natural starting point. In the TEDS amplification application, the RF signal bandwidth (50 kHz) is low enough to allow the use of an efficient and inexpensive single-phase buck converter (also known as class-S modulator) for ET. When augmented with a fourth-order *LC* output filter, very low output ripple is achievable at moderate switching frequencies [7], [11], [12], [21]. The use of a moderate 1-MHz switching frequency allowed the ET power supply used for this study to have an efficiency in the 90%–95% range with the type of load currents and voltages required by the RFPA.

Modeling the RFPA as an ohmic load, it is principally possible to tune the fourth-order output filter to exhibit the desired frequency response, e.g., a Bessel-type response for minimum over/undershoot and constant group delay. This solution requires the generated RFPA supply voltage to be proportional to the RFPA load current at all times in order to preserve ohmic load impedance. This excludes the possible use of early ramp-up and peak-hold of the RFPA supply voltage (illustrated in Fig. 2 for the "loose" ET supply rail) as could be used when the ET power supply is not fast enough to perfectly track the RF signal envelope (by "tight" ET.) Therefore, to maintain system flexibility, the ET power supply used has feedback control of its output voltage. Implementation of look-ahead is straightforward in a digital signal processor (DSP). If the ET power supply group delay is lower than that of the in-phase/quadrature (I/Q) baseband filters (as was the case in the setup used for this paper), look-ahead may be implemented without increasing the overall data latency of the transmitter.

It has been shown [22] that pulsewidth modulation (PWM) controllers based on self-oscillation allow the absolute maximum control bandwidth to be obtained for a given switching frequency due to the combination of an oscillator and a power converter controller in one and the same control loop. Applying Barkhausen's criteria for oscillation, it follows that the crossover (unity-gain) frequency of the oscillating loop equals the oscillation (switching) frequency. The same conclusion can be reached by modeling self-oscillating control systems using discrete-time techniques [23]. The hysteretic self-oscillating controller is illustrated in Fig. 3. This simple arrangement can be optimized to behave as a third-order Bessel low-pass filter [12], ideal for ET due to the property of constant group delay over frequency.

Variable switching frequency is an often cited [21] negative property of the hysteretic control scheme, but this can be counteracted by the use of variable feedback-controlled hysteresis [11], [12]. By incorporating a phase-locked loop (PLL) into the hysteresis control system, it is possible to phase lock the steady-state switching frequency of the converter to an external clock.

III. ET Power Supply Ripple Specification

It is well known [4], [12], [24] that switch-mode power supply ripple causes sidebands to appear at the RFPA output. This effect can be predicted through accurate RFPA device models [24], as found in some integrated circuit (IC) design software packages. This approach does not lend itself as well to discrete PA designs due to the unavailability of such device models. Instead, experimental characterization of candidate RFPAs can be used. Disregarding the actual physical mechanisms behind supply intermodulation (IM) and instead treating the RFPA as a "black box," it is obvious that a mixing process between supply rail and RF voltage has to take place to account for the appearance of sidebands. This line of thought leads to the empirical RFPA model of Fig. 4, where supply deviations are scaled by a factor K_{PSIM} before modulating the gain of the RFPA. Any RFPA phase response variation with supply is not modeled and RFPA gain is assumed to decrease with decreasing supply voltage.

Assuming that the RFPA is amplifying a continuous wave (CW) input

$$V_{\mathrm{RF,in}}(t) = A_{\mathrm{RF}} \cdot \cos(2\pi f_{\mathrm{RF}}\, t) \tag{1}$$

and the supply voltage has dc and ac components

$$V_{\mathrm{RFPA}}(t) = V_{\mathrm{RFPA,nom}} + A_{\mathrm{ripple}} \cdot \cos(2\pi f_{\mathrm{sw}} t) \quad (2)$$

i.e., a sinusoidal constant-frequency ET supply ripple, then applying the usual mixing equation results in the normalized RFPA output

$$\frac{V_{\mathrm{RF,out}}(t)}{A_{\mathrm{RF}} G_{\mathrm{nom}}} = \cos(2\pi f_{\mathrm{RF}} t) + K_{\mathrm{PSIM}} \cdot \frac{A_{\mathrm{ripple}}}{2} \cos(2\pi(f_{\mathrm{sw}} + f_{\mathrm{RF}})t) + K_{\mathrm{PSIM}} \cdot \frac{A_{\mathrm{ripple}}}{2} \cos(2\pi(f_{\mathrm{sw}} - f_{\mathrm{RF}})t) \quad (3)$$

which describes the amplitude of the power supply intermodulation (PSIM) sidebands using the empirical K_{PSIM} and ET power supply ripple.

For comparison, in an EER system, the RFPA output would ideally be given by

$$V_{\mathrm{RF,out,EER}}(t) = V_{\mathrm{RFPA}} \cdot \cos(2\pi f_{\mathrm{RF}} t). \quad (4)$$

With the same supply signal definition, this leads to

$$\frac{V_{\mathrm{RF,out,EER}}}{V_{\mathrm{RFPA,nom}}} = \cos(2\pi f_{\mathrm{RF}} t) + \frac{A_{\mathrm{ripple}}}{2V_{\mathrm{RFPA,nom}}} \cos(2\pi(f_{\mathrm{sw}} + f_{\mathrm{RF}})t) + \frac{A_{\mathrm{ripple}}}{2V_{\mathrm{RFPA,nom}}} \cos(2\pi(f_{\mathrm{sw}} - f_{\mathrm{RF}})t). \quad (5)$$

Therefore, as far as IM sidebands are concerned, the EER system exhibits a K_{PSIM} of $1/V_{\mathrm{RFPA,nom}}$. This simply reflects that it is (logically enough) the ratio between supply ripple and dc voltage that determines the relative power of ripple-induced sidebands in an EER system.

In order to characterize the considered RFPA, IM products were measured for different frequencies and dc supply voltages, resulting in the K_{PSIM} measurement results in Fig. 5. The RFPA CW output was 20 dBm, i.e., clipping was avoided even at 5-V supply. The PSIM effect was found to be largely frequency independent (dc–700 kHz) and strongly variable with supply voltage. In particular, K_{PSIM} increased sharply at low supply voltages, which is also where the gain of the RFPA gradually collapsed. However, these phenomena did not correlate completely in the considered RFPA. From a practical point-of-view, it seems that characterizing the PSIM mechanism at low frequencies provides substantial insight on the higher frequency behavior, which is much more difficult to measure. Also, it is evident that avoiding EER operation (or hard clipping) of the linear RFPA increases its immunity to power supply noise by around 5–15 dB. This is perhaps less than anticipated (when considering the PA device to be an ideal transconductance), but still provides an opportunity for significantly relaxing the ripple specification on the ET power supply.

Considering the QAM transmission modes in the TEDS standard, carrier power is measured across the entire carrier bandwidth (i.e., 50 kHz for 50-kHz QAM), whereas wideband noise (WBN) and ACPR are measured in a TETRA channel bandwidth (18 kHz). This reduces the PSIM problem since the power

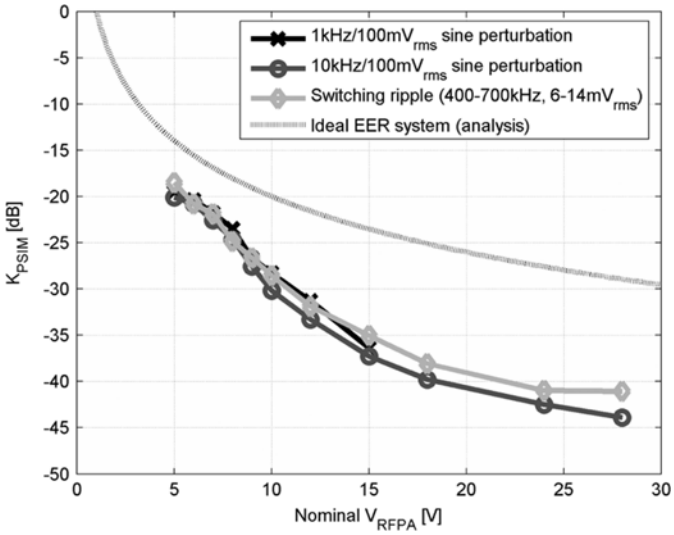

Fig. 5. Measured values of K_{PSIM} on class-A/B RFPA at different supply voltage operating points with 20-dBm CW nominal RFPA output.

TABLE I
PARAMETERS IN ET POWER SUPPLY RIPPLE SPECIFICATION DERIVATION

Parameter	Value
$BW_{carrier}$	50kHz
BW_{WBN}	18kHz
f_{sw}	1MHz
$P_{WBN}(f_{sw})$	-80dBc
V_{RFPA}	5-28V
$\max\{K_{PSIM}\}_{V_{RFPA}}$	-18.5dB (=0.12)
A_{ripple}	4.6mV

of IM products at $\pm f_{\mathrm{sw}}$ is spread over multiple measurement bands. Assuming K_{PSIM} to be constant, the ripple IM products will each have the following power relative to the carrier:

$$P_{\mathrm{PSIM,dBc}} = 20 \cdot \log_{10}\left(\frac{1}{2} K_{\mathrm{PSIM}} A_{\mathrm{ripple}}\right). \quad (6)$$

Taking into consideration the effect of potentially different bandwidths for carrier $(\mathrm{BW_{carrier}})$ and WBN measurement $(\mathrm{BW_{WBN}})$ and solving for A_{ripple} leads to a useful design equation

$$A_{\mathrm{ripple}} < \frac{2 \cdot 10^{\frac{P_{\mathrm{WBN}}(f_{\mathrm{sw}})}{20}} \cdot \frac{\mathrm{BW_{carrier}}}{\mathrm{BW_{WBN}}}}{\max\{K_{\mathrm{PSIM}}\}_{V_{\mathrm{RFPA}}}} \quad (7)$$

where $P_{\mathrm{WBN}}(f_{\mathrm{sw}})$ is the specified [10] relative WBN limit at frequency offset equal to the ET power supply switching frequency. Note that this derivation assumes that there is no effect of the CFB system.

In the 50-kHz QAM TEDS base-station application, key parameters in the ET power supply ripple specification derivation are summed up in Table I. Evidently, a very low ripple of 4.6 mV (peak) is required to ensure that the ripple-induced PSIM sidebands stay within the WBN limit. This level of ripple performance is achievable using the ET power supply topology considered, though not at very high- or low-output voltages [11] due to uncontrollable switching frequency drops caused by finite control loop delay. This coincides with the worst case scenario for PSIM, which is at low output powers (and therefore, supply

low voltages) where K_{PSIM} is maximal, leading to the highest relative PSIM sideband powers. The increase in K_{PSIM} with lower supply voltages is less of a concern for high RFPA output powers because the absolute power of the PSIM sidebands generated in low-voltage periods is still low compared to the absolute carrier power. In practice, it is possible to impose a higher supply voltage minimum during low average output power operation, using the 5 V minimum only for high-power operation where the associated efficiency increase is most useful and the effect of high K_{PSIM} during low-voltage periods is limited.

IV. CFB Optimization

Generally, the capability of a CFB system to suppress RFPA distortion at a given frequency offset can be described by the sensitivity function $S_{\mathrm{CFB}}(s)$ given as

$$S_{\mathrm{CFB}}(s) = \frac{1}{1 + G_{\mathrm{CFB}}(s)} \tag{8}$$

where $G_{\mathrm{CFB}}(s)$ is the open-loop transfer function of the I/Q feedback loops and $s = j2\pi f$ with f is the absolute value of the frequency offset. The open-loop transfer function is determined by the CFB compensator transfer function $G_c(s)$, as well as the modulator/RFPA/demodulator chain, which may be modeled as a gain K_{RF} and an equivalent group delay t_{GD} [25] that accounts for physical delay in transmission lines, as well as group delay associated with bandwidth limitations in the RFPA and I/Q modulator/demodulator circuitry. Expressed in the frequency domain, we therefore have a CFB loop gain model of

$$G_{\mathrm{CFB}}(s) = G_c(s) \cdot K_{\mathrm{RF}} \cdot e^{s \cdot t_{\mathrm{GD}}}. \tag{9}$$

At a given frequency, the time delay t_{GD} contributes with a phase shift of

$$\varphi_{\mathrm{GD}}(f) = -360^\circ \cdot t_{\mathrm{GD}} \cdot f. \tag{10}$$

Further given that $G_c(s)$ contributes with a -90° phase shift at the crossover frequency f_0, then the total phase lag at this frequency is

$$\varphi_{\mathrm{tot}}(f_0) = -90^\circ + \varphi_{\mathrm{GD}}(f). \tag{11}$$

Now, if the CFB loops need to be closed with a specified phase margin φ_m, which can be expressed as

$$\varphi_m = \varphi_{\mathrm{tot}}(f_0) + 180^\circ \tag{12}$$

then the maximum crossover frequency (i.e., bandwidth) of the CFB system is

$$f_{0,\max} = \frac{90^\circ - \varphi_m}{360^\circ t_{\mathrm{GD}}}. \tag{13}$$

It follows from this that group delay in the RF path directly limits the possible CFB bandwidth, as also observed in prior art [26]–[28]. Therefore, knowledge of the RF path group delay t_{GD} is important for estimation of the linearization improvement achievable with a CFB system.

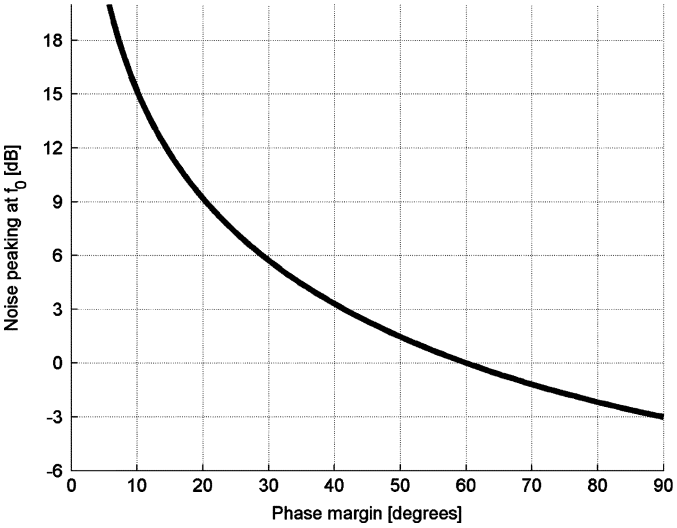

Fig. 6. Analytical relationship between CFB system phase margin φ_m and noise/distortion peaking at the crossover frequency f_0.

Noting that the following by definition applies at the crossover frequency:

$$|G_{\mathrm{CFB}}(j2\pi f_0)| = 1 \wedge \angle G_{\mathrm{CFB}}(j2\pi f_0) = -180^\circ + \varphi_m \tag{14}$$

which can be re-expressed in the complex plane as

$$G_{\mathrm{CFB}}(j2\pi f_0) = -\cos(\varphi_m) + j\sin(\varphi_m) \tag{15}$$

then the significance of adequate phase margin is evident from evaluating

$$S_{\mathrm{CFB}}(j2\pi f_0) = \frac{1}{1 - \cos(\varphi_m) + j\sin(\varphi_m)}. \tag{16}$$

Magnitudes of this expression of greater than unity correspond to amplification of unwanted noise/distortion, producing a noise spectrum peak at f_0. The magnitude of this peak is the same as the magnitude of S_{CFB}. The effect can be evaluated from Fig. 6. Since there is a limit to how much spectral content may exist at any f_0 (given as WBN limits in the TEDS specification), it is reasonable to assume that the CFB loop phase margin should be kept in the 40°–60° area. This especially applies to the experimental system design shown in this paper, where the ET power supply ripple IM products lie in the area of f_0, i.e., $f_{\mathrm{sw}} \approx f_0$.

For experimental evaluation of the actual t_{GD}, a gain-phase analyzer was used to measure the baseband-referred frequency response of the modulator/RFPA/demodulator chain. The measurement setup is illustrated in Fig. 7. The frequency response from V_{MOD} to V_{DM} was evaluated. Results are shown together with the measured $G_{\mathrm{CFB}}(s)$ in Fig. 8. An RFPA bypass allowed the modulator/demodulator delay to be isolated, thus providing exact details on the RFPA contribution to t_{GD}. It was concluded that the RF path has a frequency-independent magnitude response, as expected, with a phase lag that is roughly proportional to frequency, as expected for a time delay. The RFPA is shown to contribute with around 24 ns of delay, while the modulator and demodulator (and cables) add a total of 29 ns.

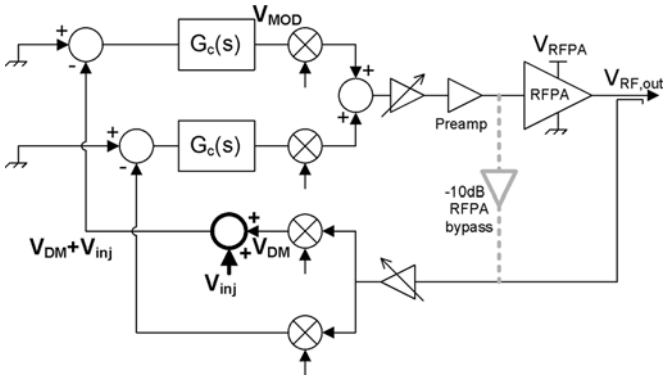

Fig. 7. Measurement setup for CFB loop characterization.

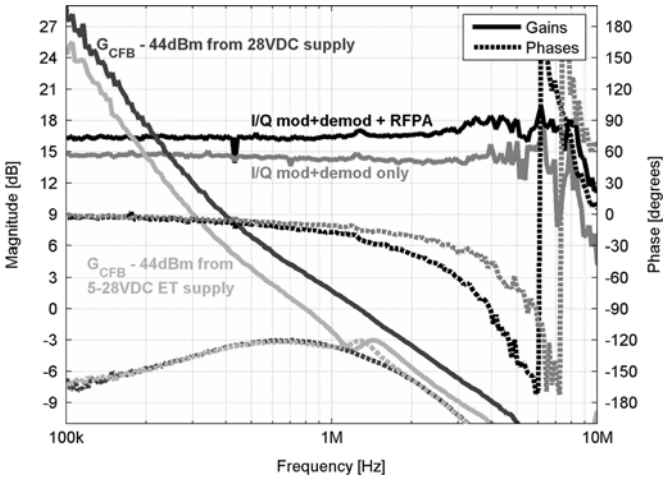

Fig. 8. Measured CFB loop characteristics. Full lines are magnitudes, dashed lines are phases.

Thus, with an overall group delay in the area of 50 ns, the CFB loop bandwidth is limited to around 1.7 MHz assuming a phase margin requirement of 60°.

Therefore, optimization of the CFB is a matter of ensuring that: 1) the noise level of the modulator/demodulator components is low enough to not be a limiting factor in WBN performance and 2) $G_c(s)$ is designed with -90° phase lag in the 1–2-MHz area and as much gain slope as possible at lower frequencies.

V. Experimental Results

The complete TEDS transmitter system consisting of ET power supply, RFPA, and CFB linearization was tested under various conditions with a 50-kHz 16-QAM TEDS carrier to validate analytical results and to demonstrate the functionality of the complete concept. To demonstrate compliance with the TEDS standard, the main parameters considered were ACPR, WBN, and error vector magnitude (EVM). The prototype system setup consisted of a PC running MATLAB for synthesizing periodical I/Q vectors and calculating the required ET supply voltage reference, connected via USB to a custom PCB with 16-bit AD5542 DACs and waveform storage memory. The bandwidth of the implemented ET power supply was sufficient to allow use of tight ET, i.e., without the use of look-ahead and peak-hold. Time alignment between the RFPA output and the ET supply rail was done by simultaneous inspection of RFPA output and the ET supply rail on an oscilloscope. Precision on the order of ± 1 μs was found necessary to achieve the demonstrated results. Baseband I/Q filters were analog 30-kHz fourth-order Butterworth low-pass types, and CFB was implemented using a CML CMX998 integrated device. Cartesian loop phase (ϕ in Fig. 1) tuning was done manually, but could be automated as richly demonstrated in prior art [25], [29].

TABLE II
Prototype TEDS Transmitter ACPR Results at 44-dBm Output

	ACPR1 [dBc]	ACPR2 [dBc]	ACPR3 [dBc]
Specification	-55.0	-63.0	-65.0
No CFB - 28VDC	-48.4	-54.5	-59.5
No CFB - 5-28V ET	-29.0	-39.9	-51.0
With CFB - 28VDC	-69.5	-74.1	-76.4
With CFB - 5-28V ET	-67.7	-70.0	-69.1

CFB loop compensators were second order, designed around 20-MHz AD8618 low-noise opamps and shaped to provide close to -90° phase shift at 1 MHz and 12-dB/octave magnitude response slope below 300 kHz for optimum low-frequency loop gain. The RFPA was a mass-produced 350–450-MHz class A/B LDMOS design based on three paralleled Freescale MW5IC970N power devices. RFPA power rating was 200-W CW with a supply voltage of 28 VDC.

The open-loop frequency response of the CFB system was measured using the technique from Fig. 7, evaluating $V_{\rm DM}/(V_{\rm DM} + V_{\rm INJ})$. Magnitude and phase responses are shown in Fig. 8, demonstrating that the CFB loop bandwidth is in the area of 800 kHz -1.5 MHz with a phase margin in excess of 40. A decrease in bandwidth is observed with 5–28-V ET supply, which can be attributed to the reduction in average RFPA gain with reduced average supply voltage. The "kinks" in loop magnitude and phase responses at 1.1 MHz were found to be caused by a resonant peak in the power supply impedance seen by the RFPA. Wiring inductance between the ET power supply and the RFPA resonated with the RFPA on-board supply decoupling capacitance. Practically, this points toward a necessity for integrating the ET power supply and RFPA blocks on a common circuit board for RFPA systems with higher ET and CFB bandwidths.

The full-power ACPRs of the CFB linearized prototype transmitter are summarized in Table II along with nonlinearized figures for comparison. It is evident that the loop gain of the CFB system is large enough to ensure that all ACPRs are well within specifications. Notably, the use of ET has a significant detrimental effect on RFPA linearity (almost 20-dB degradation of ACPR1 is observed), but this is almost fully counteracted by the CFB linearization, which provides 39-dB improvement of ACPR1. ACPRs were found to stay at the levels listed for output powers from 34 to 44 dBm.

The definition of efficiency in this work is $\eta = P_{\rm out,RF}/P_s$, where $P_{\rm out,RF}$ is the RFPA output power and P_s is the dc input power to the ET power supply. Basically, this is the RFPA drain efficiency, with the power loss in the ET power supply included in the RFPA drain input power. The relationship between ET depth and efficiency can be assessed from Fig. 9. It is evident that deep ET offers the greatest efficiency improvement, but

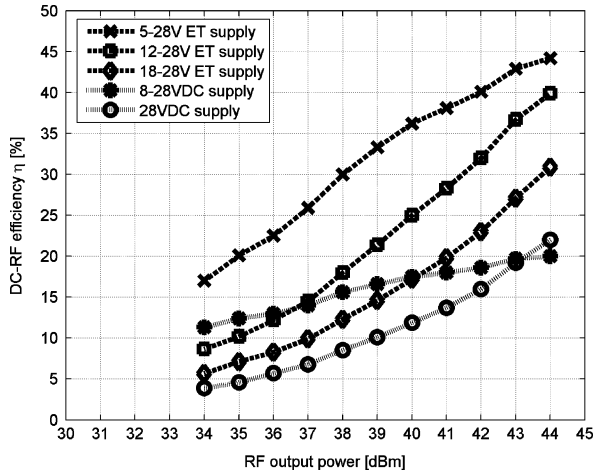

Fig. 9. Measured RFPA efficiency with TEDS carrier for various power supply configurations.

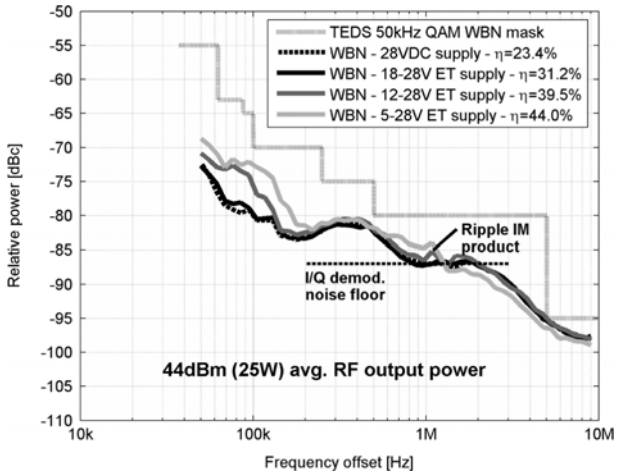

Fig. 10. Measured closed-loop WBN (worst case of carrier left/right sides) at 44-dBm output level. WBN spec is met at all offsets with 5–28-V ET supply.

with a 12 V minimum still providing a reasonable improvement from 23% to almost 40% at maximum power (44 dBm). A different supply option, variation of the RFPA supply voltage with the peak RFPA output power [8], was also examined. As seen, this leads to significant improvements in low-power efficiency. However, the concern in a base station is not average battery lifetime as in portable radios [8], but rather worst case backup battery lifetime and especially worst case thermal requirements.

WBN performance of the transmitter system at full power can be evaluated from Fig. 10. A vector signal analyzer (VSA) was combined with a discrete low noise mixer (double-balanced diode type) and a narrowband crystal filter was used to filter out the carrier to obtain the very large (105 dB) dynamic range required for this measurement. The main points to observe are that WBN is within specifications for 5–28-V ET supply with the less aggressive schemes being almost out-of-specification at ± 5 MHz. The difference in noise level can be attributed to the difference in CFB loop gain caused by reduced RFPA gain, which acts to lower the absolute output noise power while maintaining carrier power. With ET supply, a slight increase in noise around 1 MHz is seen, especially with 5–28-V ET, which is due to the 1-MHz ET power supply switching ripple. A dc supply with negligible noise was used for the 28 VDC measurements, thus it has been demonstrated that the ET power supply solution used contributes with minimal ripple IM products. At lower offsets (especially within the ACPR measurement bands), the adverse effect of ET on RFPA linearity is visible, but the effect disappears above 300 kHz. The flat shape of the WBN spectrum in the 300–400-kHz region is caused by the slopes of the RFPA distortion skirts being equal to the CFB loop gain slope. The data sheet noise figure of the CMX998 demodulator (22 dB) dictates a -86-dBc in-band noise floor given the drive power level of -23 dBm and a -131-dBm matched system thermal noise floor over the 18-kHz bandwidth used for TETRA and TEDS ACPR and WBN measurements. Hence, the I/Q demodulator contributes to the WBN spectrum shape for frequencies from 700 kHz and to beyond 10 MHz. It is clear that either a lower noise figure or higher third-order intermodulation intercept point (IIP3) would be required from the I/Q demodulator (in addition to a reduction of overall loop delay) for significant extension of the CFB bandwidth beyond the demonstrated 1 MHz.

Finally, EVM was measured for output powers from 34 to 44 dBm. At all powers, a root mean square (rms) EVM of around 4.5% was observed, with an intrinsic 3.8% EVM in the baseband I and Q references caused by the TEDS modulation scheme and following signal processing. The TEDS standard specifies a maximum rms EVM of 10%. In other words, the linearized RFPA contributes minimally to EVM and the transmitter EVM performance is well within specifications.

VI. Conclusion

A comprehensive experimental system-oriented study of a candidate high-efficiency high-linearity RFPA solution based on ET and CFB has been presented. Mainly applicable in low-bandwidth digital RF systems with high peak-to-average power carriers (such as TEDS or iDEN), the overall solution relies heavily on high-bandwidth feedback control of both the ET power supply and the RFPA output itself. It was demonstrated how application of the ET power supply rail to a representative production model class-A/B RFPA clearly decreased its linearity, but that it was possible to sufficiently compensate for this in a 50-kHz bandwidth application using CFB. Further, a simple empirical approach for modeling and determining the requirements for high-frequency switching noise (ripple) on the ET power supply output was proposed and demonstrated. Likewise, a method was demonstrated for evaluating the group delay of the RF components in the Cartesian loop, shown to the main factor limiting the obtainable bandwidth and hereby linearization improvement. In the 400-MHz application considered, Cartesian loop bandwidth was limited to 1–2 MHz, hereby also limiting the prototype RFPA system to handling carriers with 50–100-kHz bandwidth. The noise contribution of the ET power supply used was shown to be almost nondetectable against the distortion and noise generated by the system RF components. The complete prototype RF transmitter was shown to output a 50-kHz 16-QAM TEDS carrier at 44 dBm (25 W) with 44% dc–RF efficiency while maintaining state-of-the-art ACPR (better than -67 dBc) while complying

with specifications for WBN (−80 dBc at 500 kHz, −95 dBc at 5 MHz) and EVM (10%). As such, the overall system solution appears to be a viable candidate for future TEDS base-station production designs.

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Carrier Distortion in Hysteretic Self-Oscillating Class-D Audio Power Amplifiers: Analysis and Optimization

Mikkel C. W. Høyerby, *Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—An important distortion mechanism in hysteretic self-oscillating (SO) class-D (switch mode) power amplifiers—carrier distortion—is analyzed and an optimization method is proposed. This mechanism is an issue in any power amplifier application where a high degree of proportionality between input and output is required, such as in audio power amplifiers or xDSL drivers. From an average-mode point of view, carrier distortion is shown to be caused by nonlinear variation of the hysteretic comparator input average voltage with the output average voltage. This easily causes total harmonic distortion figures in excess of 0.1–0.2%, inadequate for high-quality audio applications. Carrier distortion is shown to be minimized when the feedback system is designed to provide a triangular carrier (sliding) signal at the input of a hysteretic comparator. The proposed optimization method is experimentally proven in an audio power amplifier leading to THD figures that are comparable to the state of the art. Experimental hardware is a hysteretic SO bandpass current-mode-controlled single-ended audio power amplifier capable of 45 W into 8 Ω or 80 W into 4 Ω from a ±34 V supply with less than 0.03% THD from 100 Hz to 6.7 kHz. Carrier distortion is shown to account for this limitation in THD performance.**

***Index Terms*—Audio, class-D, hysteretic, power amplifier, sliding.**

I. Introduction

SWITCH-MODE (class D) audio power amplifiers have been a commercial success over the past decade, replacing traditional linear (class A/AB/B) amplifiers in many applications. The main driver has been the reduction in physical size resulting from the increased efficiency [1].

It is generally well understood that errors in the switching stage of the class-D amplifier can introduce significant harmonic distortion to the amplifier output [1]–[3]. However, with the ever-increasing performance of modern power MOSFETs, the significance of switching stage errors diminishes [4], [5]. As a result, the distortion generated by the pulsewidth modulation (PWM) and control process itself becomes visible. An excellent illustration of this is given in [5], where the distortion generated by the injection of switching ripple components from the feedback circuitry into the PWM is analyzed by the use of discrete-time system theory. As presented, this analysis is only applicable to clocked/driven control systems, such as those based on the traditional triangle-and-comparator PWM.

For self-oscillating (SO) control systems, which have been successfully commercialized [6] for class-D audio, details on the distortion generated by the modulation and control process are more scarce, although a very good example is given in [7] for SO systems without comparator hysteresis. However, design suggestions on how to affect the amount of distortion generated by the modulation process are not offered, nor does the analysis directly apply to SO systems with comparator hysteresis. For these systems, only a few hints on optimizing modulation linearity are offered [8]–[10].

This paper examines distortion generated by the modulation process in the hysteretic SO class of control systems, a class that has yielded some of the most impressive [9], [11] THD figures published for switch-mode audio power amplifiers. The analysis is carried out using the well-established average modeling approach, leading to an optimization method proposal that is consistent with prior art findings, and complemented by experimental results on a representative, nontrivial, hysteretic SO class-D audio power amplifier. Although this paper is focused on audio power amplification, other applications exist where accurate amplification of ac signals is required. One example is various digital subscriber line (xDSL) drivers [7], where high output spectral purity is required. Another example is tracking power supplies in high-efficiency RF power amplification systems [12]. Here, the tracking power supply in some schemes directly modulates the output of an RF power amplifier, adding any distortion introduced by the tracking power supply to the RF power amplifier output. A final example is ac transmission systems [13], [14].

II. Hysteresis-Based SO Controllers

The hysteresis-based SO controllers reviewed in this paper can be considered a small, low-complexity subset of the very large set of sliding-mode control (SMC) systems. For audio power amplification using a single-phase buck-type power stage, the hysteretic SO control system will generally contain one comparator with hysteresis, which, based on a linear combination of system states and the audio input, selects one of the two possible switching states (high/low) for the power stage.

A very simple but applicable example of such a control system is the astable integrating multivibrator (AIM) [8], [15] shown in Fig. 1. Capable of good results [8] in practice, it has the

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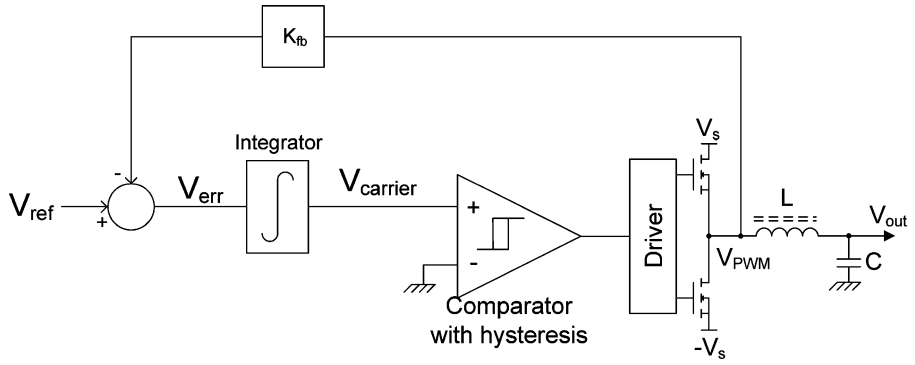

Fig. 1. Simple hysteretic SO audio power amplifier example—the AIM [8], [15].

disadvantage of not having feedback around the output filter, increasing the impact of the output filter design on amplifier distortion levels, output impedance, and frequency response [6], [9], [11]. Several alternative hysteretic SO controller implementations have been proposed in the context of audio power amplification, where the main difference lies in the way in which the output inductor current is effectively fed back, since this is the most difficult system state to measure. Some solutions opt for feeding back the output capacitor current instead, since this is the same as the inductor current with output current feedforward added [16]. The capacitor current can either be estimated by differentiation of the capacitor voltage [9], [17] and added to the raw capacitor voltage as done by proportional-derivative (PD) feedback, or measured directly with a current sense transformer [11], [18]. Alternatively, the inductor current can be estimated by low-pass filtering of the inductor voltage [10], effectively leading to bandpass current control [19]. In all cases, the use of postfilter feedback generally serves to lessen the negative effects of the output filter. Many very similar solutions have appeared in the somewhat wider context of single-phase buck dc/dc converters, where PD-based capacitor voltage feedback is richly represented [20]–[23] along with capacitor current feedback [24], [25] and direct inductor current feedback [26]. It has also been shown that the equivalent series resistance of the output capacitor can be usefully incorporated into the capacitor current estimation system [27], relaxing the demands on the differentiation circuitry.

At this time, it is useful to formally define the class of systems studied as any system with a hysteretic comparator driving a linear time-invariant system with relevant feedback and reference inputs added, as shown in Fig. 2. Of particular interest, it turns out, is the generation of the carrier signal (V_{carrier}), which is described by the effective controller transfer function (a.k.a. "loop filter" [5]), $G_{\mathrm{ctrl}}(s)$:

$$G_{\mathrm{ctrl}}(s) \equiv \frac{V_{\mathrm{carrier}}(s)}{V_{\mathrm{PWM}}(s)} \tag{1}$$

These generalizations allow all of the aforementioned systems to be represented, and are often adopted in prior art [28]–[30].

As sliding mode controllers, extensive theory [31] exists for dealing with the stability and dynamics of hysteretic SO controllers. In the application of controlling simple switch-mode power converters, classical sliding mode theory is based on the assumption

$$V_{\mathrm{carrier}} = 0 \tag{2}$$

where V_{carrier} is the input to the hysteretic comparator, generally known as the "sliding variable" in SMC context or the "carrier signal" in SO control context. This approximation can be very useful [32], but also has its shortcomings [16]. For the presented study of linearity and distortion in sliding mode controllers, it is absolutely essential to depart from this basic assumption. The carrier voltage is still usefully described as *almost* zero, but the implications of "almost" need to be considered

$$V_{\mathrm{carrier}} \approx 0 \tag{3}$$

Prior art has demonstrated several examples of this; a nonzero carrier average was used in [33] to assign a low-frequency gain to the hysteretic comparator, and it is well known [34] that a describing function can be used to find its gain at the switching/oscillation frequency of the control loop. These two methods can even be combined to yield an estimated, but still quite accurate, transfer function for the hysteretic comparator [35]. A nonzero carrier average caused by delays in the comparator and power stage is shown in [36] to lead to inaccuracy in the average output current of a hysteretic current control loop. In the following, the effects of nonzero carrier average caused by the properties of $G_{\mathrm{ctrl}}(s)$ are examined.

III. Carrier Distortion

The carrier distortion [8] mechanism in hysteretic SO controllers is claimed [8]–[10] to be a function of the shape of the carrier signal waveform, with a triangular waveform being the optimum. In order to properly explain this proposed distortion mechanism, it is useful to examine the simplest conceivable hysteretic SO control system: the AIM. The approach adopted is to analyze the average (dc) carrier voltage variation with the amplifier dc operating point, expressed as a steady-state duty cycle D for different degrees of integrator ideality. Under the assumption of quasi-stationary behavior, the dc characteristics of the loop will also apply at audio frequencies [5]. Practically, the integrator in the AIM is replaced with a pole and a gain to provide variable carrier signal "straightness" in a way that is simple enough to allow exact analysis. With this imperfect

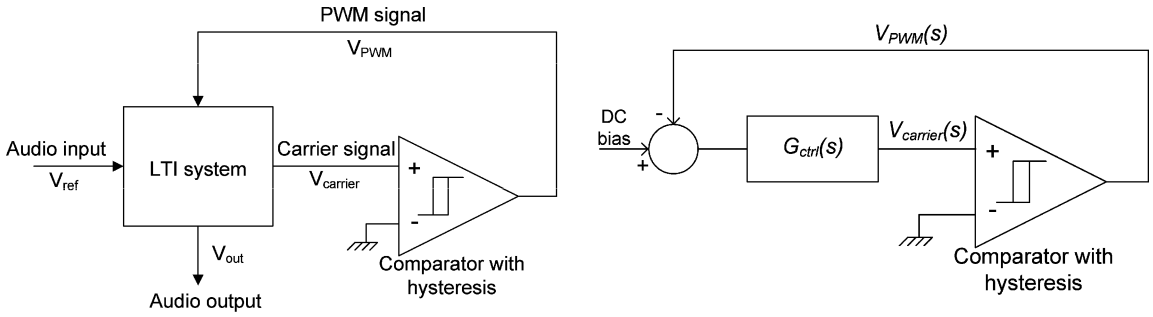

Fig. 2. Generalized views of hysteretic SO control systems for audio applications. (a) Overall system. (b) Carrier generation process.

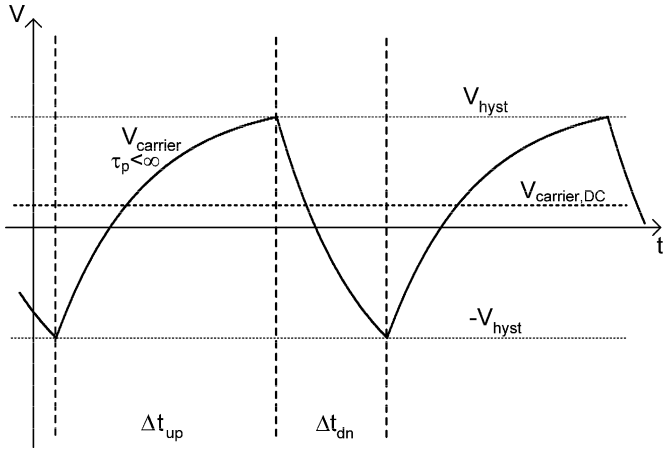

Fig. 3. AIM carrier waveform ($D = 1/3$) with single-pole $G_{\mathrm{ctrl}}(s)$ as considered for carrier distortion analysis. $V_{\mathrm{carrier,dc}}$is the average of the carrier waveform, which evidently can be nonzero in spite of a symmetrical hysteresis window $\pm V_{\mathrm{hyst}}$ and zero delay.

integrator, a representative example of the carrier signal in the AIM is shown in Fig. 3. Note that zero time delay in the comparator and power stage has been assumed for the analysis performed hereafter. $\pm V_{\mathrm{hyst}}$ denotes the hysteresis window. Likewise, it has been assumed that $V_s = 1$ and $K_{fb} = 1$ in order to clarify the analysis.

The AIM loop integrator is replaced with the transfer function $G(s)$, which also becomes the $G_{\mathrm{ctrl}}(s)$ of the system

$$G(s) = G_{\mathrm{ctrl}}(s) = \frac{G_p}{1 + s\tau_p} \tag{4}$$

Note that G_p is a gain that numerically equals τ_p, a distinction made to avoid unit confusion in the following analysis. The purpose of this particular choice of G_p is to ensure that $G_{\mathrm{ctrl}}(s)$ converges toward the ideal integrator when τ_p is made large

$$\lim_{\tau_p \to \infty} G_{\mathrm{ctrl}}(s) = \frac{1}{s} \tag{5}$$

The step response of $G_{\mathrm{ctrl}}(s)$ is given by

$$\mathrm{step}\{G_{\mathrm{ctrl}}(s)\} = G_p(1 - e^{-(t/\tau_p)}) \tag{6}$$

Assuming that the feedback system has high loop gain, the steady-state PWM voltage per-cycle average will represent the reference voltage exactly

$$\langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} = V_{\mathrm{ref}} \tag{7}$$

This allows the reference voltage to be expressed by the PWM signal steady-state duty cycle D

$$\langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} = 2(D-1) \Rightarrow V_{\mathrm{ref}} = 2(D-1) \tag{8}$$

The input to the loop filter is given by

$$V_{\mathrm{err}} = V_{\mathrm{ref}} - V_{\mathrm{PWM}} = \begin{cases} V_{\mathrm{ref}} + 1, & V_{\mathrm{PWM}} = -1 \\ V_{\mathrm{ref}} - 1, & V_{\mathrm{PWM}} = 1 \end{cases} \tag{9}$$

This can be rewritten as

$$V_{\mathrm{err}} = \begin{cases} 2D, & V_{\mathrm{PWM}} = -1 \\ 2(D-1), & V_{\mathrm{PWM}} = 1 \end{cases} \tag{10}$$

In this case, D and $(D-1)$ both stringently have the unit of V. Since the PWM signal can be considered as a series of step functions, a segment of the carrier voltage can be found by using the step response of $G_{\mathrm{ctrl}}(s)$ and observing that an initial value has to be added to reflect the presence of the hysteresis window $\pm V_{\mathrm{hyst}}$. The carrier voltage will change exponentially with time constant τ_p and initial and final values as given in Table I.

TABLE I
CARRIER SIGNAL INITIAL/FINAL CONDITIONS IN AIM WITH IMPERFECT INTEGRATOR

PWM level	Initial (t=0) value	Final (t=∞) value
$V_{PWM} = -1$	$-V_{hyst}$	$2 \cdot D \cdot G_p$
$V_{PWM} = 1$	V_{hyst}	$2 \cdot (D-1) \cdot G_p$

The carrier voltage can thus be described as

$$V_{\mathrm{carrier}}(t) = \begin{cases} -V_{\mathrm{hyst}} + (2DG_p + V_{\mathrm{hyst}})\left(1 - e^{-(t/\tau_p)}\right), & V_{\mathrm{PWM}} = -1 \\ V_{\mathrm{hyst}} + (2(D-1)G_p - V_{\mathrm{hyst}})\left(1 - e^{-(t/\tau_p)}\right), & V_{\mathrm{PWM}} = 1 \end{cases} \tag{11}$$

The up/down-slope periods Δt_{up} and Δt_{dn} can now be found by adding the boundary condition of the carrier signal hitting the hysteresis window, leading to the equations

$$\begin{aligned} &-V_{\mathrm{hyst}} + (2DG_p + V_{\mathrm{hyst}})\left(1 - e^{-(\Delta t_{\mathrm{up}}/\tau_p)}\right) = V_{\mathrm{hyst}} \wedge V_{\mathrm{hyst}} \\ &+ (2(D-1)G_p - V_{\mathrm{hyst}})\left(1 - e^{-(\Delta t_{\mathrm{dn}}/\tau_p)}\right) = -V_{\mathrm{hyst}} \end{aligned} \tag{12}$$

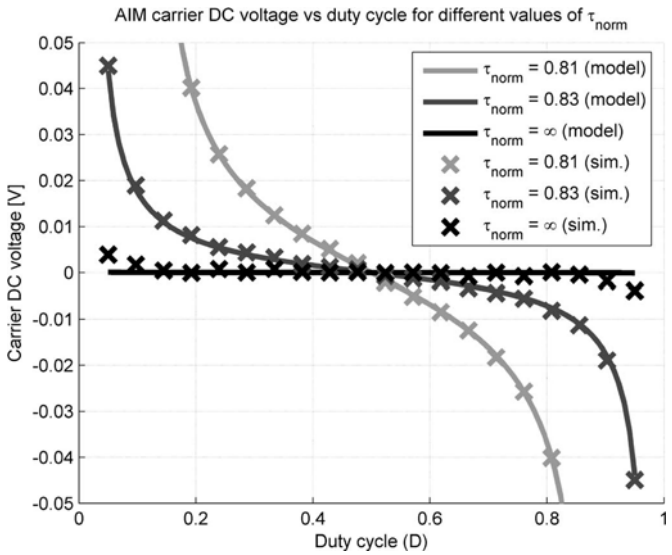

Fig. 4. Modeled (16) and simulated carrier dc voltages plotted for variable duty cycle. Modeled results match simulated results very well.

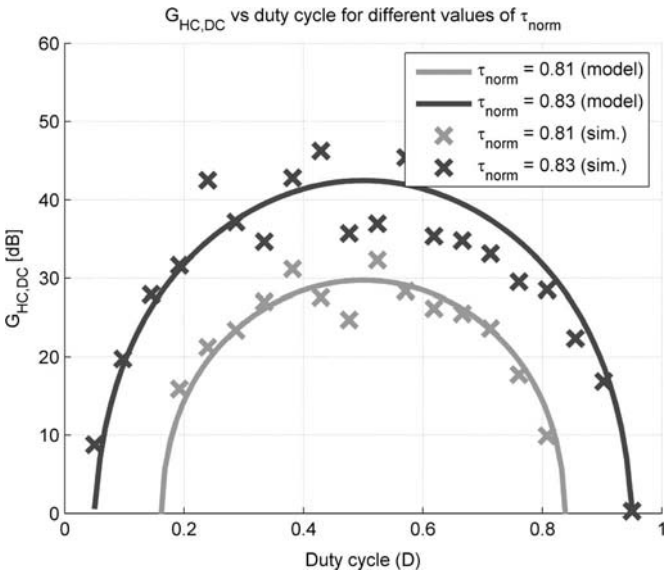

Fig. 5. Modeled [using numerical evaluation of (17)] and simulated hysteretic comparator dc gain $G_{\mathrm{HC,dc}}$. Deviation from the ideal loop filter ($\tau_p = \infty$) causes reduction and nonlinearity in $G_{\mathrm{HC,dc}}$. Results for $\tau_p = \infty$ would be a horizontal line at $G_{\mathrm{HC,dc}} = \infty$. The nonlinearity is symmetrical around $D = 0.5$, so only odd harmonic distortion is produced.

These equations can be solved easily, leading to

$$\begin{aligned}\Delta t_{\mathrm{up}} &= -\tau_p \ln\left(1 - \frac{2V_{\mathrm{hyst}}}{2DG_p + V_{\mathrm{hyst}}}\right) \wedge \Delta t_{\mathrm{dn}} \\ &= -\tau_p \ln\left(1 - \frac{2V_{\mathrm{hyst}}}{2\left(1-D\right)G_p + V_{\mathrm{hyst}}}\right) \end{aligned} \tag{13}$$

In order to provide a more general view of the influence of τ_p on system behavior, τ_p can be normalized to the nominal ($D = 0.5$) switching period ($T_{\mathrm{sw,nom}}$) of the loop

$$\tau_{\mathrm{norm}} = \frac{\tau_p}{T_{\mathrm{sw,nom}}} = \left.\frac{\tau_p}{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}}\right|_{D=0.5} \tag{14}$$

Now, the only problem is to find the average (dc) value of the carrier voltage with the given variables. This is done by calculating the per-cycle average of the carrier by integrating the carrier voltage over one switching period

$$V_{\mathrm{carrier,dc}}\left(D\right) = \frac{1}{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}} \int_0^{\Delta t_{\mathrm{up}} + \Delta t_{\mathrm{dn}}} V_{\mathrm{carrier}}\left(t\right)\, dt \tag{15}$$

Solving this integral (Mathematica was used for symbolic solution) results in (16) as shown at the bottom of this page.

This expression is best analyzed by plotting the expression output for different parameter inputs as in Fig. 4. It is obvious that the carrier dc voltage varies with D in a nonlinear manner when the loop filter is not an integrator. If τ_p approaches infinity, this expression can be shown to converge toward zero. Since the gain of the hysteretic comparator can be defined as

$$\begin{aligned} G_{\mathrm{HC,dc}}\left(D\right) &\equiv \frac{\left(\left(\partial \left\langle V_{\mathrm{PWM}}\right\rangle_{T_{\mathrm{sw}}}\right)/\partial D\right)}{\left(\left(\partial V_{\mathrm{carrier,dc}}\left(D\right)\right)/\partial D\right)} \\ &= \frac{2}{\left(\left(\partial V_{\mathrm{carrier,dc}}\left(D\right)\right)/\partial D\right)} \end{aligned} \tag{17}$$

it is also obvious that the hysteretic comparator exhibits a nonconstant gain at dc. In other words, a nonlinear element has been introduced into the loop, leading to harmonic distortion. This distortion generated by the nonlinear variation of $V_{\mathrm{carrier,dc}}$ with D is exactly what has previously been named *carrier distortion.*

For the AIM with the considered, imperfect loop filter, even with all the simplifications made (zero time delay, only dc considered), the analytical expression for $G_{\mathrm{HC,dc}}$ gets too complicated to be of real value, so numerical differentiation was used for finding the carrier dc voltage derivative. Analytical and simulated values of $G_{\mathrm{HC,dc}}$ are shown in Fig. 5. Since $V_{\mathrm{carrier,dc}}(D)$ is generally larger and more variable for smaller values of τ_{norm}, the dc gain of the hysteretic comparator also decreases with τ_{norm}. Since the average of a perfectly triangular carrier oscillating within $\pm V_{\mathrm{hyst}}$ is zero, the dc gain of the hysteretic comparator could theoretically be infinite. In practice, time delay in the comparator (and power stage) ensures that this never happens [33], [35].

In order to evaluate the effect of the found variation of $V_{\mathrm{carrier,dc}}$ with D on amplifier distortion, the system is modeled as shown in Fig. 6.

$$V_{\mathrm{carrier,dc}}\left(D\right) = -2G_p \frac{\left(1-D\right)\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_p\left(1-D\right) + V_{\mathrm{hyst}}\right)\right)\right) - D\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_pD + V_{\mathrm{hyst}}\right)\right)\right)}{\ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_p\left(1-D\right) + V_{\mathrm{hyst}}\right)\right)\right) + \ln\left(1 - \left(2V_{\mathrm{hyst}}/\left(2G_pD + V_{\mathrm{hyst}}\right)\right)\right)} \tag{16}$$

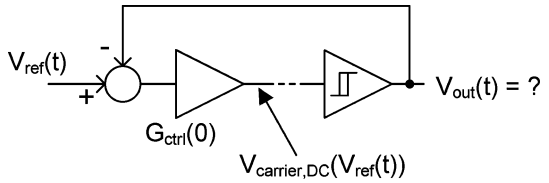

Fig. 6. Model of the AIM loop used for determination of output voltage waveform when taking carrier distortion into consideration. Reference signal $V_{\mathrm{ref}}(t)$ is assumed to be dc or "almost dc."

The output of the AIM model in Fig. 6 is given by

$$V_{\mathrm{out}}(t) = V_{\mathrm{ref}}(t) - \frac{V_{\mathrm{carrier,dc}}(V_{\mathrm{ref}}(t))}{G_{\mathrm{ctrl}}(0)} \tag{18}$$

The output, V_{out} is here formally defined as the per-(switch)-cycle average PWM voltage

$$V_{\mathrm{out}} \equiv \langle V_{\mathrm{PWM}} \rangle_{T_{\mathrm{sw}}} \tag{19}$$

Assuming that the output voltage has relatively low distortion, the D of the AIM will be determined almost exclusively by V_{ref}. Thus, for a given V_{ref}, D is approximated as

$$D = \frac{1}{2}(V_{\mathrm{ref}} + 1) \tag{20}$$

For a sinusoidal input

$$V_{\mathrm{ref}}(t) = M \sin(2\pi f_{\mathrm{ref}} t) \tag{21}$$

the duty cycle is therefore approximated as

$$D(t) = \frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1] \tag{22}$$

Note that since the studied AIM has a reference-to-output gain of unity and conceptually operates from 1 V supplies, the amplitude M of the sine wave corresponds to the modulation index of the PWM signal. The peak duty cycle $D_{\max}$ and the modulation index M are generally related as follows:

$$D_{\max} = \frac{1}{2}(1 + M) \tag{23}$$

Thus, the output of the AIM is

$$V_{\mathrm{out}}(t) = \frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1] - \frac{V_{\mathrm{carrier,dc}}\left(\frac{1}{2}[M \sin(2\pi f_{\mathrm{ref}} t) + 1]\right)}{G_{\mathrm{ctrl}}(0)} \tag{24}$$

This expression is best evaluated numerically, yielding the averaged output of the AIM, complete with carrier distortion. As shown in the calculated example waveforms in Fig. 7, the distortion generated by using a pole as a loop filter in the AIM is of expansive character, causing the peaks of the reference signal to come out at a higher level than desired. This is perhaps surprising, since $G_{\mathrm{HC,dc}}$ is reduced at high D. However, this compressive action is more than counteracted by the requirement for a specific carrier dc voltage $V_{\mathrm{carrier,dc}}$ to be present for a given D. As an example, assume that the reference is $+0.5$. The loop will attempt to establish a D of 0.75, but looking at Fig. 4, the carrier voltage must contain a small,

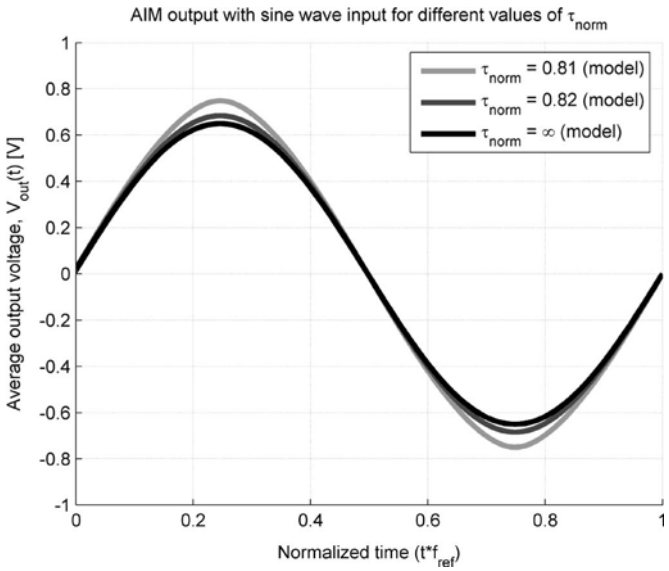

Fig. 7. Calculated AIM output with values of $\tau_{\mathrm{norm}}\,(M = 0.65)$. Carrier distortion caused by small time constants causes signal expansion at high output levels.

negative dc component. Looking at Fig. 6, this can only be produced by an output dc voltage that is slightly higher than prescribed by the reference, causing the expansion effect apparent in Fig. 7.

From the AIM output, harmonic distortion products are found by Fourier analysis. The output waveform is expressed by the Fourier series (with complex coefficients) given by

$$c_{\mathrm{out},n} = f_{\mathrm{ref}} \int_{t=0}^{t=(1/f_{\mathrm{ref}})} V_{\mathrm{out}}(t)\, e^{-j2\pi f_{\mathrm{ref}} n}\, dt \tag{25}$$

where $|c_{\mathrm{out},1},|$ corresponds to the fundamental amplitude, $|c_{\mathrm{out},3},|$ corresponds to the third-harmonic distortion product, etc. The THD generated by carrier distortion can be calculated from these numbers by evaluating the following expression:

$$\mathrm{THD} = \frac{\sqrt{|c_{\mathrm{out},2}|^2 + |c_{\mathrm{out},3}|^2 + \cdots + |c_{\mathrm{out},n}|^2}}{|c_{\mathrm{out},1}|} \tag{26}$$

In practice, the following expression is a good approximation since there are no even harmonics:

$$\mathrm{THD} \approx \frac{\sqrt{|c_{\mathrm{out},3}|^2 + |c_{\mathrm{out},5}|^2 + \cdots + |c_{\mathrm{out},n}|^2}}{|c_{\mathrm{out},1}|} \tag{27}$$

In the studied AIM example, we numerically evaluate harmonics and THD from the derived analytical expressions and compare them with simulations results in the numbers shown in Figs. 8–11. It is evident that the analysis approach shown is capable of describing the carrier distortion mechanism very well. It is also evident that this mechanism can easily produce significant harmonic distortion in an amplifier with a perfect power stage with stiff supply voltage, and no delay and no dead-time distortion, justifying the analysis performed. Finally, the generated distortion exhibits strong variation with τ_{norm} in the area of 0.80–0.85. This simply reflects that the first segment (well

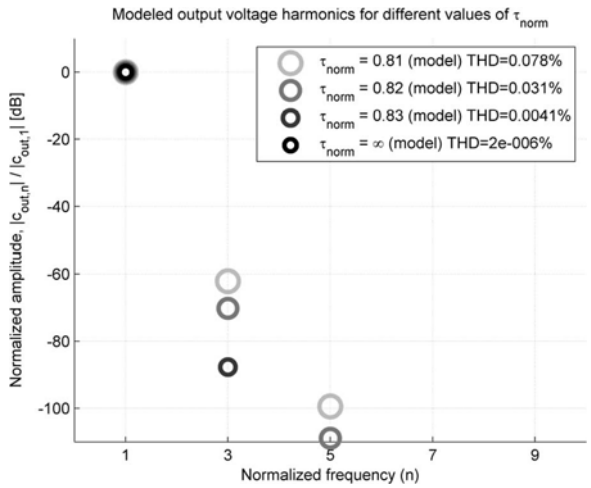

Fig. 8. Output harmonics from AIM found by calculation; $M = 0.2$.

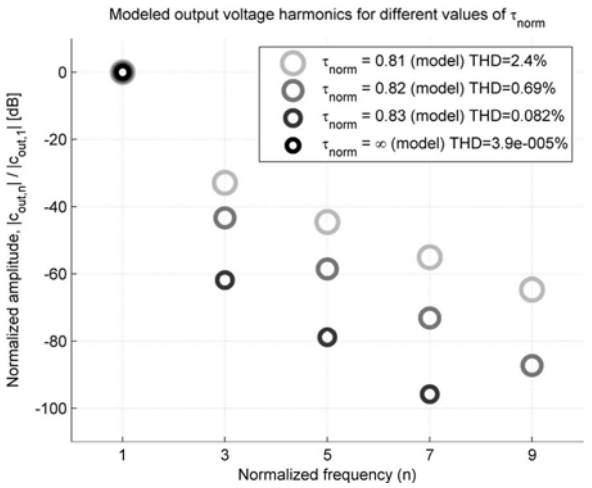

Fig. 10. Output harmonics from AIM found by calculation; $M = 0.65$.

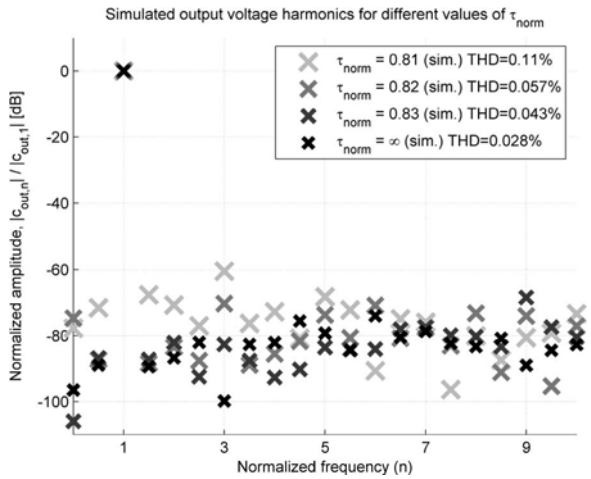

Fig. 9. Output harmonics from AIM found by simulation; $M = 0.2$.

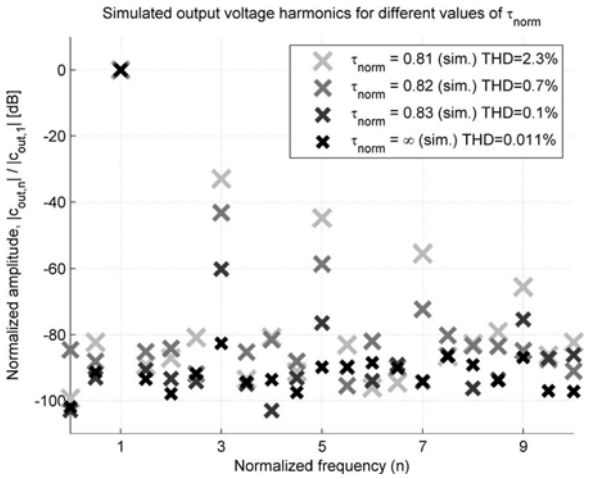

Fig. 11. Output harmonics from AIM found by simulation; $M = 0.65$.

below $t = \tau_p$) of an exponentially shaped carrier has almost-constant slope, with curvature becoming significantly closer to τ_p.

Several implications result from this analysis. First, it allows for proper explanation of the carrier distortion phenomenon by reference to the average modeling technique used. The explanation offered is that a nontriangular carrier signal (the result of not having an integrator-type $G_{\mathrm{ctrl}}(s)$) requires voltages that are a nonlinear function of the reference voltage to be present at the hysteretic comparator input, directly causing distortion, and in the process causing the hysteretic comparator to exhibit a nonconstant small-signal dc gain. Second, it allows the amount of carrier distortion in a class-D audio amplifier design to be predicted analytically from data on the carrier signal dc voltage. This is useful information in that it provides a designer with a tool for determining just how "perfect" the carrier signal should be to meet a target THD specification without time-consuming, repetitive simulations of multiple reference signal periods. Finally, the analysis supports statements in prior art [8] claiming that the carrier signal should be triangular (resulting from the use of an integrator as loop filter in the AIM), arguing from the point of view that the carrier voltage dc component should be a linear function of duty cycle to avoid causing nonlinearity. It is then taken as a trivial matter to show that a perfectly triangular carrier oscillating between $\pm/- V_{\mathrm{hyst}}$ has to have an average of zero for any D.

IV. Carrier Distortion Optimization

The previous section provided an analytical justification for pursuing a triangular carrier signal. In an AIM, this is easy; any practical operational amplifier has enough dc gain for realizing a loop filter that sufficiently resembles an integrator. In other feedback configurations, however, the problem is much more severe. For example, considering the hysteretic bandpass current-mode (BPCM) control topology demonstrated in [10] (and illustrated in Fig. 12), it is not obvious how to make the output of the combined voltage and current estimate feedbacks respond with a ramp to a step input, except perhaps by perfect estimation of the inductor current and removal of the output voltage feedback. This would make the amplifier a current source instead of the desired voltage source. The hysteretic BPCM topology has still been demonstrated to be capable of very good THD figures

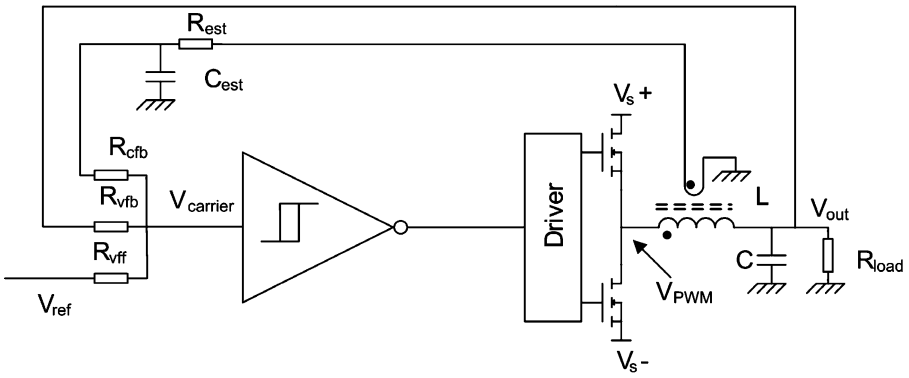

Fig. 12. Simple single-ended BPCM amplifier implementation [10].

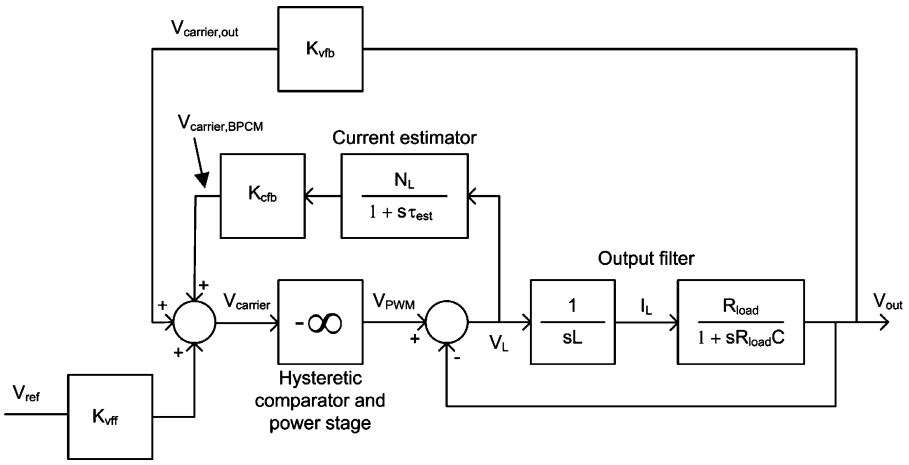

Fig. 13. Small-signal model of BPCM amplifier [10] using infinite-gain (equivalent to assuming sliding-mode operation [23], [31]) hysteretic comparator model.

(0.01%–0.03% range) with a modest control system complexity. It is a dual-loop feedback system, which incorporates the output filter dynamics, making the loop design nontrivial in comparison with the AIM. As such, it is an ideal test vehicle for the demonstration of a new analytical carrier distortion minimization technique based on the pursuit of a triangular carrier signal.

The carrier linearization approach that is proposed has the objective of shaping the step response of $G_{\mathrm{ctrl}}(s)$ as a ramp. The proposed method for minimization and evaluation of carrier distortion is simply as follows.

1) Compute the step response of $G_{\mathrm{ctrl}}(s)$ analytically.
2) Compute second (time-) derivative of $G_{\mathrm{ctrl}}(s)$ step response.
3) Use second derivative to find criteria for ensuring constant-sloping step response.
4) Use found criteria to design control loop.
5) Optional: fine-tune design by iterative simulations.
6) Optional: Evaluate $V_{\mathrm{carrier,dc}}(D)$ of design and determine carrier distortion-caused THD.

Step 3 is the main part of the method--since a constant-sloping (carrier) signal is characterized by its second derivative being zero, forcing the second derivative of the carrier signal response to a PWM step to be zero should lead to a constant-sloping (linear) carrier signal. Step 5 is typically the only tool available. It has been included since a number of approximations must be made when computing the step response of $G_{\mathrm{ctrl}}(s)$, resulting in a design that may be slightly suboptimal. Still, the proposed method saves considerable design time by reducing the number of iterative simulations required or removing these completely. Step 6 allows for a prediction of the minimum level of THD that can be expected from the optimized design, providing a second-source reference for comparison with simulated THD. The remaining parts of this section illustrate the proposed approach with the BPCM-controlled amplifier. Fig. 13 shows how the BPCM amplifier may be broken down to block diagram form, with relevant parameters summarized in Table II.

For the carrier generation, the contributions from two feedback paths (current estimate and output voltage) can be expressed by the following transfer functions:

$$G_{\mathrm{BPCM}}(s) \equiv \frac{V_{\mathrm{carrier,BPCM}}(s)}{V_{\mathrm{PWM}}(s)} = K_{\mathrm{cfb}} \times \frac{N_L}{1+s\tau_{\mathrm{est}}} \times \frac{1}{s^2LC + (L/R_{\mathrm{load}})s + 1} \times sL \times \frac{1+sR_{\mathrm{load}}C}{R_{\mathrm{load}}}$$

$$G_{\mathrm{out}}(s) \equiv \frac{V_{\mathrm{carrier,out}}(s)}{V_{\mathrm{PWM}}(s)} = K_{\mathrm{vfb}} \times \frac{1}{s^2LC + (L/R_{\mathrm{load}})s + 1} \tag{28}$$

TABLE II
PARAMETERS IN HYSTERETIC BPCM AMPLIFIER MODEL

Load resistance	R_{load}
Output filter capacitance	C
Output filter inductance	L
Inductor sense winding ratio	N_L
Current estimator time constant	τ_{est}
Current feedback coefficient	K_{cfb}
Voltage feedback coefficient	K_{vfb}
Reference feed-forward coefficient	K_{vff}

From these transfer functions, $G_{\mathrm{ctrl}}(s)$ is found to be

$$G_{\mathrm{ctrl}}(s) = \frac{V_{\mathrm{carrier,BPCM}}(s) + V_{\mathrm{carrier,out}}(s)}{V_{\mathrm{PWM}}(s)} = \frac{1}{s^2 LC + s(L/R_{\mathrm{load}}) + 1} \times \left[K_{\mathrm{cfb}} \frac{N_L}{1 + s\tau_{\mathrm{est}}} \frac{sL\,(sR_{\mathrm{load}}C + 1)}{R_{\mathrm{load}}} + K_{\mathrm{vfb}} \right] \quad (29)$$

Obviously, this transfer function cannot be reduced to a simple integrator provided that the poles of the output filter are complex and that $\tau_{\mathrm{est}} < \infty$, thus making the carrier optimization nontrivial as previously stated. With the output filter transfer function $G_{\mathrm{filter}}(s)$ as a factor in $G_{\mathrm{ctrl}}(s)$, it makes sense to start by computing the step response of the output filter transfer function, $G_{\mathrm{filter}}(s)$, given as

$$G_{\mathrm{filter}}(s) = \frac{1}{s^2 LC + s(L/R_{\mathrm{load}}) + 1} \quad (30)$$

Assuming R_{load} to be very high (a "high-Q" approximation), this simplifies to

$$G_{\substack{\mathrm{filter} \\ Q>>1}}(s) \approx \frac{1}{s^2 LC + 1} = \frac{\sqrt{(1/LC)}}{s^2 + \sqrt{(1/LC)}} \quad (31)$$

Combining this with the Laplace transform of a step function ($1/s$) results in an expression that can be easily reverse Laplace transformed. The response of the output voltage to a PWM voltage step is hereby found to be

$$V_{\mathrm{out,step}}(t) = \ell^{-1}\left\{ \frac{1}{s} \times \frac{\sqrt{(1/LC)}}{s^2 + \sqrt{(1/LC)}} \right\} = 1 - \cos\left(\frac{1}{\sqrt{LC}} t \right) \quad (32)$$

The output voltage feedback component of the carrier signal thus exhibits the following step response:

$$V_{\mathrm{carrier,out,step}}(t) = K_{\mathrm{vfb}} \left[1 - \cos\left(\frac{1}{\sqrt{LC}} t \right) \right] \quad (33)$$

The current estimator output can be usefully reexpressed as

$$V_{\mathrm{carrier,BPCM}}(s) = V_{\mathrm{PWM}}(s)\,[1 - G_{\mathrm{filter}}(s)]\,\frac{K_{\mathrm{cfb}} N_L}{1 + s\tau_{\mathrm{est}}} \quad (34)$$

Note that at the frequencies of interest for carrier shaping (frequencies in the range around the switching frequency), $G_{\mathrm{filter}}(s)$ is negligible compared to 1 (the filter cutoff can be more than a decade away from the switching frequency), allowing this contribution to be neglected. Practically, this corresponds to assuming the output voltage to be constant, i.e., free from switching ripple. This is also intuitively reasonable since the ac component in the PWM signal will be much larger than the ripple voltage in any practical design. Therefore

$$V_{\mathrm{carrier,BPCM}}(s) \approx V_{\mathrm{PWM}}(s)\,K_{\mathrm{cfb}} \times \frac{N_L}{1 + s\tau_{\mathrm{est}}} \quad (35)$$

The response of the BPCM component of the carrier to a PWM step is hereby

$$V_{\mathrm{carrier,BPCM,step}}(t) = \ell^{-1}\left\{ \frac{1}{s} \times K_{\mathrm{cfb}} \times \frac{N_L}{1 + s\tau_{\mathrm{est}}} \right\} \quad (36)$$

Again, doing a reverse Laplace transformation, this can be reexpressed as

$$V_{\mathrm{carrier,BPCM,step}}(t) = K_{\mathrm{cfb}} \times N_L \times \left[1 - e^{-\tau_{\mathrm{est}} t} \right] \quad (37)$$

Hereby, it has been found that the carrier response to a PWM voltage step is approximately

$$V_{\mathrm{carrier,step}}(t) \equiv \mathrm{step}\,\{G_{\mathrm{ctrl}}(s)\} \approx K_{\mathrm{vfb}} \left[1 - \cos\left(\frac{1}{\sqrt{LC}} t \right) \right] + K_{\mathrm{cfb}} N_L \left[1 - e^{-\tau_{\mathrm{est}} t} \right] \quad (38)$$

Now, the carrier signal slope can expressed as

$$\dot{V}_{\mathrm{carrier,step}}(t) = \frac{K_{\mathrm{vfb}}}{\sqrt{LC}} \sin\left(\frac{1}{\sqrt{LC}} t \right) + \frac{K_{\mathrm{cfb}} N_L}{\tau_{\mathrm{est}}} \times e^{-\tau_{\mathrm{est}} t} \quad (39)$$

To ensure that this signal has a constant slope (at least over a brief time horizon following the step), the following optimality criterion is applied as per step 3) in the optimization method:

$$\ddot{V}_{\mathrm{carrier,step}}(0) = 0 \quad (40)$$

Of course, it would be preferable to demand this for all time instances--but this cannot be solved for the BPCM control system since only an integrator has an ideal, constant-sloping step response and $G_{\mathrm{ctrl}}(s)$ of the BPCM amplifier is indeed not an integrator. It should also be noted that this criterion is only useful in a controller structure that is actually capable of producing a triangular carrier signal. This will be the case if the inductor current, or a high-frequency estimate of this is fed back, since the inductor current is (almost) triangular, especially at high switching frequencies. Differentiating the carrier slope leads to

$$\ddot{V}_{\mathrm{carrier,step}}(t) = \frac{K_{\mathrm{vfb}}}{LC} \cos\left(\frac{1}{\sqrt{LC}} t \right) - \frac{K_{\mathrm{cfb}} N_L}{\tau_{\mathrm{est}}^2} \times e^{-\tau_{\mathrm{est}} t} \quad (41)$$

Applying the optimality criterion results in the following simple expression that should be satisfied for an optimal design of the considered BPCM controller:

$$\frac{K_{\mathrm{vfb}}}{LC} = \frac{K_{\mathrm{cfb}} \times N_L}{\tau_{\mathrm{est}}^2} \quad (42)$$

TABLE III
PROTOTYPE BPCM AMPLIFIER DESIGN CONSTANTS

Component	*Value*
L	*20.25μH*
C	*2μF*
N_L	*2:9*
τ_{est}	*3.3μs*

V. EXAMPLE PROTOTYPE AMPLIFIER DESIGN

To demonstrate the usefulness of the proposed optimization method, a practical amplifier design is considered. Initial design constants are summed up in Table III. The design considered is single-ended and based on the use of 100-V switching components and a 20.25-μH dual-winding power inductor on a gapped RM10 ferrite core, combined with 2 μF of output capacitance. For the typical speaker load of 4–8 Ω, this leads to a minimum filter Q of 1.26, not exactly infinite as approximated, but still underdamped. The current estimator time constant ($\tau_{\rm est}$) was set at 3.3 μs, realized with $R_{\rm est} = 100\ \Omega$ and $C_{\rm est} = 33$ nF.

In order to increase the amplifier immunity to low-frequency supply voltage perturbations, as well as to help establish the carrier voltage dc operating point, the basic BPCM control system is augmented with a parallel integrating control loop as shown in Fig. 14. Equation (42) can still be used to predict the optimum feedback coefficients given that the integrator time constant is kept slow enough compared to the switching frequency, which ensures that the $G_{\rm ctrl}(s)$ step response is not significantly influenced within a time frame of one switching cycle. Note that the paralleling of proportional and integral output voltage feedback effectively provides PI output voltage feedback, hence the term BPCM + PI used for describing this topology. In the implementation shown, the comparator and the operational amplifier run off a single +5 V supply ($V_{\rm cc}$) generated from $+V_s$(34 V.) This is permissible since the operational amplifier has rail-to-rail inputs and the comparator inputs have dc offsets added via resistors to $V_{\rm cc}$.

Taking into account the carrier voltage dc bias resistor $R_{\rm bias}$, the BPCM controller gain constants are given as

$$\begin{aligned} K_{\rm cfb} &= \frac{R_{\rm vfb}||R_{\rm vff}||R_{\rm bias}}{(R_{\rm vfb}||R_{\rm vff}||R_{\rm bias}) + R_{\rm cfb}} \\ K_{\rm vfb} &= \frac{R_{\rm cfb}||R_{\rm vff}||R_{\rm bias}}{(R_{\rm cfb}||R_{\rm vff}||R_{\rm bias}) + R_{\rm vfb}} \\ K_{\rm vff} &= \frac{R_{\rm vfb}||R_{\rm cfb}||R_{\rm bias}}{(R_{\rm vfb}||R_{\rm cfb}||R_{\rm bias}) + R_{\rm vff}} \end{aligned} \tag{43}$$

From these expressions, the ratio $K_{\rm vfb}/K_{\rm cfb}$ can be derived as

$$\frac{K_{\rm vfb}}{K_{\rm cfb}} = \frac{R_{\rm cfb}}{R_{\rm vfb}} \tag{44}$$

Setting $R_{\rm vfb} = 10\ {\rm k}\Omega$, the analytically predicted optimal $R_{\rm cfb}$ is 8.264 kΩ, which was rounded off to 8.2 kΩ in the prototype design. In order to get a closed-loop gain of 20 dB, $R_{\rm vff}$ was set to 1 kΩ. The carrier dc bias point $V_{\rm carrier,bias}$ was set using $R_{\rm bias}$ from the following expression:

$$V_{\rm carrier,bias} = V_{\rm cc} \times \frac{R_{\rm vfb}||R_{\rm cfb}||R_{\rm vff}}{R_{\rm vfb}||R_{\rm cfb}||R_{\rm vff} + R_{\rm bias}} \tag{45}$$

The choice of $R_{\rm bias} = 3.3\ {\rm k}\Omega$ thus lifts the carrier dc operating point to 1 V, to ensure that the carrier stays within the common-mode input range of the comparator. The prototype design gain coefficients are summed up in Table IV along with the true optimum coefficients and two sets of suboptimal coefficients. The suboptimal designs represent the lumped effect of component tolerances that are likely to be significant in the output filter components. Although $K_{\rm cfb}$ is physically determined only by resistors, deviations in L and C require proportional changes in $K_{\rm cfb}$ for optimality to be preserved, so tolerances on L and C can be directly mapped to a tolerance on $K_{\rm cfb}$ as far as carrier distortion is concerned. Practically, the suboptimal designs were implemented by changing $R_{\rm cfb}$ to 10 kΩ and 6.2 kΩ, respectively.

With the prototype design gain coefficients, the carrier signal unity-step response slope is found to be

$$\dot{V}_{\rm carrier,step}\,(0) = \frac{K_{\rm cfb} \times N_L}{\tau_{\rm est}} \approx 5.39\,{\rm mV}/\mu{\rm s} \tag{46}$$

With a nominal supply voltage V_s of 34 V, this means that a 34 V step is applied to $G_{\rm ctrl}(s)$ for $D = 0.5$, leading to a carrier signal slope of 183 mV/μs. This means that the K [23] of the design is

$$K \equiv 2 \times \left.\frac{dV_{\rm carrier}}{dt}\right|_{D=0.5} = 2V_s \times \frac{K_{\rm cfb} N_L}{\tau_{\rm est}} \approx 0.366\,{\rm V}/\mu{\rm s} \tag{47}$$

where K can also be found as follows [23]:

$$K = 2V_s \times {\rm step}\left\{\lim_{s\to\infty} G_{\rm ctrl}(s)\right\} \tag{48}$$

Since the switching frequency of a triangular-carrier hysteretic control system is a parabolic function of duty cycle [16], [33], [35], [37] given quite precisely by

$$f_{\rm sw}\,(D) = \frac{D\,(1-D)}{2(V_{\rm hyst}/K) + t_d} \tag{49}$$

then, for a nominal ($D = 0.5$) switching frequency $f_{\rm sw,nom}$ of 350 kHz, assuming 100 ns comparator/power stage delay t_d, the hysteresis level $V_{\rm hyst}$ should be

$$V_{\rm hyst} = \frac{K}{2}\left[\frac{1}{4f_{\rm sw,nom}} - t_d\right] \approx 110\,{\rm mV} \tag{50}$$

Note that the hysteresis window of the comparator in this case is still defined as $\pm V_{\rm hyst}$. The desired hysteresis window is easily implemented by proper choice of the resistors (R_{h1}–R_{h4}) attached to the noninverting comparator input. The prototype design used $R_{h1} = 33\ {\rm k}\Omega$, $R_{h2} = 3.3\ {\rm k}\Omega$, $R_{h3} = 22\ {\rm k}\Omega$, and $R_{h4} = 3.3\ {\rm k}\Omega$.

VI. SIMULATED/CALCULATED RESULTS

The accuracy of the proposed carrier distortion optimization method and the sensitivity of the optimum to parameter variations were examined by PSpice simulation and the results are

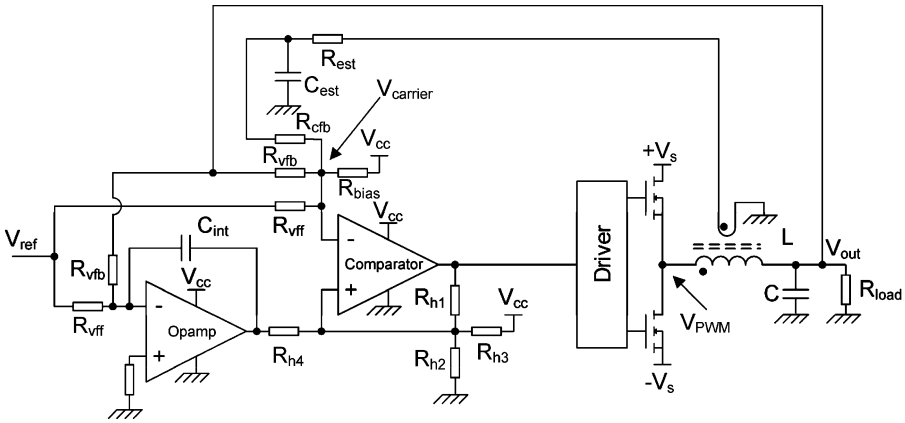

Fig. 14. Hysteretic SO BPCM + PI controlled single-ended amplifier with single-supply ($V_{\rm cc}$) control circuitry.

TABLE IV
OPTIMAL AND IMPLEMENTED BPCM AMPLIFIER DESIGN GAIN COEFFICIENTS

Parameter	Optimal design	Prototype design	Sub-optimal design I ("-20%")	Sub-optimal design II ("+29%")
K_{cfb}	0.0800	0.0800	0.0665 (-20%)	0.103 (+29%)
K_{vfb}	0.0661	0.0656 (-0.7%)	0.0665 (+0.7%)	0.0639 (-3.4%)
K_{vff}	0.661	0.656	0.665	0.639

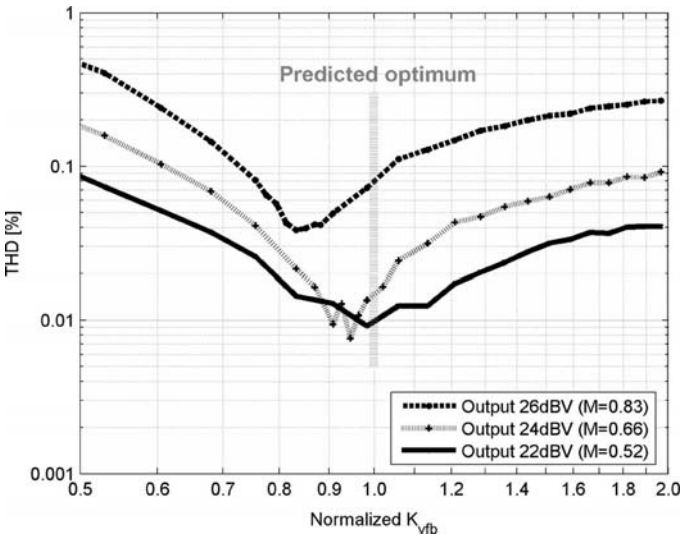

Fig. 15. Simulated THD (3rd + 5th harmonics only) with $K_{\rm vfb}$ values around the predicted optimum.

shown in Fig. 15. A simulation model of the found optimum BPCM + PI design was implemented, with the switching components made ideal so that only carrier distortion was generated. The output THD of the BPCM + PI amplifier simulation model was evaluated for three different amplitudes of 5-kHz sine wave output. In each case, voltage feedback coefficient $K_{\rm vfb}$ was varied from 0.5 to 2 times ($\pm$6 dB) its predicted optimum value. As can be seen, the proposed method succeeds in finding the $K_{\rm vfb}$ that leads to minimal THD for low output levels. The optimal $K_{\rm vfb}$ is seen to vary with output level, however, with a lower $K_{\rm vfb}$ (or a higher $K_{\rm cfb}$) being preferable at high output levels. This suggests that a true global optimum feedback coefficient weighting does not exist and that each output level has its own optimum $K_{\rm cfb}/K_{\rm vfb}$. The amount of carrier distortion generated is seen to be relatively sensitive to component tolerances; optimizing the amplifier for 24 dBV output by choosing a $K_{\rm vfb}$ of 0.95, $\pm 10\%$ $K_{\rm vfb}$ variation is enough to cause a THD increase from 0.01% to 0.02% at 24 dBV output. For $\pm 20\%$, the THD potentially increases to 0.03%. Still, these numbers are far lower than what would probably be obtained by not paying attention to carrier distortion; for all three output levels, THD varies by a factor of around 10 for relatively modest $K_{\rm vfb}$ variations of $\pm$6 dB around the predicted optimum. An interesting point to note is that even though the amplifier loop gain increases with $K_{\rm vfb}$, overall distortion also increases when $K_{\rm vfb}$ is too high, showing that loop gain maximization alone is not necessarily the best strategy for linearizing SO class-D amplifiers. When combined with minimization of carrier distortion, however, maximized loop gain is still an advantage. This is because 1) high loop gain reduces the amplifier's sensitivity to other disturbances than carrier distortion and 2) loop gain still has an effect on carrier distortion. As seen from (24), designing for a high-gain $G_{\rm ctrl}(s)$ in the audio band directly reduces sensitivity to carrier distortion. There is a complication associated with this, however, since increasing the magnitude of $G_{\rm ctrl}(s)$ also requires an increase in the amount of hysteresis needed for a given switching frequency thereby also increasing the amount of carrier dc variation by the same amount. To maximize loop gain while maintaining carrier distortion, it is therefore necessary to increase the low-frequency magnitude of $G_{\rm ctrl}(s)$ while still ensuring a linear step response and not increasing K as seen from (48) and (49). A difficult exercise, this is at least made somewhat easier by the avail-

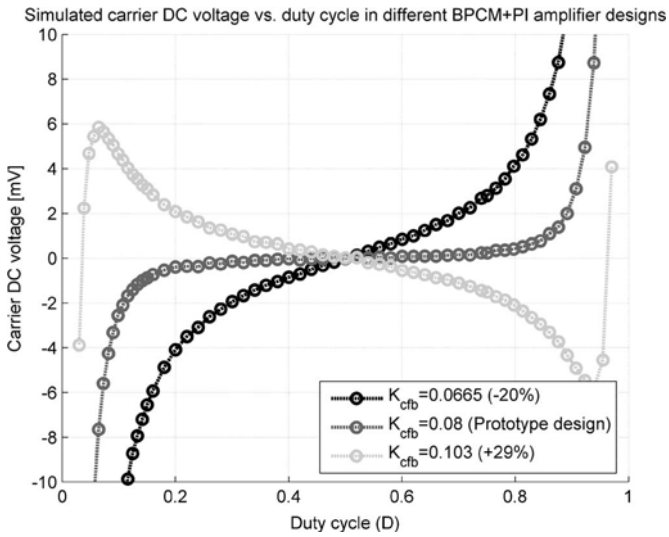

Fig. 16. Simulated carrier dc voltage versus steady-state duty cycle for prototype and suboptimal BPCM + PI amplifier designs. Implemented design can be expected to be very linear for duty cycles from 0.2 to 0.8 (corresponding to an $M < 0.6$ or 23 $\mathrm{dBV_{rms}}$ sine wave from $V_s = 34$ V).

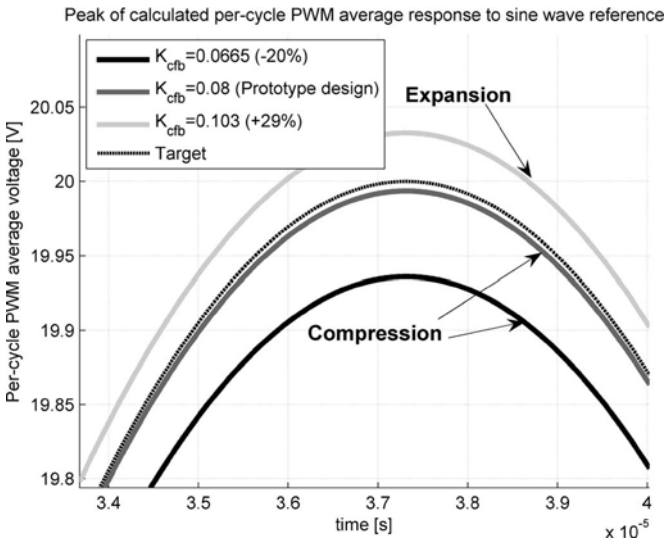

Fig. 17. Calculated sine wave responses of optimal and suboptimal amplifier implementations at 20 V_{peak} (23 $\mathrm{dBV_{rms}}$ or $M = 0.6, D_{\max} = 0.8$) output level. The optimized design is visibly more ideal than the suboptimal designs.

ability of the proposed method for optimizing the $G_{\mathrm{ctrl}}(s)$ step response.

In order to further quantify the carrier distortion mechanism, the methodology already used for THD calculation on the simple AIM controller was adapted for the BPCM + PI system. Due to the complexity of $G_{\mathrm{ctrl}}(s)$ of the BPCM + PI controller, simulation, rather than analysis, was used to determine $V_{\mathrm{carrier,dc}}(D)$. The control loop time delay t_d was set to zero to avoid masking of the nonlinear, dc variation caused by any nonintegrator $G_{\mathrm{ctrl}}(s)$, by the linear, delay-induced variation [21], [35]. The results are shown in Fig. 16 for the nearly-optimal implemented design as well as for the suboptimal designs. It is generally apparent that the relatively slight variation in K_{cfb} causes the carrier average to exhibit significantly more nonlinear variation with duty cycle; hence, the THD can also be expected to increase. As shown in Fig. 17, the generated carrier distortion is expansive (like in the AIM) when the current feedback component is too high since this leads to an overemphasis of the exponential carrier component. Conversely, the carrier distortion instead becomes compressive when the output feedback component is too high.

For THD calculations, the data from Fig. 16 was used (interpolating between data points) to calculate the amplifier response to a sine wave. The sine wave was assumed to have a frequency above the PI corner frequency (i.e., integral output voltage feedback is assumed negligible compared to proportional feedback), allowing (29) to be used for $G_{\mathrm{ctrl}}(s)$, which was then assumed to be flat within the audio band. This is justified by the fact that the inductor current signal is effectively high-pass filtered (see (29)) by the current estimator, so that the output voltage feedback via K_{vfb} dominates at low frequencies. With the low-frequency approximation $G_{\mathrm{ctrl}}(s) = K_{\mathrm{vfb}}$, the method used for the THD calculation in the AIM was applicable. Results for the prototype and suboptimal designs are shown in Fig. 18, where it is confirmed that THD performance is quite sensitive to the carrier composition. For example, inspecting Fig. 18, an amplifier rated for 0.02% maximum THD would have its rated output power reduced by a factor of two (3 dB) with a K_{cfb} tolerance of 20%. As will be demonstrated in the experimental section, this is a reasonable claim since carrier distortion is shown to be the dominant nonlinearity at high output levels. For the optimal design, THD is predicted to stay at a very low level (less than 0.01%) up to 24 $\mathrm{dBV_{rms}}$ output level, where a sharp increase is observed as the carrier average voltage deviates strongly from zero at the peaks of the sine wave.

VII. Experimental Results

The BPCM + PI amplifier in Fig. 14 was implemented on a four-layer printed circuit board (PCB) with one-sided component placement as shown in Fig. 19. Small IRF6645 (28 mΩ, 100 V, 14 nC gate charge) MOSFETs were used together with ample dead time (around 15 ns) to allow cooling via the PCB. A standard HIP2100 with input-side residual current device networks for setting the dead time was used for the MOSFET driver along with a discretely built phase-split/level-shift circuit for interfacing with the LMV7219 comparator.

THD + N measurements were performed using an Audio Precision System 2 with 22 kHz bandwidth without the Aux-25 prefilter. The raw distortion and noise generated by the control system are assessable from the no-load THD + N versus output level measurements in Fig. 20. These measured results are directly comparable to the calculated ones in Fig. 18, since the third and fifth harmonics were found (via the fast fourier transform function) to dominate the generated THD. To ensure a flat $G_{\mathrm{ctrl}}(s)$ as assumed for the calculations in Fig. 18, C_{PI} was temporarily doubled to 100 nF, effectively halving the integral feedback term. The measurements confirm

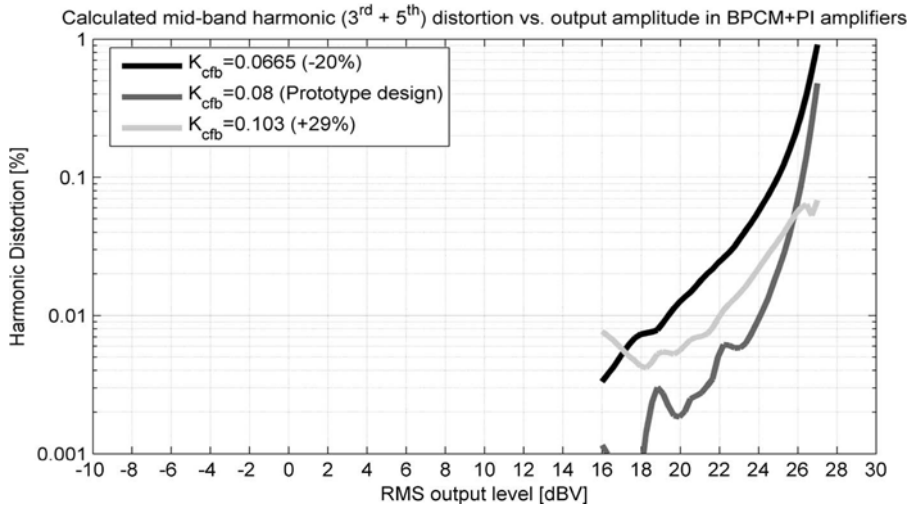

Fig. 18. Calculated THD (3rd + 5th harmonics only) caused by carrier distortion in optimum and implemented prototype BPCM + PI amplifier designs with variable K_{cfb}. For the implemented design, no-load THD is expected to be less than 0.02% below 25 $\mathrm{dBV_{rms}}$ ($M = 0.74$ or $D_{\max} = 0.87$ output level.

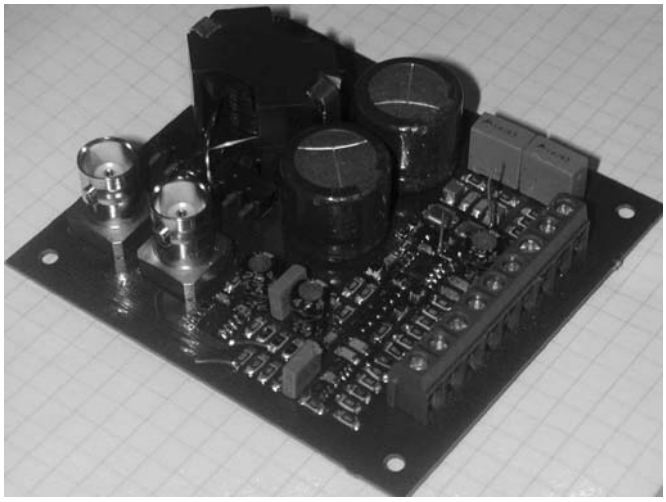

Fig. 19. Prototype hysteretic BPCM + PI amplifier PCB.

that even modest – 20% or +29% deviation from the optimal carrier composition creates significant THD at high output levels. Some deviation is evident below 25 dBV (particularly in the "+29%" implementation), but agreement is very good above this level.

Given that the optimized prototype design produces higher THD at high levels than the "+29%" design, it is of course debatable whether or not it is in fact optimal. However, by defining the optimal design as the one that provides the lowest THD at low output levels, optimality has been achieved. As also predicted by simulations in Fig. 15, linearity can be increased at high output levels by increasing K_{cfb} (or lowering K_{vfb}) thereby sacrificing low-level performance Such tradeoffs are best implemented following a precise specification of the desired THD and output power performance of the amplifier.

The noise generated by the BPCM + PI amplifier is 240 μV since THD + N is 0.02% at 0 $\mathrm{dBV_{rms}}$ output level where noise is dominant (as seen by the 6 dB/octave slope of the THD + N curve). This is a rather high number that could probably be reduced by the use of a slower comparator. This is because [29] the comparator integrates the circuit noise (generated by resistors and active components) during the time when the switching decision is made, and slower comparators have a longer decision "window," effectively averaging the applied noise for a longer period.

The triangularity of the carrier signal in the three different configurations is assessable from the measurements in Fig. 21. Visually, the optimized carrier signal appears the most triangular, as also expected for the design with the lowest THD.

The performance of the implemented power switching stage was examined using the "analog persist" function on a Lecroy WaveRunner oscilloscope. This allowed observation of the total spread in variation of the switch node behavior with load current. For a sinusoidal output current of ±6.25A, a 15 ns spread in transition delay time was observed as seen in Fig. 22. This is a result of the use of 15 ns dead time and a ripple current of 2.4 $\mathrm{A_{pp}}$, leading to the power stage operating in both the zero current switching (ZCS) mode (for output currents less than ±1.2A, given enough dead time) and hard-switched mode (for higher output currents).

The THD + N performance of the prototype design with the usual 4 Ω and 8 Ω loads and three commonly used test frequencies (100 Hz, 1 kHz and 6.7 kHz) is indicated in the measurements in Figs. 23 and 24. The maximum frequency of 6.7 kHz is often used for switch-mode amplifiers since the third harmonic distortion of higher frequencies falls outside of the commonly used 20–22 kHz measurement bandwidths. Due to the dominance of the integral voltage feedback term at low frequencies, the 100 Hz THD figures are very low. The use of higher-order integral low-frequency feedback allows extremely low THD to be obtained at low frequencies [5], [6], [9], but usually does not help at higher frequencies since the loop gain inevitably has to roll off. Additionally, it is obvious that taking extra integral feedback too far will result in an increase in carrier

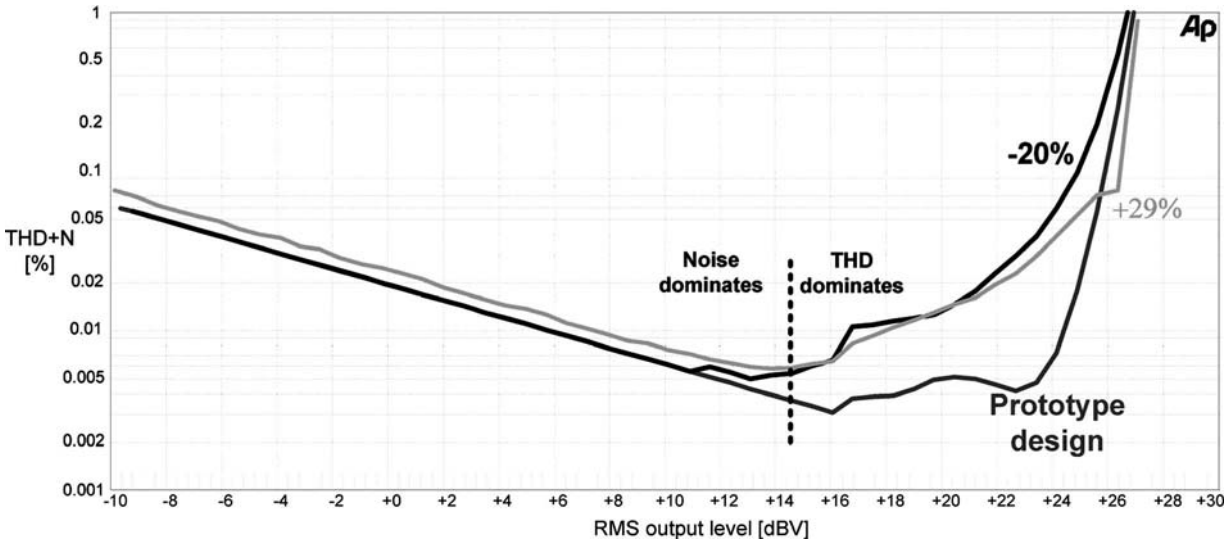

Fig. 20. Unloaded prototype amplifier THD + N versus output level ($0\ \mathrm{dBV} = 1\ V_{\mathrm{rms}}$) at 1 kHz with optimal and suboptimal K_{cfb}, for comparison with Fig. 18. THD of the optimized design is less than 0.02% up to 25 $\mathrm{dBV_{rms}}$. Suboptimal designs have higher THD as expected.

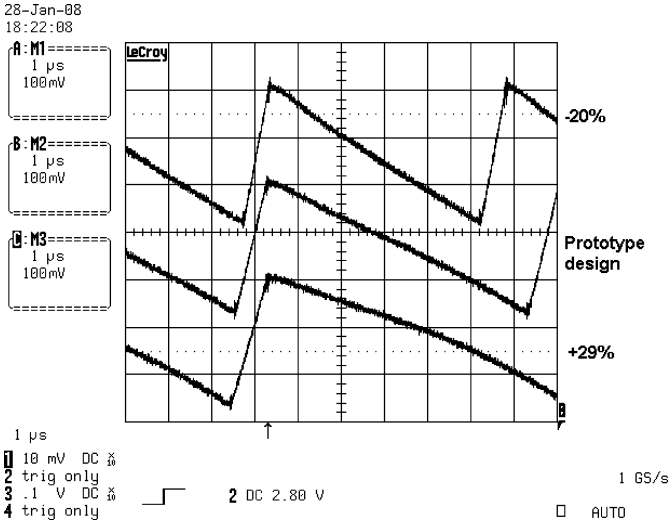

Fig. 21. Prototype carrier waveforms for $D = 0.88$ (peak of $M = 0.76$ sine wave.) Optimized design runs at 150 kHz, indicating an idle switching frequency of 350 kHz. The optimized carrier visually appears to be the most triangular, as also targeted by the proposed optimization method.

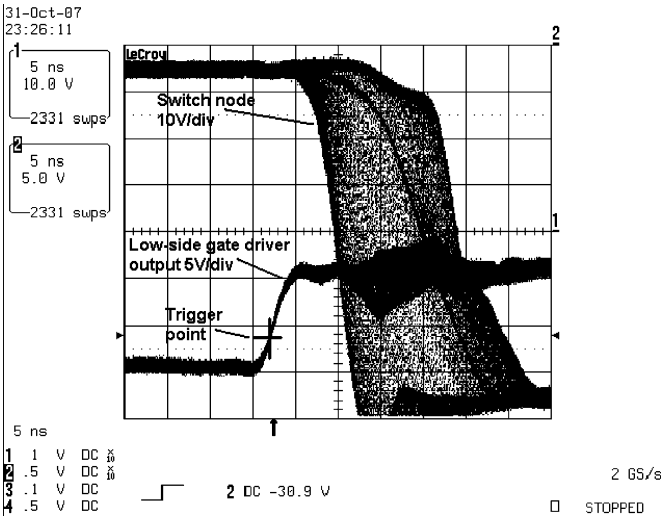

Fig. 22. Variation of switching behavior of prototype, measured using the "analog persist" function. Output is an 80 W ($25\ V_{\mathrm{peak}}$) sine wave into 4 Ω and there is evidently a switching transition point variation of around 15 ns due to the combination of dead time and variation in load current.

distortion, since a higher-than-first-order integral of a PWM signal is not triangular.

Overall, the presented design can be rated at 80/45 W with less than 0.03% THD + N for 4/8 Ω, which is a very decent result for a design done purely by analysis. As indicated by Fig. 20 and the analysis performed, it would in fact be quite difficult to come up with a significantly better design given the BPCM feedback topology and the power stage used. This statement is backed up by results from prior art, which are summarized in Table V. Control schemes, power stage configurations, and switching frequencies are also listed for reference. BTL refers to "Bridge Tied Load," i.e., the full-bridge configuration while SE refers to "single-ended." Other very noteworthy results exist [6], [11], but details are inadequate for comparative purposes. It should of course be noted that the power stage components used in the presented paper are nearly state of the art with discrete components and that this of course impacts the results positively. However, it was shown in Figs. 18 and 20 that carrier distortion generates exactly 0.02–0.03% THD for $M = 0.75$, so it is the carrier distortion that dictates the final THD specification of the design. Hence, the presented optimization method has been shown to be instrumental in obtaining the THD results in Figs. 23 and 24. This was indeed also the conclusion in [5] for the discrete-time-based optimization method for fixed-frequency PWM-based amplifiers. It is expected by the authors that future publications will demonstrate a clear link between the proposed averaging and time-domain-based view of "carrier distortion" and the discrete-time and frequency-domain-based view of "aliasing distortion" [5]. The presented averaging approach is principally also applicable for THD prediction in phase-shift

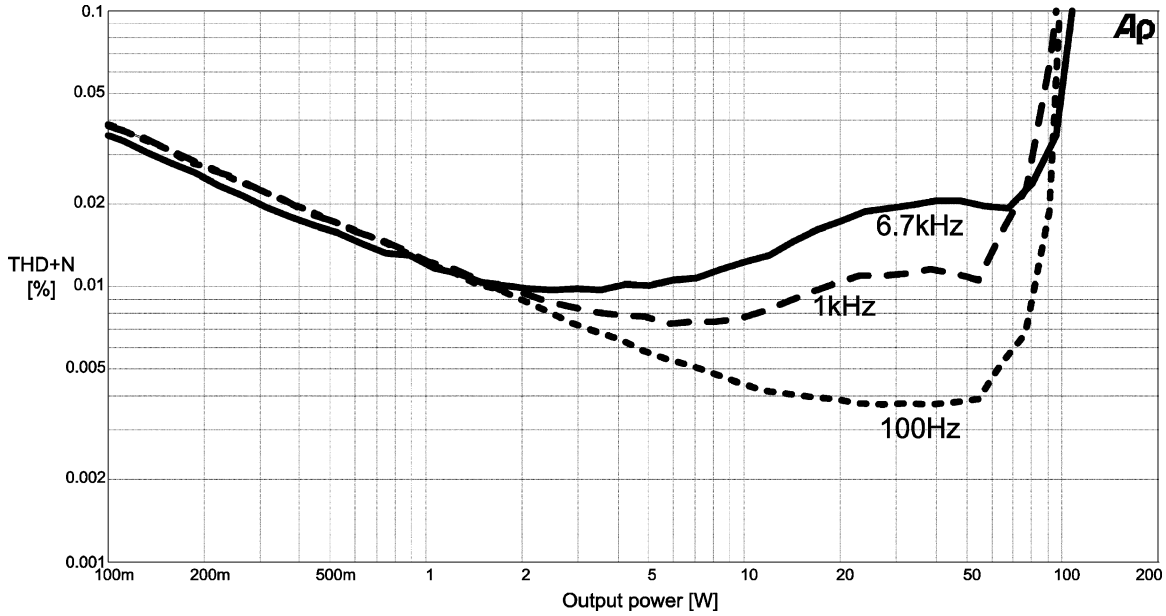

Fig. 23. Optimized prototype amplifier THD + N versus output power with a 4 Ω load. Worst case (below 80 W or $M = 0.75$) THD + N is very respectable at 0.03% at 6.7 kHz.

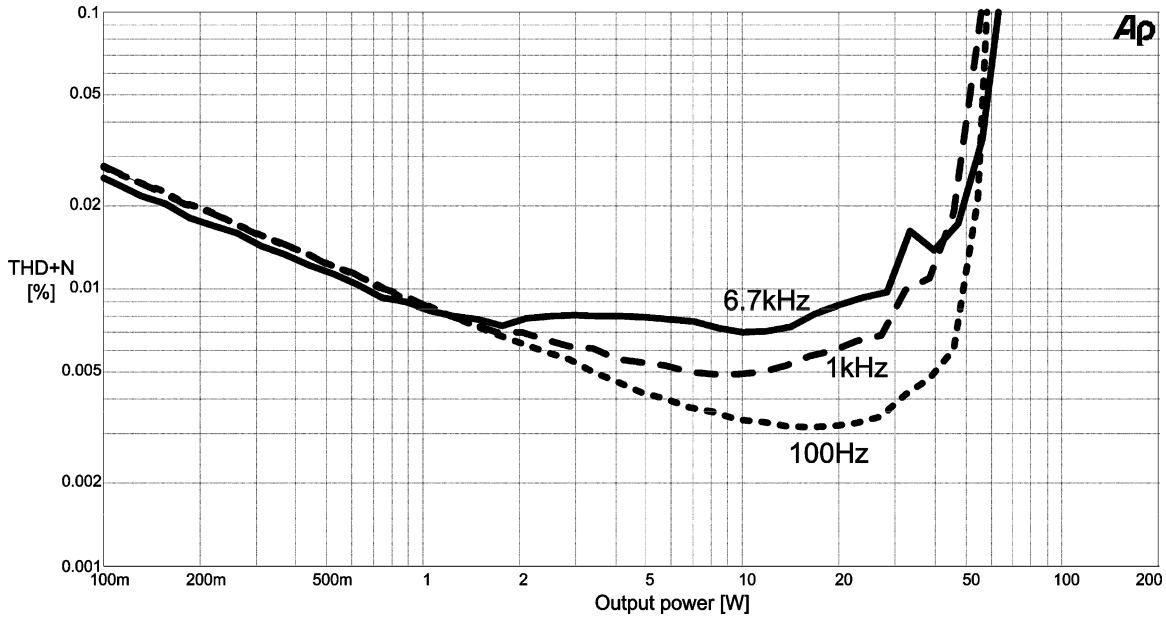

Fig. 24. Optimized prototype amplifier THD + N versus output power with an 8 Ω load. Distortion stays below 0.02% below 45 W, corresponding to $M = 0.79$.

SO control systems [6]–[8], where the carrier signal is sinusoidal and oscillation is induced by raw phase shift in the loop filter $G_{\rm ctrl}(s)$ rather than by comparator hysteresis. The carrier average in these systems will also potentially exhibit nonlinear variation with duty cycle. However, averaging the carrier signal in such systems is nontrivial since oscillation is only possible if the loop filters are second-order or higher [7] or comparator time delay is added to the analysis.

Finally, one important amplifier parameter that has not yet been considered, namely the frequency response, is examined in Fig. 25. For the typical 4–8 Ω load, the frequency response is fortunately flat within 1.2 dB below 20 kHz. Prefiltering could be used to straighten this out if desired. Computation of the frequency response for verification is easily done using the classical sliding mode approximation, but falls outside the scope of this paper.

TABLE V
REPRESENTATIVE PRIOR ART THD + N RESULTS FOR COMPARISON WITH PRESENTED STUDY

Reference	THD+N, 4Ω, M=0.75, 6.7kHz	THD+N, 8Ω, M=0.75, 6.7kHz	Control topology	Power stage, supply voltage, f_{sw}
[5]	?	0.018%	Fixed-freq. PWM + "MAE filter"	BTL, 55V, 350kHz
[9]	0.04%	?	Hysteretic SO, "GLIM"	SE, +/-40V, 350kHz
[38]	?	0.05%	One-cycle	BTL, 54V, 250kHz
This work	0.03%	0.02%	Hysteretic SO, BPCM+PI	SE, +/-34V, 350kHz

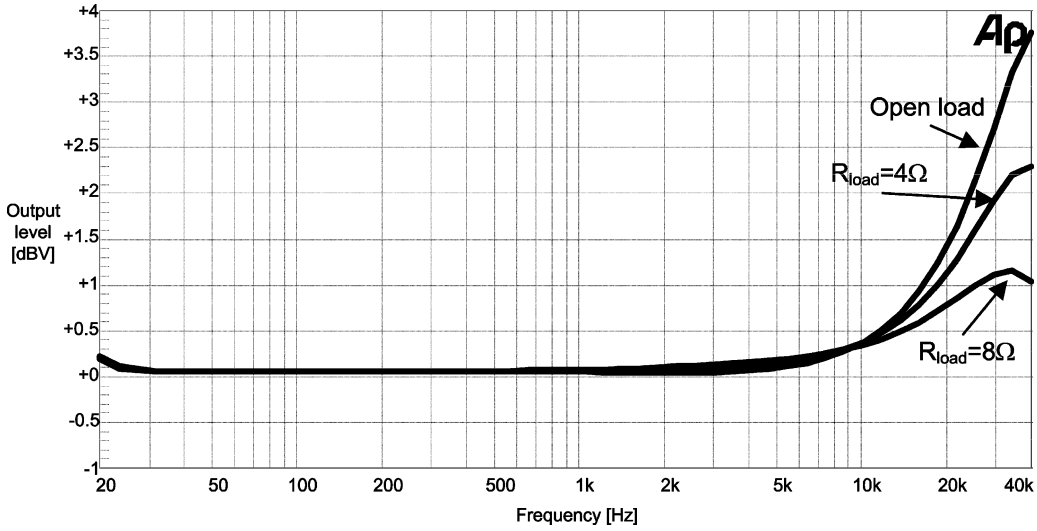

Fig. 25. Measured frequency responses of prototype amplifier. With a typical speaker load (4–8 Ω), response is flat within 1.2 dB over the audio band (20 Hz to 20 kHz.).

VIII. CONCLUSION

An approach for understanding, evaluating, and minimizing the intrinsic distortion generated by hysteretic SO controllers applied to buck-type power converters has been presented. The term "carrier distortion" has been used for this intrinsic distortion phenomenon, referring to prior art. Carrier distortion is mainly an issue of concern in switch-mode ac power amplifiers where the signal bandwidth is high compared to the switching frequency and where fast, high-quality switching components are used. In such cases, distortion generated by imperfect switching is low while loop gain of the control system is limited at high signal frequencies, making carrier distortion the dominant nonlinearity in the power amplifier at high output levels. Class-D audio power amplifiers are an obvious application for the presented analysis, but reducing harmonic distortion of switch-mode power amplifiers is also of interest in a variety of other niche applications. Examples include xDSL drivers, envelope-tracking power supplies, and ac transmission line filters.

In agreement with prior art statements, it has been found that the carrier signal (a.k.a. sliding variable) should be made triangular by proper design of the control loop(s) to minimize this distortion. This directly resulted from an averaging analysis of the steady-state hysteretic comparator input/output waveforms. It was shown that even an amplifier with a perfect power stage supplied with a perfect dc supply voltage can in fact produce significant harmonic distortion due to the carrier distortion mechanism. Based on the desire for a triangular carrier signal for minimizing carrier distortion, a simple s-domain analytical approach was proposed and demonstrated on a nontrivial control topology. An optimized prototype amplifier design was implemented and verified against modeled results. The generated harmonic distortion was found to be well described by the proposed methodology as well as quite sensitive to parameter variation. The harmonic distortion results achieved with the prototype design were at state-of-the-art level, verifying the validity and usefulness of the presented approach.

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A Versatile Discrete-Time Approach for Modeling Switch-Mode Controllers

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***Abstract*—This paper presents a universal method for modeling the frequency response of comparators in switch-mode controllers. As the main non-linearity in most switch-mode controllers, understanding the comparator is the key to understanding the system. Based on discrete-time modeling, the proposed method is demonstrated to allow very precise predictions of comparator frequency response in a variety of control schemes. In the presented work, the modeling method is exemplified for the standard PWM and two different self-oscillating (a.k.a. sliding mode) control schemes. The proposed method is believed by the authors to be the first method that is able to handle these fundamentally different control schemes within a single modeling framework. Experimentally measured output impedance and comparator magnitude responses are compared to the model results. Great accuracy is achieved from DC to frequencies far beyond the switching frequency.**

I. INTRODUCTION

Accurate system modeling is essential in the design, optimization and verification of switch-mode control loops and has been studied intensely for many decades. This work is motivated by the need for better models for high-performance switch-mode control systems, as required in e.g. class-D audio power amplifiers or envelope tracking power supplies for RF power amplifiers. Such systems need to accurately reproduce reference waveforms with relatively high frequencies and thus need a very high loop-bandwidth relative to the switching frequency. Moreover, these switching circuits may get subjected to frequency components in far excess of their switching rate: Audio amplifiers may receive high frequency noise components from over-sampled digital to analog converters and a power supply is subjected to very high frequency load current components, e.g. from a CPU core. Power conversion systems with multiple power converters operating at different frequencies prescribe that converters may be subjected to supply ripple and harmonics at frequencies far above their switching frequency.

Consequently, accurate control system modeling from DC to far beyond the switching rate is important.

Currently a wide array of models and methods exist for use with different types of switch-mode control loops. A simple averaging-based text book example [1] is the continuous-time, fixed-gain model of the standard pulse width modulator (PWM). Discrete-time models based on cycle-by-cycle averaging are capable of better high-frequency accuracy [2], but are generally not accurate above half the switching frequency. Self-oscillating (a.k.a. sliding mode) control loops are arguably the most difficult systems to model due to the merging of oscillator, control system and modulator functions. A common approach is the "sliding mode" approximation [3] (error/carrier/sliding signal is always zero), which can work very well in some cases [4], but not in others [5]. More accurate, continuous-time approaches use describing function techniques [5], [6], but are only accurate below the switching frequency. While other prior art [8] also accounts for aliasing effects, DC-to-above-f_{sw} accuracy has yet to be demonstrated.

A discrete-time modeling framework was proposed in [7] in the context of switch-mode audio power amplifiers. This model provides a linearized small-signal model accurate at any frequency and it elegantly accounts for frequency aliasing/imaging. The essence of the model is that the comparator acts as a sampler with a frequency-independent finite gain being inversely proportional to the slew-rate of the carrier waveform on its input, in accordance with the textbook model [1]. This finite and constant gain property is seemingly contradicted by other modeling work [9] yielding a theoretically infinite comparator DC gain for the simple 1st-order hysteretic control (sliding mode assumption).

As the present paper will demonstrate, the reason for this discrepancy is the constant-gain behavior only applies in the discrete-time domain. A gain-phase analyzer however, treats all signals as being in continuous-time and performs a narrow-band analysis centered on the stimulus frequency. The resulting narrow-band or continuous-time equivalent comparator gain consequently becomes frequency dependent due to the mixing of continuous-time and discrete time signals.

The presented work aims at deriving the single frequency, narrow-band in/out transfer function of the comparator (ideally the only non-linear control loop component) using the framework from [7]. Using the derived comparator frequency response $K_s(f)$, the single frequency stimulus small-signal response of the entire system can be found using conventional continuous-time (s-domain) analysis techniques without entering the z-domain.

A. Definitions

The following definitions are used throughout the paper, where f is the stimulus frequency and f_{sw} is the switching frequency:

$$s = j2\pi f \quad T_s = \frac{1}{2f_{sw}} \quad z = e^{sT_s}$$

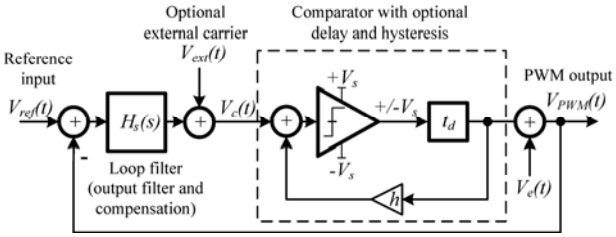

Figure 1. Generic model of a switch-mode control loop [7]

II. DISCRETE-TIME LOOP MODEL

The modeling approach proposed in this paper is based on the generic switch-mode control loop model from [7], as shown in Fig. 1. The physical comparator in the control loop is combined with the switching power stage, time delay t_d and positive feedback h (for providing hysteresis) to form the comparator block shown. The output filter (e.g. an LC filter), compensation network (e.g. a PID) and phase-shift network (as required for a phase-shift self-oscillating controller) are lumped together in the loop filter $H_s(s)$ which represents the combined s-domain transfer function from the comparator (which notionally includes the switching power stage) output back to the comparator input. An optional carrier signal $V_{ext}(t)$ is added to the comparator input when the system is clocked (e.g. using triangle waveform in a conventional clocked PWM control loop).

A. Model Scope

The modeling framework to be presented is applicable when the system is in a periodic steady-state condition with a 50% duty cycle PWM signal. The model then describes the system dynamics for infinitesimal perturbations around the periodic steady-state. This gives thus a small-signal AC model that is valid at any frequency but only for very low amplitude stimulus signals. The model will thus not reflect large-signal behavior. A large-signal model only accurate near DC was presented in [13].

B. Sampling Comparator Model

At steady state with no stimulus applied on the input V_{ref}, the comparator input signal $V_c(t)$ is a periodic carrier waveform composed of the optional external carrier added to the ripple signal coming from the feedback path via the loop filter $H(s)$. The zero-crossings of $V_c(t)$ aligns with the 50% duty cycle transitions of the comparator PWM signal. If we superimpose a small-amplitude perturbation signal $V_p(t)$ on top of $V_c(t)$ we will perturb the PWM transition time instants by a small amount. We further assume that the perturbation is so small that it does not change the carrier signal $V_c(t)$. If we subtract the PWM waveform of an un-perturbed system, we get a pulse train of narrow pulses around each PWM edge. These narrow error pulses have either $+2V_s$ or $-2V_s$ in amplitude depending on the polarity of the perturbation signal and the slope polarity of the carrier $V_c(t)$. As shown in Fig. 2, for small perturbations, the area of each perturbation error pulse can be approximated by:

$$A_n \cong 2V_s \cdot \frac{V_p(n \cdot T)}{\left|\dot{V}_{c0}\right|} \tag{1}$$

This means that the comparator samples the perturbation waveform at every zero crossing and

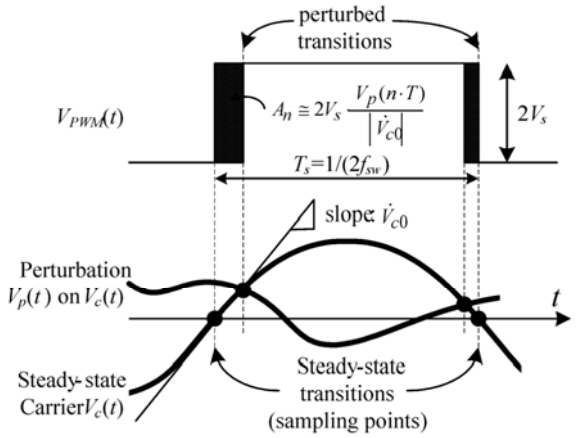

Figure 2. Gain computation concept for sampling comparator model.

produces a narrow output pulse (approximating a Dirac delta pulse) having an area proportional to the sampled amplitude. If we assume that the zero-crossings of the steady-state carrier $V_c(t)$ are symmetrical (same absolute value of the slope) then the comparator samples uniformly at a frequency of $2f_{sw}$. The comparator also acts as a gain K_z which is the proportionality between the sampled amplitude and the average pulse area over one sampling period:

$$K_z = \frac{A_n}{V_p(nT_s) \cdot T_s} = \frac{2V_s}{\left|\dot{V}_{c0}\right| T_s} = \frac{4V_s f_{sw}}{\left|\dot{V}_{c0}\right|} \tag{2}$$

Note that this gain corresponds to the classical model used for pulse-width modulators [1].

As known from digital signal processing theory, the sampling process gives rise to frequency aliasing and imaging. This means that the sampler does not tell the difference between frequency components that deviate by a multiple of the sampling frequency – also known as frequency aliasing. For example, a signal near the sampling frequency is treated the same way as a close-to-DC signal. The sampler also produces identical frequency images replicated at every multiple of the sampling frequency (called frequency images). This aliasing /imaging behavior may for example shift high-frequency circuit noise into the audible band of a switching amplifier. Another example is harmonic distortion due to aliasing of high-frequency image components generated by the Pulse-Width Modulation (PWM) [13].

C. Closing the loop

The Dirac delta pulses of the comparator propagate back via the loop filter and produce a waveform superimposed on the carrier. This feedback waveform is then sampled again by the comparator and we have a closed-loop system around a sampler. It is first noted that the comparator input (perturbation) waveform is ignored at all other time instants but the sampling time points. This means again that we can replace the loop filter $H_s(s)$ with a suitable discrete-time domain (z-domain) filter $H_z(z)$ and achieve a loop fully in discrete-time as shown in Fig. 3.

This z-domain equivalent of $H_s(s)$ has the property that its impulse response matches exactly with the impulse response of its s-domain counter-part at the sampling time points. This transformation from s- to z-domain is known as the Impulse Invariance Method [11] and is obtained by performing a partial fraction expansion and mapping the

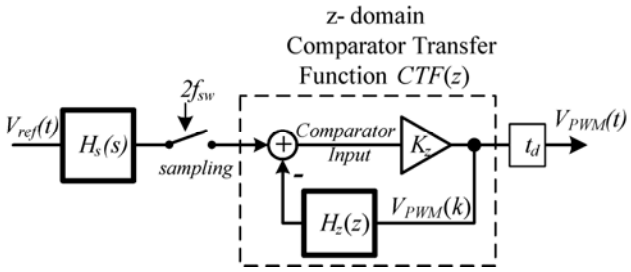

Figure 3. The comparator transfer function, *CTF(z)*

s-domain poles and zeros to the *z*-plane by using the transformation $z = \exp(s/(2f_{sw}))$ and scaling down the gain by the sampling rate. Note that the comparator delay t_d has to be included in the *s*-domain before transforming to the z-domain loop transfer function $H_z(z)$, e.g. by using a Padé approximation.

Once the comparator has made a transition, the feedback path cannot can not change the timing of the current transition but only affect the timing of the following transition. In other words, the current sampled value will first affect the comparator in the next sampling time. Consequently, this causality constraint forces the $H_z(z)$ impulse response to zero at time zero. Practically, this can be enforced in the model by taking the impulse invariance transform $\hat{H}_z(z)$ and subtracting the impulse response at time-lag zero $\hat{h}_z(k=0)$:

$$H_z(z) = \hat{H}_z(z) - \hat{h}_z(k=0) \tag{3}$$

The impulse response for a *z*-transfer function at time-lag zero can be found by normalizing the transfer function so that the highest order term in the denominator *z*-polynomial is unity. In this case, the time-lag zero response is equal to the numerator *z*-term with order equal to the denominator order.

For example, an s-domain integrator:

$$H_s(s) = \frac{1}{\tau \cdot s} \tag{4}$$

The pole at $s = 0$ is mapped to $z = 1$ which leads to the *z*-domain integrator with no delay (and scaling by $2f_{sw}$). By eliminating the impulse response at time zero by subtraction we then get a *z*-domain integrator with one sample delay:

$$H_z(z) = \frac{z^{-1}}{2\tau \cdot f_{sw}\left(1 - z^{-1}\right)} \tag{5}$$

Note that $H_z(z)$ is invariant to any pure delay added in the *s*-domain being less than one sample interval. Such a small delay just shifts the $H_s(s)$ impulse response (which is a step function) in time and results in the same discrete-time sequence when sampled. This delay-invariance only applies to a pure integrator.

The 2nd-order ($1/s^2$) integrator has an impulse response being a linear ramp starting at zero amplitude at time zero. Consequently, the Impulse Invariant transform obeys the causality constraint with no further correction. The resulting z-domain function becomes a double integrator with just one sample delay.

Note that the described *s* to *z* transformation is linear meaning that for a sum of *s*-functions we can transform each term individually and sum in the *z*-domain. For example, a loop filter may be a linear combination of a 1st- and a 2nd-order integrator. However, the transform of a product is not in general the same as the products of the transform of the multiplicands.

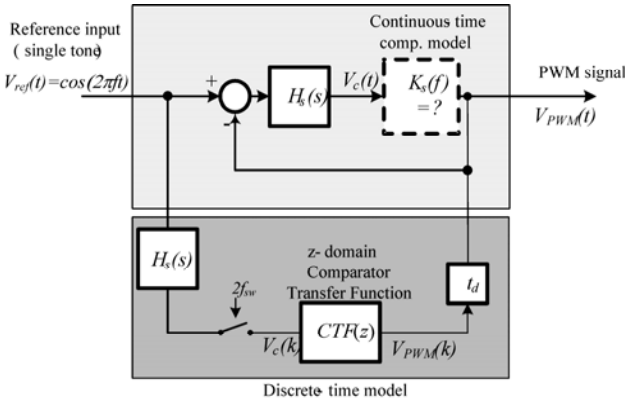

Figure 4. Using *CTF(z)* for finding the continuous-time comparator frequency response $K_s(f)$.

D. Comparator Hysteresis

A consequence of the feedback causality constraint mentioned above is that comparator hysteresis does not affect $H_z(z)$ since the hysteresis can be modeled as a positive feedback path (with gain *h*, see Fig. 1) that only shows up in the impulse response at time-lag zero and is thus removed. Moreover, the hysteresis does not change the slope of the carrier signal $V_c(t)$ since the positive feedback only adds a square wave (50% duty cycle) with zero slope at the sampling instants. Consequently, the comparator gain is unaffected so hysteresis does not factor in to the closed-loop *z*-domain transfer function either. The only effect of adding hysteresis is that the switching/sampling/oscillation frequency is changed when the loop is self-oscillating.

E. The Comparator Transfer Function CTF(z)

We now have a feedback loop that is described fully in discrete-time (*z*-domain) consisting of loop filter $H_z(z)$, comparator and gain K_z. However, external input signals (such as $V_{ref}(t)$) need in general to be treated as being in continuous-time until they get sampled by the comparator and injected into the *z*-domain loop at the equivalent *z*-domain comparator input node. Consequently, a closed-loop model accepting continuous-time input is shown in Fig. 3. The loop dynamics are governed by the *z*-domain Comparator-Transfer-Function *CTF*(*z*):

$$CTF(z) = \frac{K_z}{1 + K_z H_z(z)} \tag{6}$$

Note that the z-domain part needs to be treated as a "black-box" that we only can be affected by adding sampled signals via the comparator sampling process. The *z*-domain part also fully accounts for the feedback path.

F. Modelling Continuous-time input

The reference signal $V_{ref}(t)$ will thus first be filtered by $H_s(s)$ – in continuous-time – prior to being sampled and subjected to *CTF(z)* and then delayed by t_d. This gives the following input output transfer function:

$$G_{ref-out}(s) = \exp(-s \cdot t_d) \cdot H_s(s) \cdot CTF(z) \tag{7}$$

This transfer function mixes *s*- and *z*-domain and needs to be interpreted carefully. It is well-known that a continuous-time single-frequency sinusoidal input to an *s*-domain filter such as $H_s(s)$ gives a steady-state response

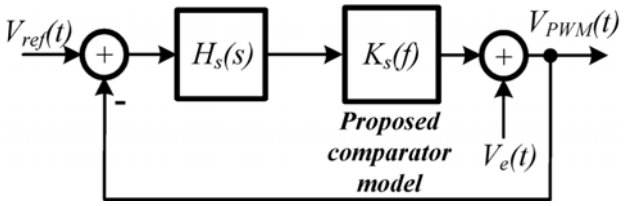

Figure 5. Versatile system model with $K_s(f)$

being a sinusoidal with an amplitude and phase given by the s-domain transfer function. When this sinusoid is sampled we get a frequency component of exact same frequency, amplitude and phase plus an infinity of spectral images (with same amplitude/phase) shifted by any multiple of the sampling frequency. The *z*-domain *CTF(z)* describes then how the amplitude and phase is modified by the *z*-domain loop which has cyclical transfer function being periodic with $2f_{sw}$, i.e. the sampling frequency. When the z-domain loop output signal is interpreted as a "real-world" continuous-time PWM signal we have a periodic spectrum with a component at the original system input frequency and at any frequency image. If we observe the PWM signal with a narrow-band filter centered on the stimulus frequency then the stated mixed-domain transfer function accurately describes the steady-state amplitude/phase change causes by the system. This is in fact true for any frequency even far beyond the switching rate. Such a narrow-band measurement is indeed what the popular gain-phase analyzer performs.

III. Continuous-time Comparator Model

This section derives the theoretical continuous-time transfer function $K_s(f)$ of the comparator corresponding to what a gain-phase analyzer will measure. The approach is that we apply a continuous-time single-frequency stimulus on $V_{ref}(t)$ and use the modeling frame-work presented to calculate the single-frequency response at both the comparator output (PWM node) and the comparator input. This procedure is shown in Fig. 4. The response at the output PWM node is directly given by (7). However, the comparator input has to be constructed as shown in Fig. 4 as the difference between $V_{ref}(t)$ and $V_{PWM}(t)$ being filtered by the loop filter $H_s(s)$. The resulting transfer function from V_{ref} to the comparator input is given by:

$$G_{ref-Cin}(s) = H_s(s)\left[1-\exp(-s\cdot t_d)\cdot H_s(s)\cdot CTF(z)\right] \tag{8}$$

The comparator transfer function $K_s(f)$ is then given by the ratio of (7) and (8):

$$\begin{aligned} K_s(f) &= \frac{\exp(-s\cdot t_d)\cdot H_s(s)\cdot CTF(z)}{H_s(s)\left[1-\exp(-s\cdot t_d)\cdot H_s(s)\cdot CTF(z)\right]} \\ &= \frac{K_z\cdot\exp(-s\cdot t_d)}{1+K_zH_z(z)-K_z\cdot\exp(-s\cdot t_d)\cdot H_s(s)} \\ &= \frac{K_z\cdot\exp(-s\cdot t_d)}{1+K_z\left(H_z(z)-\exp(-s\cdot t_d)\cdot H_s(s)\right)} \end{aligned} \tag{9}$$

By using the derived comparator transfer function $K_s(f)$ above, the loop can be modeled purely in the *s*-domain in the sense that the model accurately yields the single frequency in/out response. This property is a simple consequence of the fact that $K_s(s)$ is fitted to match the results obtained by the discrete-time model. However, such s-domain model does not account for the frequency images produced by the sampling (that are ignored by a narrow-band gain-phase analyzer).

When examining (9) we note first that if $H_s(s)$ plus delay-term is equal to its *z*-domain counter-part $H_z(z)$ at any frequency then the $K_s(f)$ would be frequency-independent and equal to the sampling gain K_z with the delay-term. The *z*-domain $H_z(z)$ can be viewed as $H_s(s)$ plus the delay-term being sampled. The sampling aliases the high-frequency response of the *s*-domain function and produces a periodic *z*-domain function. For example: a near infinite low-frequency gain of $H_s(s)$ results in near infinite gain peaks at every even multiple of f_{sw} in the *z*-domain counterpart. As seen from (9) this result in a near zero comparator gain $K_s(f)$ which can be explained by discrete-time loop treating a single frequency component near an even multiple of f_{sw} as a near DC component which gets suppressed by the high low-frequency s-domain loop-gain.

Conversely, the comparator gain $K_s(f)$ may become infinite at some frequencies when the denominator of (9) becomes zero which occurs when the difference between the *z*- and *s*-domain transfer functions (i.e. the aliasing error) is equal to $1/K_z$.

A. Closed-loop continuous-time single-frequency response

We can now replace the comparator block in Fig. 1 (comparator, delay and hysteresis) with $K_s(f)$ and obtain a system model (shown in Fig. 5) entirely in the *s*-domain which can be analyzed with standard methods. This *s*-domain model is accurate for a single-frequency narrow-band analysis but does as previously stated not account for frequency images due to the sampling.

For example, we can calculate the closed-loop response to an error-signal injected just prior to the feedback point on the PWM output node ($V_e(t)$ in Fig. 1 and Fig. 5) to the output. This error-suppression transfer function *ETF*(*s*) (a.k.a. the sensitivity function) is given by:

$$ETF(s) = \frac{1}{1+K_s(s)\cdot H_s(s)} \tag{10}$$

Note that this small-signal transfer function is valid at any frequency even beyond the switching rate.

For example, a current injected into the system output terminals causes some error voltage due to the open-loop output impedance (power stage and LC filter) which can be modeled as an error voltage $V_e(t)$. The control loop compensates by adjusting the power stage duty cycle in order to reduce the error voltage. Consequently, *ETF*(s) represents the ratio by which feedback changes the open-loop output impedance.

IV. The 1st-order integrator loop

We will analyze the simple 1-order loop with a pure integrator loop filter with integration time-constant τ according to (4) and (5). Note that $H_z(z)$ does not depend on the comparator delay t_d (if less than one sample) or the hysteresis *h*.

We add an external triangular carrier $V_{ext}(t)$ with amplitude V_t. The slope of the carrier $V_c(t)$ just prior to the transitions is the sum of the triangle wave slope and the slope of the triangular feedback ripple. This leads to the following expression for the comparator sampling gain:

$$K_z = \frac{4f_{sw}V_s}{4f_{sw}V_t+\frac{V_s}{\tau}} \tag{11}$$

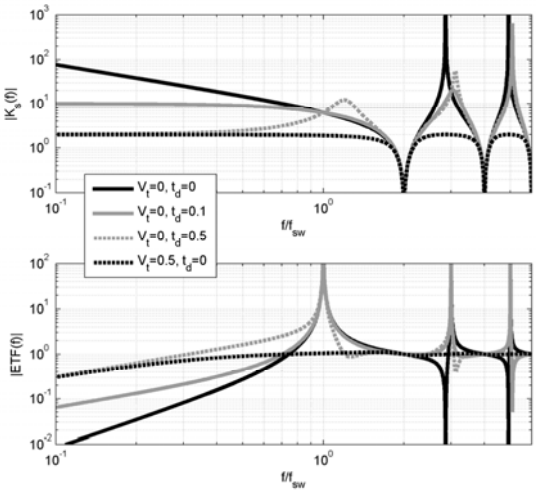

Figure 6. Calculated $K_s(f)$ and $ETF(f)$ for different loop configurations with an integrator loop filter.

Note that the comparator sampling gain K_z is reduced by the presence of feedback ripple. This means that K_z with the loop closed is less than traditionally assumed [1]:

$$K_{z[1]} = \frac{V_s}{V_t} \tag{12}$$

By finding the zero-frequency limit value of the rather complex expression for K_s (9) we can after some calculation find the continuous-time DC comparator gain:

$$K_{s,0} = \frac{V_s}{Vt + V_s \cdot \frac{t_d}{\tau}} \tag{13}$$

We note that for zero delay t_d, the DC gain is the ratio between the supply voltage and the triangle amplitude which is in perfect agreement with classical theory. When the triangle is removed, the loop will self-oscillate when a suitable hysteresis h is applied. For zero delay, it is noted that the DC gain is infinite which is in perfect agreement with sliding mode theory [3]. This can be visualized by comparator input waveform that will ramp linearly between the symmetrical hysteresis-bands which gives a zero input average for any output duty cycle and thus an infinite delay [9]. However, introducing a non-zero delay, the hysteresis-bands are exceeded giving a non-zero input average voltage and thus a finite gain as reflected in (13) [6], [9]. Notice that the delay also reduces the DC gain when using a triangular carrier contrary to classical theory [1].

For the self-oscillating case with hysteresis, the carrier slope is given by:

$$\left|\dot{V}_{c0}\right| = \frac{V_S}{\tau} \tag{14}$$

This means that the hysteretic comparator DC gain can be written as:

$$K_{s,0,HC} = \frac{V_s}{\left|\dot{V}_{c0}\right| \cdot t_d} \tag{15}$$

which is in perfect agreement with the expression found in [9].

The continuous-time comparator gain $|K_s|$ is plotted versus frequency in Fig. for 4 different configurations all using an integrator loop with $\tau=1$, $V_s=1$, $f_{sw}=1$. It is noted that all configurations have notches at even harmonics of f_{sw} reflecting that the z-domain loop filter has infinite gain here due to the frequency aliasing. The self-oscillating delay-free loop has a comparator gain that asymptotically at low frequencies behaves like an integrator in accordance with [9]. The integrator-like behavior combined with a finite DC gain due to a small delay lead to a simple 1-pole approximation to $K_s(f)$ in [9].

Note that all self-oscillating loops have a comparator gain equal to 2π at the switching frequency. This gives a total loop gain of unity (and -180 degree phase) when the integrator transfer function is included which is in agreement with the oscillation (e.g. the so-called Barkhausen criteria for oscillation). This is contrary to [12] that assumes a -6dB loop gain at f_{sw} which will not cause the desired oscillation. The underlying z-domain model always has a pole at $z = -1$ that accounts for the oscillation.

At frequencies just below odd harmonics of f_{sw} the self-oscillating loops have very high gain peaks, actually infinite gain peaks for the zero-delay hysteretic loop. These peaks give a very high error suppression at the peak frequencies which can be seen on the Error Transfer Function $ETF(s)$ plot. This means that the control loop can suppress errors at certain frequencies far beyond the switching rate. It is also noted that the hysteretic self-oscillating loop has far better error suppression compared to the triangular-carrier PWM loop at low frequencies due to the integrator-like behavior of the self-oscillating comparator. For zero comparator delay the errors-suppression of the self-oscillating loop exceeds the suppression of the triangle PWM loop by about 2 orders of magnitude at 5% of the switching rate (e.g. at the upper audio bandwidth for a 400kHz switching amplifier). Note here that V_t=0.5 is the lowest triangle amplitude (thereby the highest loop gain) that can be used without ripple instability at full modulation. However, the self-oscillating loops are extremely sensitive around odd-harmonics of the switching rate where $ETF(s)$ has high (infinite) gain.

V. Experimental Results

An experimental buck-converter was studied in three quite different control topologies; namely the standard PWM control, a phase-shift self-oscillating (SO) controller, and a hysteretic self-oscillating controller [10]. In all cases, voltage-mode feedback was used from the output terminal after an LC filter with 23kHz resonance. A PID control block with 10kHz double zeros was used to compensate for the 2nd-order response of the LC filter. The switching frequency was in all cases held around 400kHz. The three studied control schemes are illustrated in Fig. 7 and the experimental hardware shown in Fig. 11.

As demonstrated in prior art, the comparators in these different configurations can be expected to behave very differently, and no prior art modeling method has been demonstrated to account accurately for these differences.

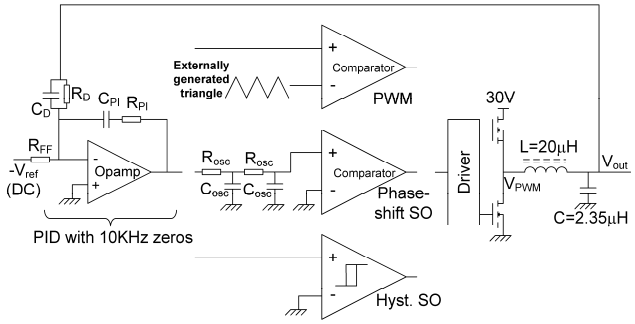

Figure 7. Experimentally tested control system configurations.

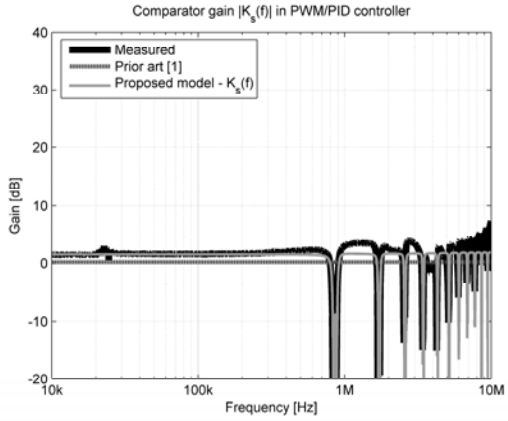

Figure 8. Measured and modeled PWM comparator gains.

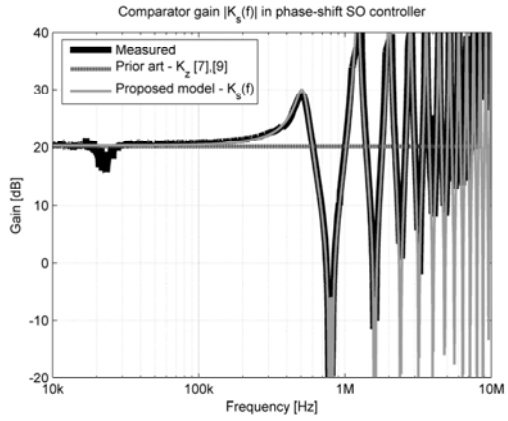

Figure 9. Measured and modeled phase-shift SO comparator gains

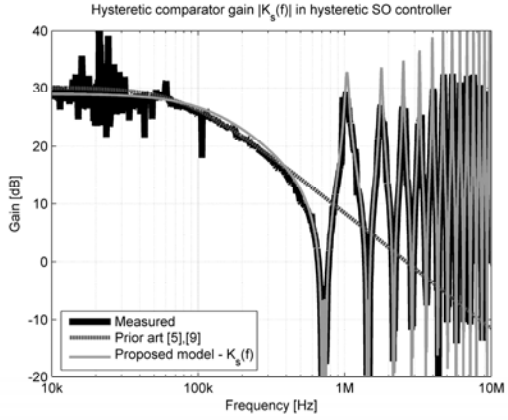

Figure 10. Measured and modeled hysteretic SO comparator gains

For verification of the proposed modeling approach, comparator magnitude responses and output impedances were measured using an AP Instruments Model 200 gain-phase analyzer. In all cases, 1000 points were measured, logarithmically spaced between 1kHz and 10MHz, and the variable injection generator feature was used to provide a good signal/noise ratio at low frequencies (by the use of a large perturbation) while avoiding injection locking at high frequencies (requiring a small perturbation.)

The continuous-time loop transfer function $H_s(s)$ was modeled in MATLAB as the product of the LC and PID *s*-transfer functions calculated from circuit component values. In the phase-shift self-oscillating controller case, two poles of the oscillation network (R_{osc}/C_{osc}) were added. The comparator and power stage delay was estimated to t_d = 80ns and modeled using a 2nd-order Padé approximation.

The carrier waveform $V_c(t)$ was found as the steady-state response of $H_s(s)$ to a 50% duty-cycle square-wave and calculated using a state-space representation. From this the carrier slope at the zero-crossings was found and used to calculate the comparator sampling gain K_z.

Figures 8-9-10 show comparisons between measurements of comparator magnitude responses and predictions made using relevant prior art models and the proposed modeling approach. In general, the proposed modeling method allows an unprecedented level of accuracy to be obtained from DC to above 10 times the switching frequency. In particular, the +6dB magnitude response increase at the switching frequency (needed to ensure oscillation) for the phase-shift SO controller [9] is accounted for, likewise is the single-pole behavior [5] of the hysteretic comparator. At the same time, the model handles the standard PWM block nicely, although there are 2-3dB errors at some frequencies above the switching frequency. Note that in all measurements, the LC filter resonance at 23kHz produces visible measurement noise, especially in the hysteretic SO controller, which has the highest loop gain (and therefore is the most noise sensitive at the LC resonance) among the studied controllers. As expected, the standard clocked PWM controller has the lowest gain followed by the phase-shift and hysteretic self-oscillating controllers. The gain of the hysteretic loop could possible be increased further by aligning the PID zeros with the LC resonance so that the total response is closer to an integrator. In this case, the DC gain is only limited by the power stage delay and not by the phase shift due to mismatching pole/zeros. An intuitive explanation of the lower gain of the phase-shift SO controller is that the oscillation poles add excessive phase lag that results in a DC gain reduction similar to a very large delay. For example, the theoretical $K_s(f)$ graph in Fig. 6 for a hysteretic 1st -order loop with an extreme delay equal to half a switching period shows a gain-peaking just above the switching rate very much similar to the plots for the phase-shift controller.

A. Output Impedance measurements

Figures 12 and 13 show the measured and modeled output impedances for the three controller configurations. The modeled output impedance is the product of the open-loop LC filter impedance multiplied by the error transfer function (sensitivity function) $ETF(s)$. The clocked PWM controller only reduces the impedance up to around 60kHz while the self-oscillating controllers are effective at much

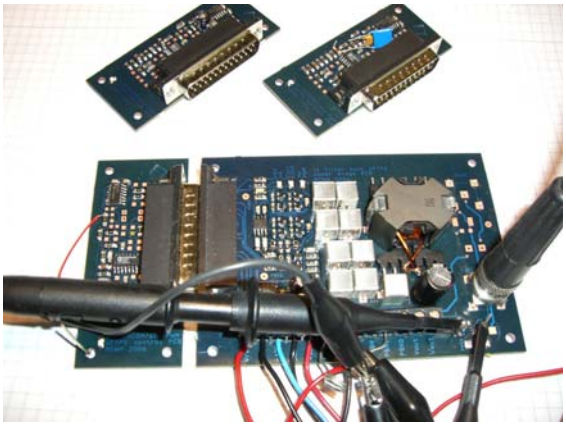

Figure 11. Experimental hardware – a common buck power stage with exchangeable control PCBs.

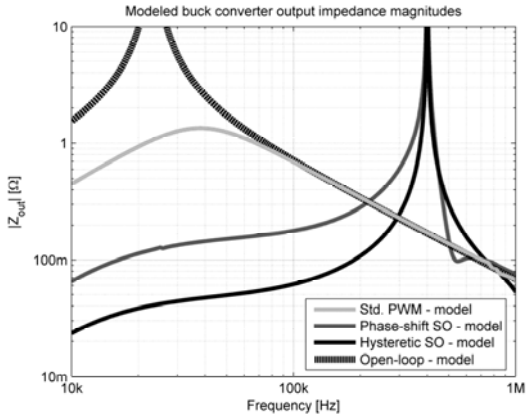

Figure 12. Modeled output impedances of studied control systems, all systems switch at 400kHz.

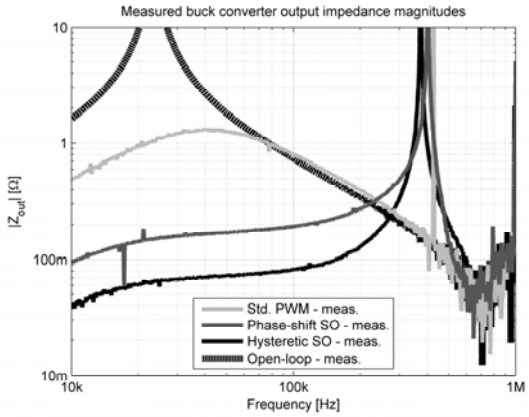

Figure 13.Measured output impedances; systems switch at 420khz, 400khz and 380kHz respectively.

higher frequencies (up to the 200-300kHz range). The output impedance goes to infinity as expected at the switching frequency. However, in certain narrow frequency bands above the switching rate the model predicts that the controller actually reduces the output impedance compared to open-loop. Moreover, the impedance drops faster above f_{sw} for the phase-shift controller than for the hysteretic. This is in excellent agreement with the measurements. However, the measurements diverge at high frequencies above 700kHz from the model due to stray inductance around the filter capacitor.

VI. Conclusion

A versatile modeling approach has been proposed applicable to a large class of switching control systems The model is fully in continuous-time thanks to the introduction of the comparator gain $K_s(f)$ which reflects the underlying sampling nature but uses readily observable continuous-time signals.

The model gives valuable insights into the very different behaviors of various control schemes that now can be modeled and compared in the same framework. In this paper, the model has been used to demonstrate a close connection between the often separately considered clocked PWM and self-oscillating (sliding mode) control techniques. Furthermore, the model has been verified against measurements with excellent accuracy even far beyond the switching frequency.

One important limitation of the model is that it only applies to 50% duty cycle operation. Future work will hopefully extend the model to any duty cycle.

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Optimized Envelope Tracking Power Supply for Tetra2 Base Station RF Power Amplifier

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***Abstract* – An ultra-fast tracking power supply (UFTPS) for envelope tracking in a 50kHz 64-QAM Tetra2 base station power amplification system is demonstrated. A simple method for optimizing the step response of the PID+PD sliding-mode control system is presented and demonstrated, along with a PLL-based scheme for locking the switching frequency to an external clock. High UFTPS efficiency (up to 95%), very low ripple ($5mV_{pp}$) and a fast step response (10µs) are obtained from a single-phase buck converter with a 4^{th}-order output filter. This ripple performance is demonstrated to be critical in the considered application. Also demonstrated is the effect of non-zero UFTPS output impedance on envelope tracking performance. At 13W average (156W peak) RF output, a reduction of DC input power consumption from 93W (14% efficiency) to 54W (24% efficiency) is obtained by moving from a fixed RF power amplifier supply to envelope tracking.**

I. INTRODUCTION

In RF power amplification systems, the use of envelope-tracking (ET) supply voltage [1-4] for the RF power amplifier (RFPA) has been shown to be an effective solution to increasing RFPA efficiency. A basic example of such a system is shown in Figure 1. This scheme is especially interesting in modern digital radio systems, where advanced modulation techniques (such as QAM, Quadrature Amplitude Modulation) are used to pack more data into a given bandwidth, but at the cost of an increased peak-to-average RF signal power ratio. For example, the 10dB (approximately) peak-to-average ratio in a typical QAM signal means that the transmission of a 10W RF signal actually requires an RFPA capable of 100W peak output power, generally leading to an inefficient RF amplification process. Envelope tracking solves this by effectively adjusting the RFPA peak power rating dynamically with the required power level.

From a power electronics perspective, an interesting problem lies in implementing ultra-fast tracking power supplies (UFTPSs) for this application. To be effective, the UFTPS should be able to vary its output voltage at the same rate as the RFPA output amplitude varies, as reflected by the RF signal bandwidth. Depending on the type of RF signal being transmitted, the UFTPS ripple voltage can also be very important. This paper considers the step-response optimization of a UFTPS for the 50kHz QAM transmission mode in a Tetra2 [5] base station, an application that calls for relatively high output power along with relaxed tracking bandwidth and very low output ripple voltage.

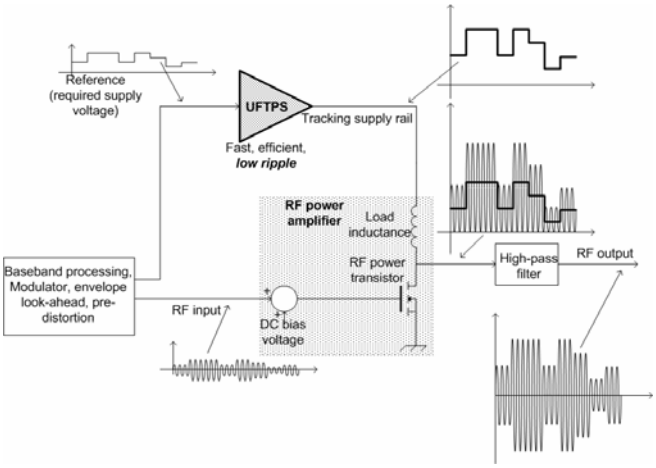

Figure 1 Basic RFPA system with envelope tracking power supply.

II. UFTPS SOLUTION

For a Tetra2 base station, initial studies have lead to the UFTPS specifications in Table 1. It has been demonstrated in prior art [6] that a buck converter with 4^{th} order output filter is capable of meeting the step response and output voltage/current rating with reasonable ripple and efficiency. For an optimized UFTPS, the ripple should be further reduced and output impedance should be added to the list of parameters to be controlled. Specification of the UFTPS output impedance is a topic not often discussed, so this is currently best done experimentally.

The hysteretic PID+PD control scheme proposed in [6] is again considered in this paper (see Figure 2) since this is a very simple and effective method for controlling the 4^{th} order filtered buck converter. This control scheme capitalizes on the very large loop gain and bandwidth [7] provided by the self-oscillating (sliding mode) inner PID loop. The inverting-input configuration was chosen since this greatly simplifies small-signal analysis, producing more readily interpretable results.

Table 1 Output specifications of UFTPS

Output voltage	10-30V
Output current	0-20A
Output voltage step response	10µs
Output ripple voltage	< $10mV_{pp}$
Max. output impedance	? (100mΩ area)

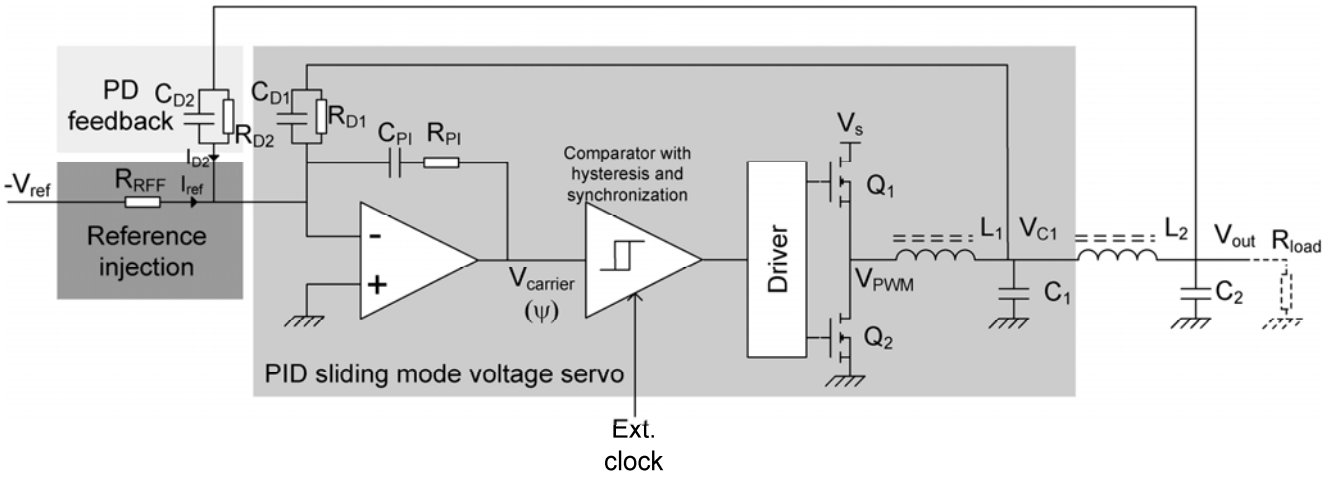

Figure 2 Considered UFTPS solution – sliding PID+PD controlled 4th order filtered buck with switching synchronization and inverting reference input.

III. Control System Modeling and Optimization

The transfer function from reference to output of the UFTPS should ideally be a Bessel-type low-pass filter [8], since this means that over/under-shoot is avoided. It is especially important to avoid undershoot since this could drive the RFPA into clipping and thereby lead to excessive distortion of the RF output.

Assuming sliding mode operation, the closed PID loop can be modeled easily. The basic sliding equation [9], [10], with L_2 and C_2 removed, can be written as:

$$\psi(t)=0 \Rightarrow \psi(s)=0$$

$$\psi(s)=V_{carrier}(s)=0=[V_{C1}(s)\cdot G_{D1}(s)+V_{out}(s)\cdot G_{D2}(s)]\cdot G_{PI}(s)$$

where the PD branches are modeled as

$$G_{D1}(s)=1+sR_{D1}C_{D1} \wedge G_{D2}(s)=1+sR_{D2}C_{D2}$$

and the PI part of the compensator is modeled as

$$G_{PI}(s)=\frac{1+sR_{PI}C_{PI}}{sR_{PI}C_{PI}}$$

The closed-loop transfer function of the inner loop, from V_{out} (with L_2, C_2 removed) to V_{C1} is given by:

$$G_{CL,inner}(s)\equiv\frac{V_{C1}(s)}{V_{out}(s)}=-\frac{G_{D2}(s)}{G_{D1}(s)}$$

The closed-loop transfer function of the outer loop will generally be given by

$$G_{CL,outer}(s)\equiv\frac{V_{out}(s)}{V_{ref}(s)}=G_{ref}(s)\cdot\frac{G_f(s)}{1+G_f(s)G_{fb}(s)}$$

where $G_f(s)$ and $G_{fb}(s)$ denote the forward and feedback path transfer functions respectively and $G_{ref}(s)$ represents any dynamics in series with the reference input. The forward path can be described as the impedance

$$G_f(s)=\frac{V_{out}(s)}{I_{D2}(s)}=\frac{1}{G_{D2}(s)}\cdot G_{CL,inner}\cdot\frac{1}{s^2L_2C_2+s\frac{L_2}{R_{load}}+1}$$

while the feedback path is simply given as the admittance

$$G_{fb}(s)=\frac{I_{D2}(s)}{V_{out}(s)}=\frac{1+sR_{D2}C_{D2}}{R_{D2}}$$

The reference input is described as the admittance

$$G_{ref}(s)=\frac{I_{ref}(s)}{V_{ref}(s)}=\frac{1}{R_{ref}}$$

Now, these can be combined, eventually leading to the closed-loop transfer function:

$$G_{CL,outer}(s)=-\frac{R_{D2}}{R_{RFF}}\cdot\frac{1}{s^3L_2C_2R_{D1}C_{D1}+s^2\left(L_2C_2+\frac{L_2}{R_{load}}R_{D1}C_{D1}\right)+s\left(\frac{L_2}{R_{load}}+R_{D1}C_{D1}+R_{D2}C_{D2}\right)+2}$$

This is a 3-pole transfer function, so there is an obvious opportunity for realizing a 3rd order Bessel filter by placing the poles correctly. In practice, the complex pole pair can be placed first, and then the real pole can be positioned as required by a pre-filter arrangement.

When actually designing the PID+PD control system, it is of practical importance that the first LC filter section (L_1/C_1) is made fast enough to allow its dynamics to be ignored, even under large-signal conditions. The inner loop PD networks should then be designed to ensure that the carrier voltage responds with a triangle waveform to the PWM voltage – this intuitively ensures that the carrier oscillates properly within the

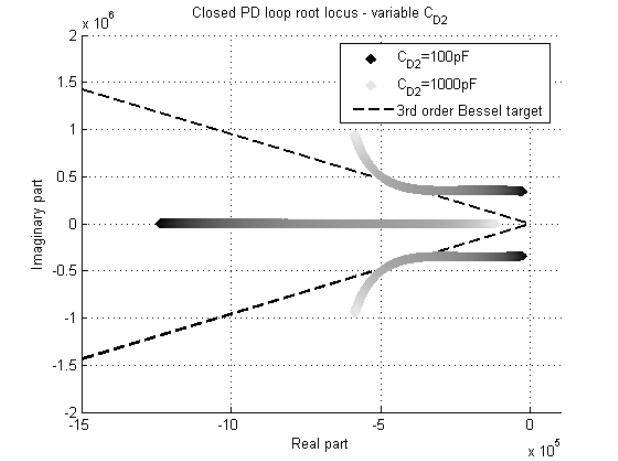

Figure 3 Complex pole placement by C_{D2} tuning following an appropriate choice of $G_{D1}(s)$.

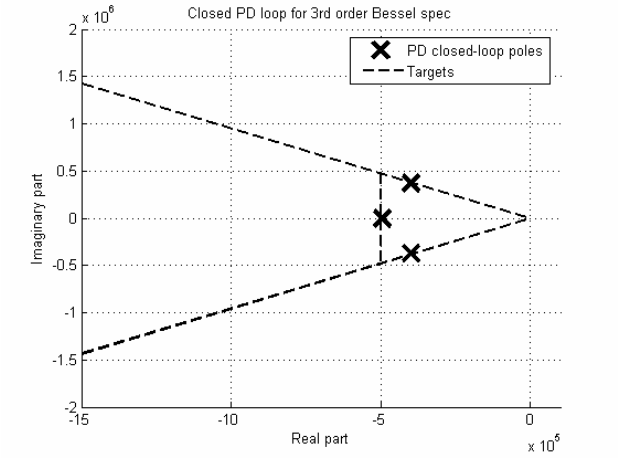

Figure 4 Real pole verification after complex pole placement. Real pole is easily adjusted by pre-filtering.

hysteresis window. This is because the switching frequency should be controllable by adjusting the hysteresis window for the shown switching frequency control scheme to function.

It can also be shown [11] that having a loop filter that approximates an integrator at high frequencies (from around the switching frequency and up) maximizes the small-signal gain of the hysteretic comparator.

The design of the second LC section is more straight-forward; its cut-off should be in the vicinity of the RF signal bandwidth in order to allow a suitably fast step response and maximum ripple attenuation. As a final adjustment, the impedance level of the 4th order LC filter should be scaled appropriately to minimize output impedance while avoiding excessive ripple-induced power losses.

Simulation is useful for determining the limits for the inner loop and outer loop designs under large-signal conditions, such as a 10-30V output voltage step in the considered application.

For a 10µs step response with 1MHz switching frequency, the filter and compensator parameters in Table 2 were found suitable.

Table 2 Filter and inner loop parameters

LC filter corner frequencies (open-loop)	*360kHz, 27kHz*
Inner PD time constant	0.77µs
L1	*2µH*
L2	*2µH*
C1	*200nF*
C2	*8.8µF*

The optimization method using $G_{CL,inner}(s)$ is very useful when an approximate filter and compensation network design has been found, and the step response is to be optimized. As illustrated in Figure 3, this can be done by plotting a root-locus for the closed-loop system for a variable C_{D2}. With a C_{D2} ensuring the right placement of the complex pole pair selected, the real pole can now be checked against the desired location (as shown in Figure 4) and, if necessary, re-located by an appropriate pre-filter. In the control system design implemented for this paper, no pre-filtering was necessary.

Another closed-loop parameter of interest is the output impedance. Since the RFPA supply current will fluctuate with the instantaneous output power level (which varies a lot with a QAM signal), it is an advantage if the UFTPS provides a low output impedance so that the correct V_{out} is maintained at all times.

For the hysteretic PID+PD control solution, the very high loop gain of the inner, oscillating loop [7] means that the first filter section (L1/C1) contributes negligibly to the overall closed-loop output impedance. This can be analyzed quite accurately through the use of a finite-gain model of the hysteretic comparator [12]. When adding the second (L_2/C_2) filter stage and the outer control loop, the closed PID loop can therefore practically be considered an ideal voltage source, greatly simplifying the analysis. Standard amplifier theory states that the closed-loop output impedance $Z_{out,CL}(s)$ of an amplifier with open-loop output impedance $Z_{out,OL}(s)$ and loop gain $G_{loop}(s)$ is given as:

$$Z_{out,CL}(s) = \frac{Z_{out,OL}(s)}{1 + G_{loop}(s)}$$

In the case of the PID+PD controller with negligible inner loop output impedance, the following will apply for the open outer loop:

$$Z_{out,OL}(s) = \frac{sL_2}{s^2 L_2 C_2 + \frac{L_2}{R_{load}} + 1}$$

$$G_{loop}(s) = G_{CL,inner}(s) \cdot \frac{1}{s^2 L_2 C_2 + \frac{L_2}{R_{load}} + 1}$$

This leads to the closed-loop output impedance of:

$$Z_{out,CL}(s) = \frac{sL_2}{s^2 L_2 C_2 + s\frac{L_2}{R_{load}} + 1 + \frac{G_{D2}(s)}{G_{D1}(s)}}$$

Note that since $G_{D1}(s)$ and $G_{D2}(s)$ are both close to unity at low frequencies, the PD loop only reduces the low-frequency output impedance contribution of L_2/C_2 by a factor of 2. It is also apparent that the impedance level of the filter has a direct influence on the overall output impedance, since L_2 directly figures as a proportional component in the transfer function.

The accuracy of the derived output impedance expression is indicated in the section on experimental results.

IV. Switching Frequency Phase Locking

In order to ensure that the switching frequency of the self-oscillating control system is well-defined and controllable at system level, a switching frequency control mechanism is desirable. A number of approaches have been proposed in prior art, including the injection of synchronization pulses [13], the use of a PLL (Phase Locked Loop) acting on a variable delay [14] or the use of an FLL (Frequency Locked Loop) acting on the hysteresis window of the comparator [6]. The approach proposed in this paper is to combine an FLL with a PLL, in order to provide the phase-locking, zero-frequency-error properties of a PLL while maintaining the wide dynamic range of the FLL.

The latter is important in a self-oscillating UFTPS, where the significant frequency disturbances that occur constantly would drive most phase-frequency detector (PFD) circuits beyond their linear operating range of typically +/-180°. The proposed switching frequency control scheme is illustrated in Figure 5. The overall block has the basic functionality of a comparator with hysteresis, with the slight twist that the hysteresis window is controlled so that phase lock is achieved between the external (synchronization) lock and the PWM output.

The small-signal properties of the FLL are analyzed in [15], where the end result is the model of the FLL incorporated into the overall model in Figure 6. The power converter (oscillation process) is modeled as a gain that reflects the influence of the hysteresis window on the switching frequency. The MMV (Monostable MultiVibrator a.k.a. one-shot) is average-modeled as a gain that represents the conversion from switching frequency to voltage. For the PLL, the phases of the external clock and the PWM signal are the quantities to be matched. The PFD accomplishes a translation from phase error to voltage, a proportional process, and the PI compensator ensures that the steady state phase error is zero while also allowing closed-loop stability in spite of the integration introduced in the translation from PWM frequency to phase. Worth noting is that the closed FLL is practically a VCO (Voltage Controlled Oscillator), but usually with a pole (arising from the error integrator) that reflects that the FLL has limited bandwidth. This adds dynamics that should be taken into account in the PLL design, especially since most textbook examples [16] assume that the VCO is fast.

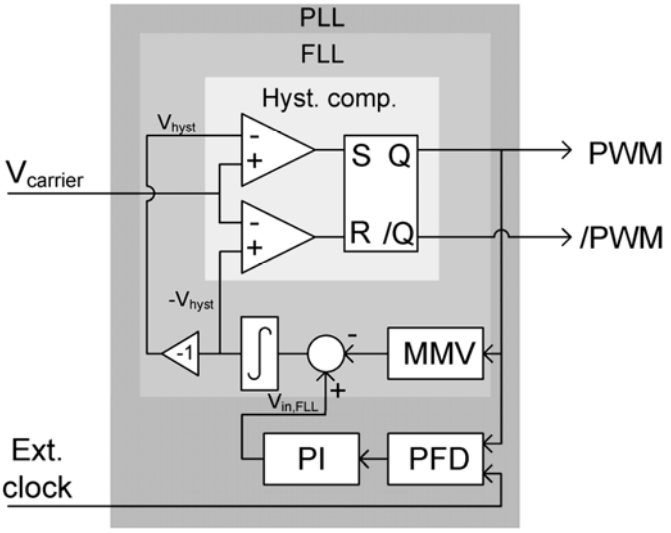

Figure 5 Nested-FLL based PLL synchronization for a hysteretic self-oscillating control system.

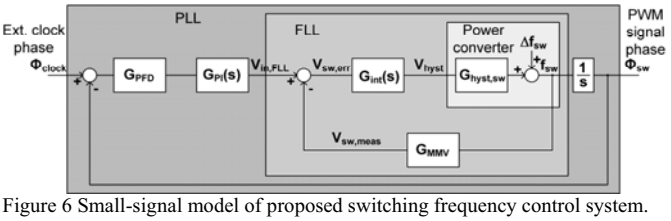

Figure 6 Small-signal model of proposed switching frequency control system.

V. Experimental Results

A test setup similar to the one described in [17] was used for experimental verification of the RF amplification system. The main power components, the RFPA and the UFTPS, are shown in Figure 9.

A key feature of the 4th-order filtered buck converter, ripple voltage that is strongly switching frequency dependent, is evident from Figure 7. A switching frequency increase of 42% from 700kHz to 1MHz reduces output ripple by a factor of 5 (14dB), which is necessary as indicated in Figure 8. The 25mVpp ripple at 700kHz f_{sw} is enough to cause -73dBr (relative to transmitted signal plateau) intermodulation (IM) products at 700kHz offset from the RF carrier at 360MHz. This is enough to lead to non-compliance with the -80dBc 500kHz-5MHz wideband noise limit specified in the Tetra2 standard. RFPA output power is 13W average, corresponding to 156W peak given the 10.8dB peak-to-average ratio of the used 64-QAM signal. With the 200W (CW) class-AB RFPA, this roughly corresponds to maximum output.

The efficiency of the UFTPS prototype is indicated in Figure 10. The efficiency peaks at 95%, but is usually in the 85-90% range. Note that the idle power consumption of 4W (a lot of which is due to a rather inefficient house-keeping power supply) is included in the shown figures.

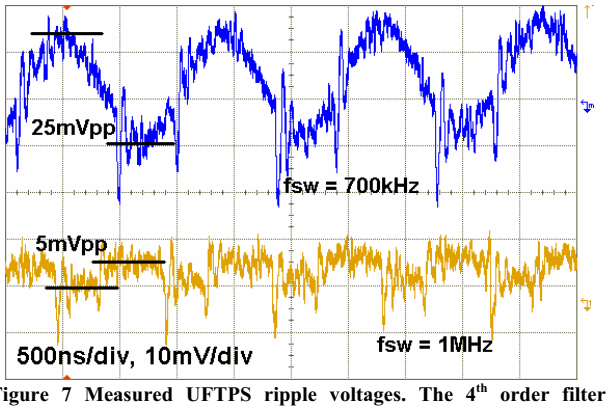

Figure 7 Measured UFTPS ripple voltages. The 4th order filter provides large ripple reductions for modest f_{sw} increases.

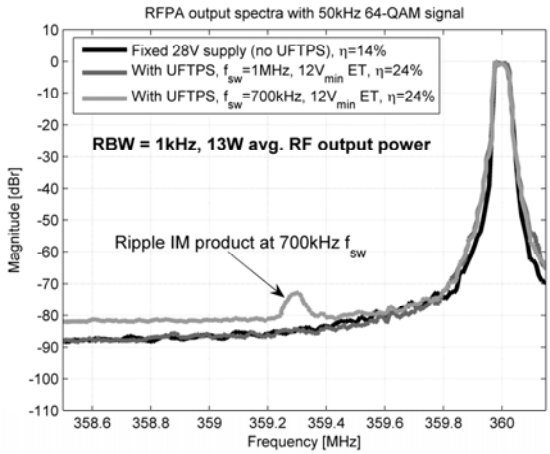

Figure 8 RFPA output spectra. UFTPS ripple of $5mV_{pp}$ with f_{sw}=1MHz keeps ripple IM product below -86dB relative to carrier plateau level.

The FLL/PLL switching frequency locking scheme can be evaluated from Figure 11. Before the output voltage step, the PWM signal is in phase with the external clock, but the change in duty cycle caused by the voltage step produces a switching frequency disturbance. Most of the disturbance is compensated for by the FLL, but a phase error is left, which is removed by the PLL in around 20µs. Since both FLL and PLL control bandwidths need to be considerably lower than the switching frequency, this is about as fast as the system can reasonably be expected to respond.

The UFTPS design output impedance as well as precision of the derived model are assessable from Figure 14. In spite of the idealization of the inner control loop, the derived model is accurate within 1dB up to several times the RF bandwidths. The output impedance itself stays below 300mΩ.

The basic tracking performance of the UFTPS is examined in Figure 12, where loaded and un-loaded UFTPS responses to a representative reference input are compared. As can be seen, adding the RFPA unfortunately somewhat spoils the almost-perfect, Bessel-optimized step response of the un-loaded case. The reason behind the effect of the RFPA load on the UFTPS step response can be found by examination of Figure 13 and 15.

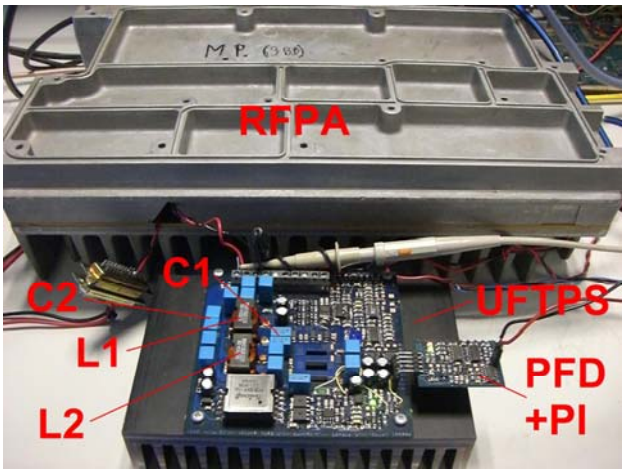

Figure 9 Part of experimental setup – UFTPS and RFPA.

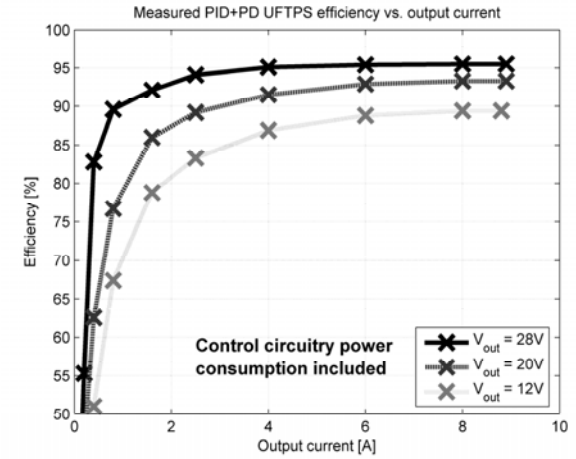

Figure 10 Measured UFTPS DC output efficiencies with 40V input. Idle losses of 4W limit the low-power efficiency.

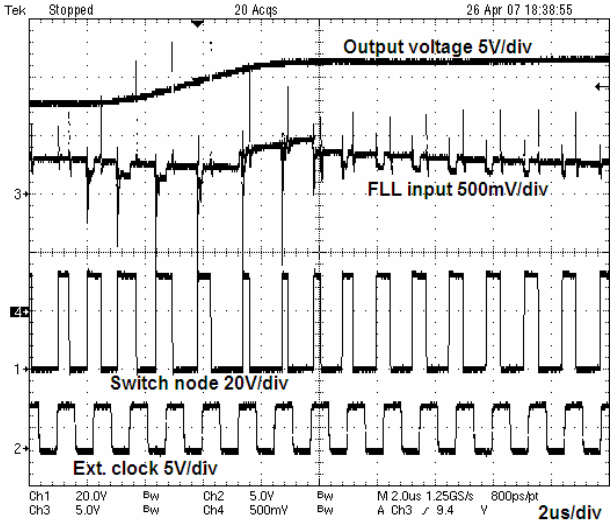

Figure 11 Measured PLL and switching frequency response to an output voltage step. PWM signal phase slips from clock but is brought back in around 20µs.

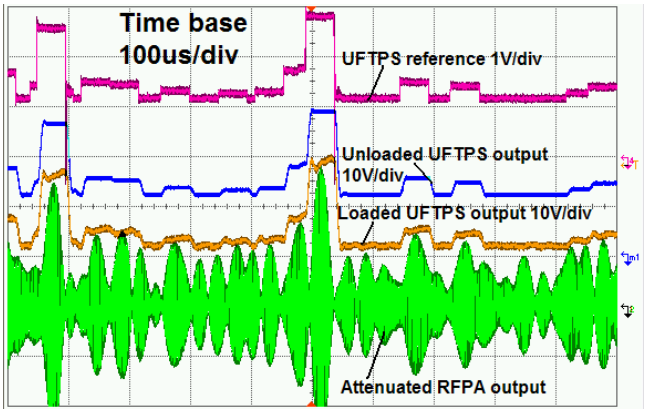

Figure 12 UFTPS output with and without RFPA load. Response is ideal (no overshoot) without the load.

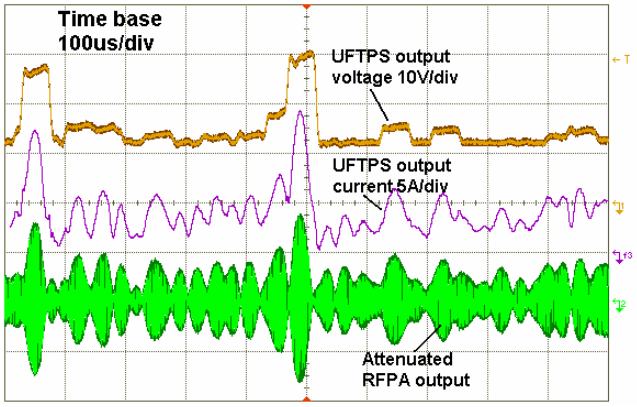

Figure 13 UFTPS output voltage/current when driving the RFPA at maximum (13W average) output power.

The RFPA draws a supply current that varies with the instantaneous output level, peaking at 14A. The measured RFPA load current was recorded along with the UFTPS reference and output voltages, and the derived UFTPS reference-to-output and output impedance transfer functions used to simulate the effect of real wave forms on the UFTPS output, as shown in Figure 15. Since the derived model is linear, the UFTPS responses to reference voltage and load current can be calculated separately. The UFTPS output impedance causes un-wanted output voltage deviations of up to $2V_{pp}$, explaining the less-than-ideal loaded UFTPS output voltages measured. In practice, non-zero output impedance must be expected, and it seems reasonable to specify the UFTPS output impedance based on a maximum load current induced output voltage deviation. The combination of a realistic load current waveform and an accurate output impedance model hereby provides a workable solution for dealing with the effect of UFTPS output impedance.

The adjacent channel power ratios (ACPR) of the non-linearized RFPA system are evident from Figure 16. The measured RFPA output spectra were filtered with a 25kHz root-raised cosine (RRC) filter as prescribed by the Tetra2 standard. The carrier power reference (0dBc) is defined as the total in-band power of the carrier, which is roughly 3dB above

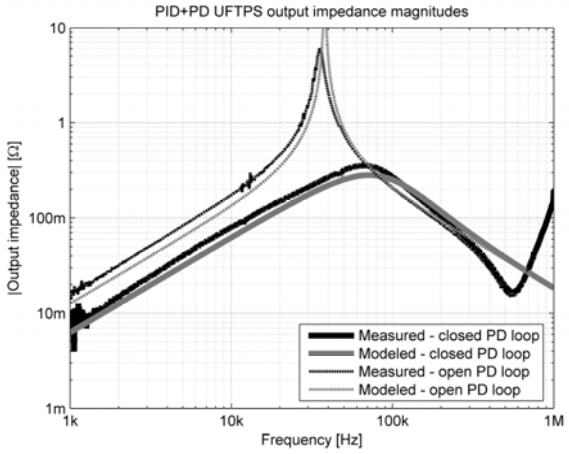

Figure 14 Measured and modeled output impedance with and without the outer (PD) loop closed. Model is accurate up to 300kHz.

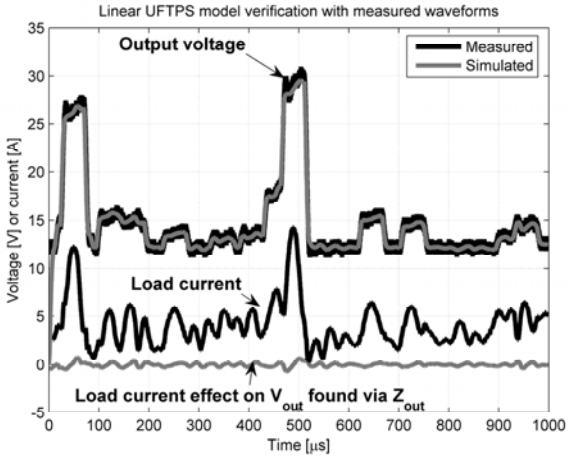

Figure 15 Simulation of UFTPS output response to measured reference and load current waveforms. Non-zero output impedance accounts for sub-optimal tracking.

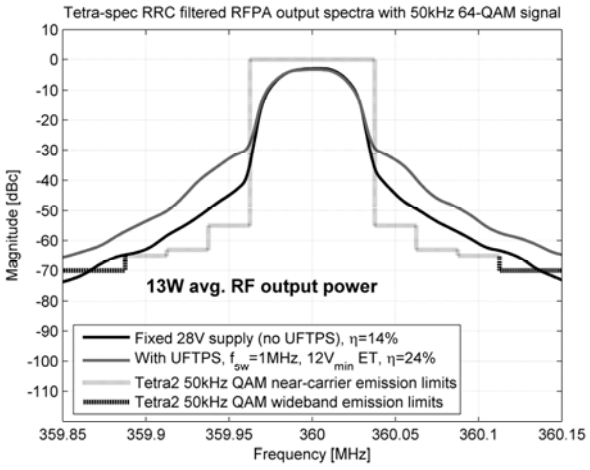

Figure 16 Processed RFPA output spectra for ACPR evaluation. 25+dB of linearization is needed for compliance with 1st ACPR spec of -55dBc (at +/-37.5kHz.)

the RRC filtered mid-carrier plateau due to the 50kHz carrier bandwidth.

The use of envelope tracking leads to a 10dB degradation of 1st ACPR, which will have to be corrected for through an improved RFPA linearization system. Note that extra linearization is normally incorporated into any RFPA system, with or without envelope tracking.

Finally, the efficiency improvement obtained by the use of the UFTPS instead of a fixed 28VDC supply for the RFPA is (printed in Figure 8 and Figure 16) is 10 percentage points, from 14% with 28VDC to 24% with 12-28V supplied by the UFTPS. Practically, this corresponds to a reduction of DC supply power from 93W to 54W – quite a substantial reduction. The 28VDC efficiency was measured with power provided directly from a laboratory power supply.

VI. Conclusion

The practical effects of two somewhat hard-to-specify UFTPS performance parameters; ripple voltage and output impedance, have been experimentally demonstrated. It has been shown that the effects of these, in the case of a Tetra2 base station transmission system, can be limited to a non-problematic level by proper design of the UFTPS. The 4th-order filtered self-oscillating PID+PD controlled buck converter has been shown to be a simple and cost-effective solution to this end.

Theoretically, a number of refinements have been proposed to the PID+PD controlled UFTPS known from prior art. A simple s-domain model of the sliding-mode PID+PD was derived in compliance with classical sliding mode control theory, and used in a step response optimization method that leads to a Bessel-type step response using a minimum of control system components. The UFTPS output impedance was also expressed accurately using the sliding-mode modeling framework.

Additionally, a variable-hysteresis based switching frequency control technique has been presented. This allows synchronization of the sliding mode control system to an external clock, a very useful feature in a radio system.

Sizeable reductions of RFPA system power consumption (38.7W for a 13W average RF output level) have been demonstrated at relatively high RF output power, although accompanied by an increase in RFPA distortion.

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Self-Oscillating Soft Switching Envelope Tracking Power Supply for Tetra2 Base Station

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Abstract – **This paper presents a high-efficiency, high-bandwidth solution to implementing an envelope tracking power supply for the RF power amplifier (RFPA) in a Tetra2 base station. The solution is based on synchronous rectified buck topology, augmented with high-side switch zero-current switching (ZCS) implemented with a series inductor and an external clamping power supply. Combined with advanced power stage components (die-size MOSFETs), a high-performance fixed-frequency self-oscillating (sliding mode) control strategy and a 4th-order output filter, this leads to a compact, effective and efficient overall solution switching at 1MHz with 88-95% efficiency. In a class-AB RFPA amplifying a 50kHz bandwidth QAM Tetra2 signal at 4.6W average output power, the use of tracking supply voltage reduced power dissipation by 25W.**

I. INTRODUCTION

Power amplification in many modern digital radio systems requires low distortion while operating with signals with significant amplitude dynamics, such as QAM (Quadrature Amplitude Modulation.) Because of this, linear RF power amplification (class-A or AB) is the standard solution, with associated low efficiency. One technique for increasing the RFPA efficiency is to adjust its supply voltage in accordance with the instantaneous output level so that power consumption is minimized while avoiding RFPA clipping. To maximize the efficiency improvement, the power supply for the RFPA should be capable of tracking the envelope of the RF signal, hence the term envelope tracking power supply. The term "ultra-fast tracking power supply" (UFTPS) coins the fact the dynamics required for envelope tracking are generally much faster than what is required for typical DC power supplies. This paper presents a solution for designing and implementing a UFTPS suitable for powering the RFPA in a base station for the Tetra2 communications network standard. The considered transmission mode is 50kHz 64-QAM (QAM with 64 amplitude/phase combinations per transmitted symbol.) While the RF signal bandwidth is relatively modest, the Tetra2 standard prescribes that output spectral components at typical switching frequency offset from the main carrier must be below -90dBc. This is much stricter than what is required in, for example, W-CDMA [1] or EDGE [2], and generally means that the UFTPS output ripple voltage becomes important. The combination of modest bandwidth and low ripple has been shown to be achievable at high efficiency using the low-cost combination of a single-phase buck converter with a 4th order filter [3]. This paper elaborates on this basic approach by proposing a soft-switching method to increase the UFTPS efficiency, as well as a voltage control system providing lower output impedance.

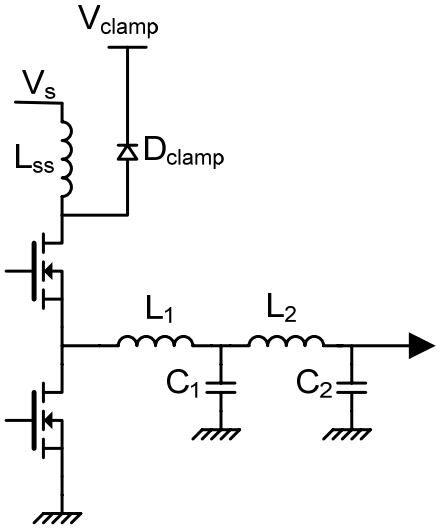


Figure 1 Considered power topology; buck with 4th order output filter and ZCS high-side turn-on.

II. POWER STAGE TOPOLOGY

For the synchronous buck converter operating at high output current, the dominant switching loss is the hard-switched turn-on of the high-side (HS) switch, because:

- The drain-source voltage is maximum while the drain current ramps up
- Reverse recovery in the low-side (body) diode causes an increase in turn-on current

A simple and pragmatic solution to this is to insert a small inductor L_{ss} in series with the high-side (HS) switch in order to remove the voltage from the switch during commutation [5], [6]. The problem with this is that the inductor has to be demagnetized before the next switching cycle in order to provide a zero turn-on current for the high-side switch. The solution used in this work is to use a diode and a voltage above V_s to demagnetize the series inductor when the HS switch turns off, as illustrated in Figure 1. Idealized voltages and currents in this topology when the output current is significantly higher than the ripple current in L_1, are illustrated in Figure 3. A turn-on of the HS switch begins with the pull-down of the drain voltage (which is ideally instantaneous) and

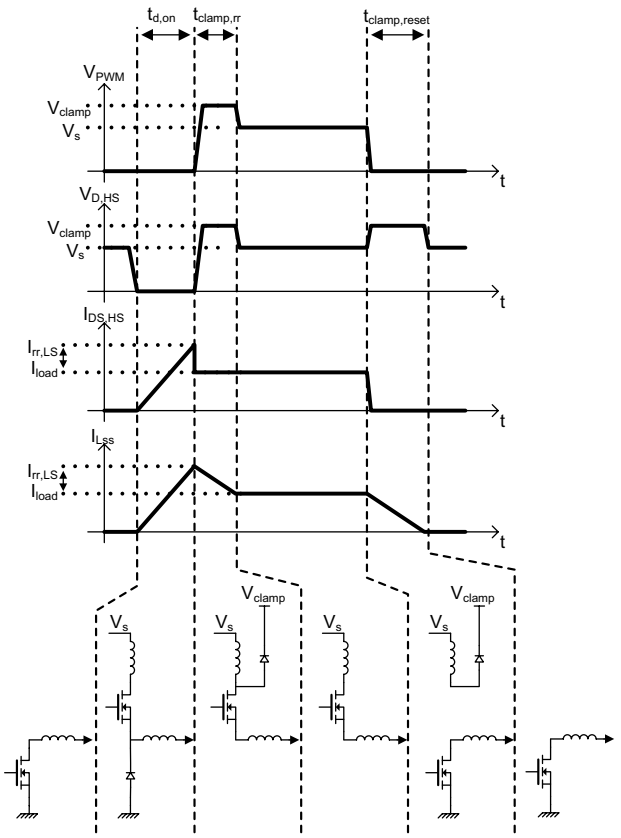


Figure 3 Principal functioning of ZCS sync. buck power stage. Soft-switching inductor ensures zero-current high-side turn-on.

the following rise of HS drain current, the rate of which is controlled by L_{ss}. Due to reverse recovery of the low-side (LS) MOSFET body diode, L_{ss} will be charged to a current higher than the output current. The delay from HS switch turn-on to the actual PWM voltage rise is approximately:

$$t_{d,on} = \frac{L_{ss}\left(I_{out} + I_{rr,LS}\right)}{V_s}$$

where $I_{rr,LS}$ is the LS body diode peak reverse recovery current. Following the positive transition of the PWM voltage, the resulting excess energy in L_{ss} will be clamped. The duration of this clamping interval is:

$$t_{clamp,rr} = \frac{L_{ss} I_{rr,LS}}{V_{clamp} - V_s}$$

At HS turn-off, all energy in L_{ss} is ideally returned to the clamping supply in the time of:

$$t_{clamp,reset} = \frac{L_{ss} I_{load}}{V_{clamp} - V_s}$$

The power returned to the clamping supply is:

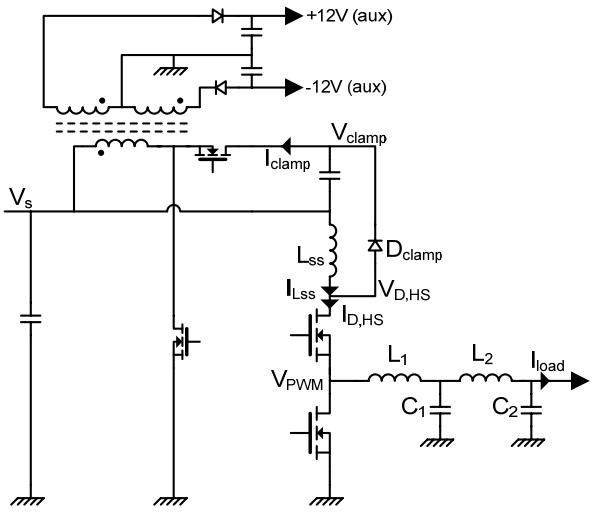


Figure 2 Complete power system implementation; a small auxiliary converter maintains clamp voltage and generates housekeeping supplies.

$$P_{clamp} = f_{sw} \cdot \frac{1}{2} L_{ss}\left(I_{load} + I_{rr,LS}\right)^2$$

For the representative numerical example of f_{sw}=*1MHz*, L_{ss}=*100nH*, I_{load}=20A, $I_{rr,LS}$=*10A*, P_{clamp} is *45W*, so the clamped energy should be recycled to avoid a substantial efficiency penalty. This could be done through the main power supply (that already generates V_s) or using a dedicated on-board converter. In any case, the clamping supply must be capable of sinking a current of:

$$I_{clamp} = \frac{P_{clamp}}{V_{clamp} - V_s}$$

Note that the average current in the diode D_{clamp} is heavily dependent on the choice of V_{clamp}. Using the same numbers as in the above, and assuming V_s=*40V*, V_{clamp}=*75V*, I_{clamp} is found to be 1.8A, which can be handled with modest (in comparison with the main converter) power components. If on-board, the clamping supply can also be used to generate the low-voltage supplies for driving the control circuitry of the UFTPS locally, as shown in Figure 2.

The exact design of the soft-switching circuitry involves a tradeoff between a number of mechanisms:

- L_{ss} should be large enough to be the main limititation factor in $dI_{D,HS}/dt$.
- L_{ss} should be minimal to minimize clamp power
- $t_{d,on}$ should be minimized to increase self-oscillating controller performance [6], [7] => minimize L_{ss}
- $V_{D,HS}$ and V_{PWM} should be kept below the MOSFET/driver voltage ratings => low V_{clamp}
- I_{clamp} should be kept low to minimize D_{clamp} conduction losses => high V_{clamp}

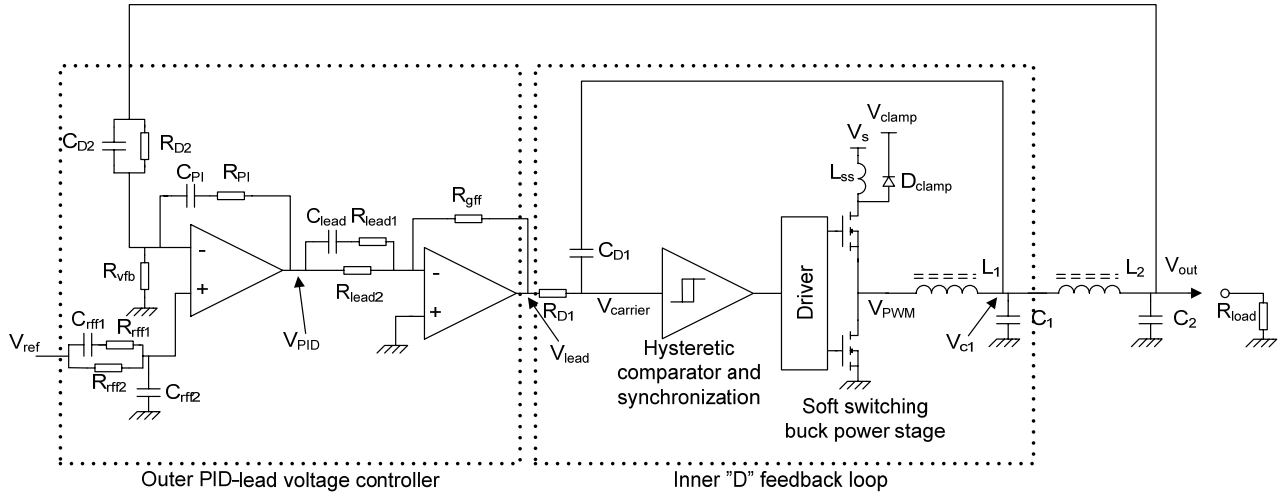


Figure 4 Dual-loop (D + PID-lead) controller for low output impedance though high gain in outer loop

A good solution would use a minimal L_{ss} for ensuring soft switching, while taking advantage of the voltage ratings of the power MOSFETs and the driver circuit for minimizing I_{clamp}. In the considered application, the 40V supply voltage and the availability of very good 100V rated switching components provides the voltage headroom needed for effective use of the considered ZCS topology.

III. VOLTAGE CONTROL SYSTEM

The voltage control system implemented in the presented design is an evolution of the simple PID+PD controller proposed in [7]. While being relatively easy to design and implement, the PID+PD has the disadvantage of low loop gain in the outer loop. This means that the output impedance of the second filter section is relatively unchanged by the feedback, resulting in high output impedance. In order to decrease output impedance, loop gain must be increased, but this also means that the outer open-loop transfer function must have a slope at low and medium frequencies, increasing the difficulty with obtaining adequate phase margin. The proposed controller structure (see Figure 4) solves these problems relatively simply through:

- An inner derivative ("D") loop that transforms the inner filter and power stage into an integrator
- An outer PID loop with added lead compensation, providing high loop gain and adequate phase margin

The shown implementation requires only two opamps, and allows a non-inverting reference-to-output transfer function.
An additional feature necessary for maintaining low ripple across a wide range of output voltages is switching frequency control [7]. The switching frequency of the hysteretic control loop varies as:

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{hyst}}{K} + t_d}$$

where D is the converter duty cycle, V_{hyst} is the hysteresis window, K is twice the carrier signal dV/dt at $D=0.5$ and t_d is the comparator/power stage time delay. Since the output filter is 4th-order, even a small drop in switching frequency results in a dramatic ripple voltage increase. Keeping the switching frequency constant allows tight ripple specs to be kept over a wide D range while not switching excessively fast at $D=0.5$.

IV. VOLTAGE CONTROL SYSTEM MODEL

Using the infinite-gain model [7], [8] of the hysteretic comparator or sliding mode theory [8], [9], the closed inner loop is found to behave as an integrator:

$$G_{inner}(s) \equiv \frac{V_{c1}(s)}{V_{lead}(s)} = -\frac{1}{sR_{D1}C_{D1}}$$

This comes naturally, since the assumed infinite loop gain forces the inner filter pole pair to an infinitely high frequency, making the feedback zero dominate the closed-loop dynamics. The shown model is also coherent with the basic sliding-mode control property of reducing the closed-loop system order by 1 [8]. The lead compensator is characterized by:

$$G_{lead}(s) \equiv \frac{V_{lead}(s)}{V_{PID}(s)} = -\frac{R_{gff}}{R_{lead2}} \cdot \frac{1 + s(R_{lead1} + R_{lead2})C_{lead}}{1 + sR_{lead1}C_{lead}}$$

The PID compensator dynamics can be described as:

$$\frac{V_{out}(s)}{Z_{D2}(s)} = V_{-}(s)\left[\frac{1}{R_{vfb}} + \frac{1}{Z_{D2}(s)} + \frac{1}{Z_{PI}(s)}\right] - \frac{V_{PID}(s)}{Z_{PI}(s)}$$

with

$$Z_{D2}(s) = R_{D2} \| \frac{1}{sC_{D2}} \qquad Z_{PI}(s) = R_{PI} + \frac{1}{sC_{PI}}$$

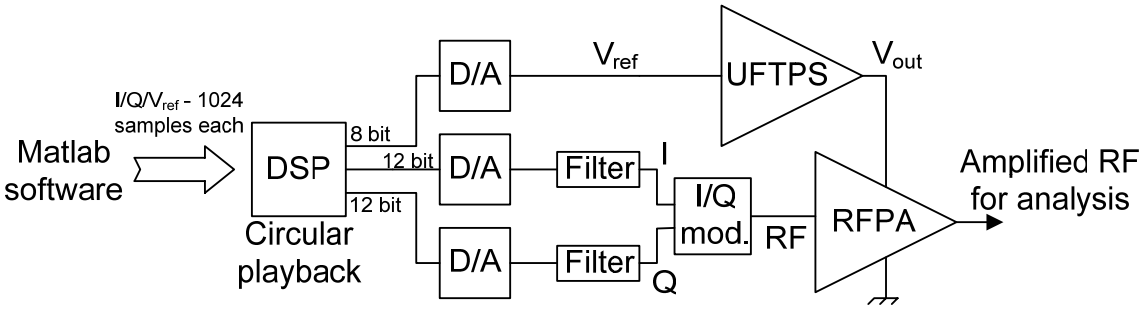


Figure 5 Simplified system test setup as implemented

The choice of reference injection point leads to:

$$V_{-}(s) = V_{+}(s) = V_{ref}(s) \cdot G_{rff}(s)$$

with

$$G_{rff}(s) = \frac{1 + s(R_{rff1} + R_{rff2})C_{rff1}}{1 + s\left[(R_{rff1} + R_{rff2})C_{rff1} + R_{rff2}C_{rff2}\right] + s^2 R_{rff1}R_{rff2}C_{rff1}C_{rff2}}$$

Recognizing that the following has to apply:

$$V_{PID}(s) = \frac{V_{out}(s)}{G_{filter2}(s) \cdot G_{inner}(s) \cdot G_{lead}(s)}$$

where

$$G_{filter2}(s) = \frac{1}{1 + s\frac{L_2}{R_{load}} + s^2 L_2 C_2}$$

allows the overall reference-to-output transfer function to be written as:

$$\frac{V_{out}(s)}{V_{ref}(s)} = \frac{G_{rff}(s) \cdot G_{filter2}(s) \cdot G_{inner}(s) \cdot G_{lead}(s) \cdot \left[1 + \frac{Z_{D2}(s)}{R_{vfb}} + \frac{Z_{D2}(s)}{Z_{PI}(s)}\right]}{G_{filter2}(s) \cdot G_{inner}(s) \cdot G_{lead}(s) + \frac{Z_{D2}(s)}{Z_{PI}(s)}}$$

Assuming the closed inner loop to present negligible output impedance (as resulting from infinite assuming loop gain) to the outer loop leads to the following expression for the overall UFTPS output impedance:

$$Z_{out}(s) = \frac{Z_{filter2}}{1 + G_{loop,outer}} = \frac{sL \cdot G_{filter2}(s)}{1 + G_{filter2}(s) \cdot G_{inner}(s) \cdot G_{lead}(s) \cdot G_{PID}(s)}$$

where $G_{PID}(s)$ is given by:

$$G_{PID} \equiv \frac{V_{PID}(s)}{V_{out}(s)} = \frac{R_{PI}}{R_{D2}} \cdot \frac{(1 + sR_{D2}C_{D2}) \cdot (1 + sR_{PI}C_{PI})}{sR_{PI}C_{PI}}$$

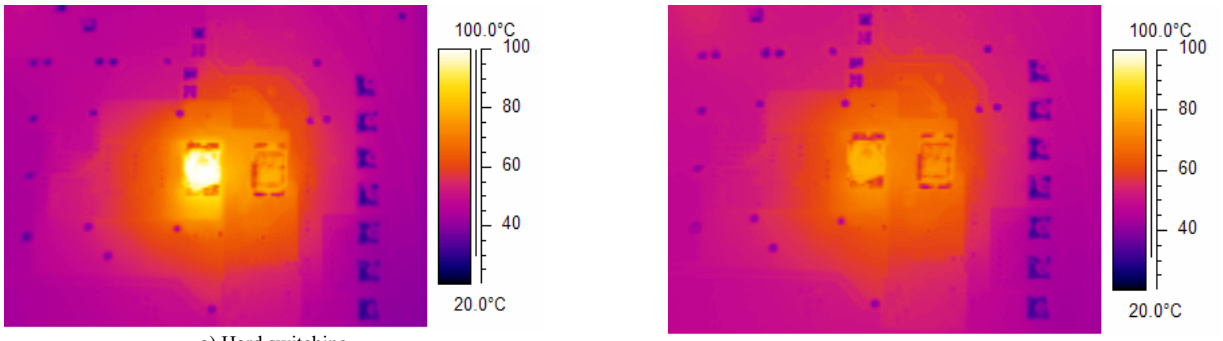
A more accurate output impedance prediction would require the use of a finite-gain hysteretic comparator model [7].

V. PROTOTYPE DESIGN/IMPLEMENTATION

To demonstrate the low-cost potential of the 4th order filter topology, identical, stock power inductors (Coilcraft SER2012-202) were used for L_1 and L_2. Similarly, C_1 and C_2 were of relatively inexpensive polyester film construction. The filter *L1=L2=2uH* and *C1=0.94uF*, *C2=4.4uF* allowed a reasonable compromise between ripple current, cost and open-loop output impedance, while providing corner frequencies of 37kHz and 169kHz. For the soft switching circuitry, a 100nH air cored inductor was used for L_{ss}, while 4 SMA packaged 100V schottky diodes in parallel provided a low-inductance D_{clamp}. An inexpensive Coilcraft POE300F-12 (Power-Over-Ethernet flyback transformer) was used for the clamping converter inductor/transformer. Die-size, 10mΩ/100V IRF6644s were used as main power MOSFETs. For the voltage control system, R_{D1}*=1kΩ*, C_{D1}*=33pF* were selected as a compromise between carrier signal amplitude (promoting a larger $R_{D1}C_{D1}$ time constant) and obtaining effective derivative action (promoting a smaller $R_{D1}C_{D1}$ time constant.) Derivative action in the inner loop ensures the carrier signal is triangular (assuming that the inner loop dominates high-frequency feedback), which intuitively ensures proper hysteresis-mode oscillation. The PID and lead compensators were designed to provide an outer loop crossover frequency of 250kHz and sufficient phase margin to avoid ringing in the closed-loop response. The reference input filter network was designed to provide a fast step response without overshoot by canceling closed-loop poles and zeros, and replacing these with new poles and zeros. Simulation was used extensively for the design process, and the linear model used for verifying that the design was operating predictably in a linear manner, as well as for fine-tuning the controller time constants. Key parameters in the implemented control system are given in Table 1.

Table 1 Voltage controller parameters in prototype

Component	Value	Component	Value
R_{D1}	*1kΩ*	R_{D2}	*18kΩ*
C_{D1}	*33pF*	C_{D2}	*180pF*
R_{gff}	*1kΩ*	R_{vfb}	*2kΩ*
R_{lead1}	*47Ω*	R_{rff1}	*5.6kΩ*
R_{lead2}	*1kΩ*	C_{rff1}	*4.7nF*
C_{lead}	*4.7nF*	R_{rff2}	*2.7kΩ*
R_{PI}	*1.8kΩ*	C_{rff2}	*4.7nF*
C_{PI}	*3.7nF*		



a) Hard switching

b) Soft switching

Figure 6 Thermal images of power MOSFETs on prototype during 10V/4A output, with and without soft switching.

VI. COMPLETE SYSTEM SETUP

The test setup used to demonstrate system functionality is illustrated in

Figure 5. Baseband QAM RF data (*I* and *Q*) and the UFTPS control signal V_{ref} was precalculated based on a random bit sequence using Matlab. This allowed 10µs look-ahead and peak-hold for V_{ref} as well as delay tuning to be implemented easily. The same processing could also have been done real-time in a DSP. The digital $I/Q/V_{ref}$ data sequences had a length of 1024 samples, and were preprocessed to ensure continuous waveforms with looped playback. The data was uploaded into the DSP of a standard Motorola base station transceiver PCB to provide the QAM modulated RF signal at 360MHz and the accompanying V_{ref}. An 80W (with a continuous sine wave output) base station class-AB RFPA was used for the RF amplification. Due to the high peak-to-average power ratio of the QAM signal (10.86dB in the 1024 sample sequence used), the 80W RFPA could only provide 6.5W of average output power. In practice, when linearity is taken into consideration, less than 6.5W is more realistic.

VII. EXPERIMENTAL RESULTS

The prototype UFTPS is shown in Figure 7, the PCB contains the auxiliary converter (upper 25% of PCB) as well as the main converter. Modeled and measured step responses of the prototype design are compared in Figure 8. The linear model is accurate and a 15-20µs response time was achieved with almost no overshoot. In the tracking application, the supply voltage and RFPA output waveforms were measured as shown in Figure 9. The bandwidth of the UFTPS is evidently sufficient for tracking the 50kHz QAM signal envelope, and the delays in the RF and supply voltage signal paths are well matched.

The functionality of the soft-switching circuitry can be assessed from Figure 10. At 20A output current, it takes around 50ns to charge L_{ss}, and the voltage across the high-side MOSFET is zero for this duration. During the HS "on" phase, the switch node rings at about 30MHz, corresponding with the 100nH L_{ss} and the 300pF C_{ds} of the used MOSFETs. At HS turn-off, L_{ss} demagnetizes in around 35ns. In spite of all the extra circuitry and ringing, the soft-switching power stage actually reduces power losses, as indicated from the measured efficiency curves in Figure 13. Hard switching measurements were made simply by (low-inductively) shorting L_{ss}. The efficiency gain is on the order of 0.5-2%, with the gain being the highest at low output voltage, where the power losses are more significant compared to the output power. It can also be observed that the efficiency improvement only occurs when the output current is larger than the ripple current in L_1 (around 2.5A at D=0.5); this is natural since the synchronous buck power stage naturally has full soft switching when its output current is lower than the ripple current. The practical effect of the soft-switching circuitry on MOSFET temperatures is demonstrated in Figure 6; at a modest output of 10V/4A, the case temperature of the high-side MOSFET was reduced by 25°C. In a design targeting PCB cooling of the MOSFETs, soft switching could thus be a design enabling factor.

The derived small-signal model is further examined in Figure 11 and Figure 12. The inner loop model is seen to be very accurate at high frequencies, with significant deviation at lower frequencies, primarily due to finite gain in the hysteretic comparator [10]. This is reflected in the resulting loop gain in the outer loop. Closed-loop output impedance is also affected by this, although reduced loop gain cannot account for all the LF deviation between modeled and measured output impedance. Layout parasitics and/or measurement technique may account for the remaining deviation. Still, the quite simple output impedance model provides a good clue to the actual output impedance.

The output ripple of the prototype design is very low (less than 10mV peak-peak) as can be seen from the measured spectra in Figure 14. Changes in the inductances of L_1 and L_2 with DC bias account for the measured ripple voltage increase at 20A output current.

The generated QAM modulated RF signal spectrum is shown in Figure 15, although the noise floor could not be measured with the used spectrum analyzer, it is generally clear that the RF signal is relatively pure. Spectral purity allows the distortion products from the RFPA to be clearly visible. The RFPA output was initially measured with constant 28VDC supply (generated by the UFTPS) and 5.0W average output power, the result is shown in Figure 16. Distortion products are (roughly) below -30dBc and input DC power was 57W, indicating an overall efficiency of 8.8%.

Figure 7 Prototype PCB mounted on over-size heat sink. Power MOSFETs are located on the bottom side of the PCB.

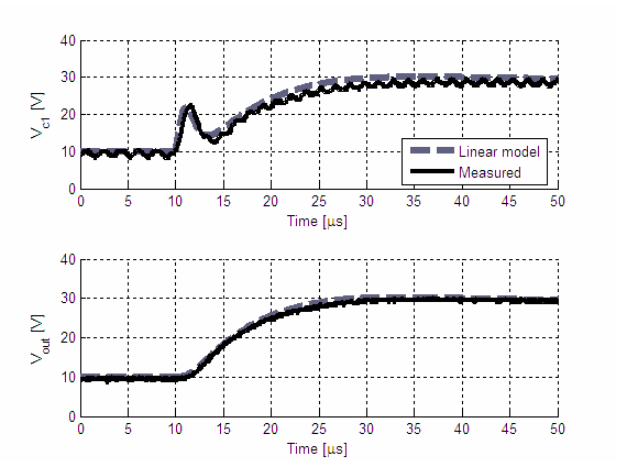


Figure 8 Modeled and measured step response of prototype design. Linear model predicts measured performance very well and an overall 15-20µs response time is evident.

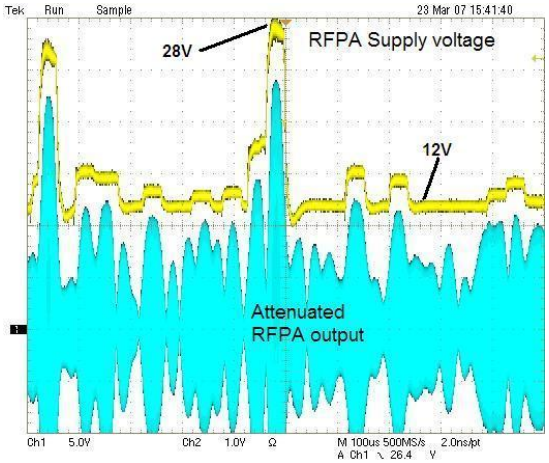


Figure 9 Measured V_{out} (top, yellow) and RFPA output (bottom, blue) with 12V minimum envelope tracking. High peak-to-average of QAM is evident.

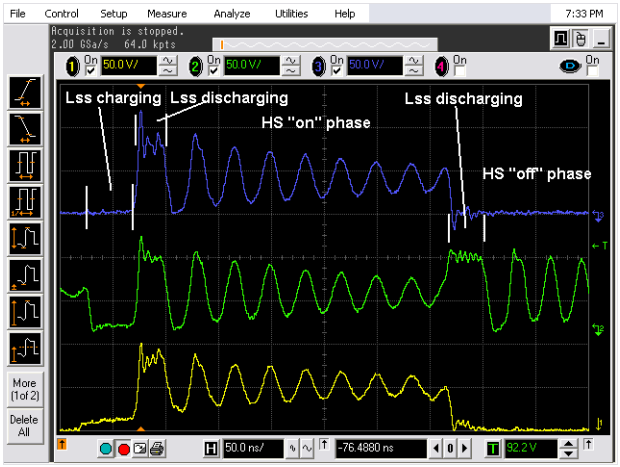


Figure 10 Measured switch node (blue), HS drain (green) and HS gate (yellow) voltages at HS turn-on and turn-off with 20A output current

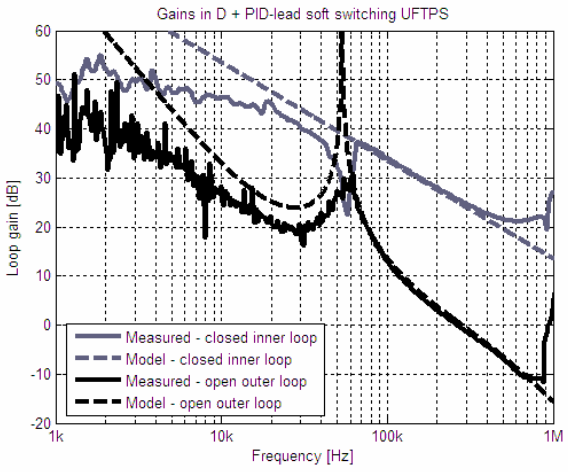


Figure 11 Modeled and measured inner loop closed-loop gain (grey) and loop gain in outer loop (black.) Inner loop deviates from integrator behavior at LF due to finite hysteretic comparator gain, which is reflected in outer loop.

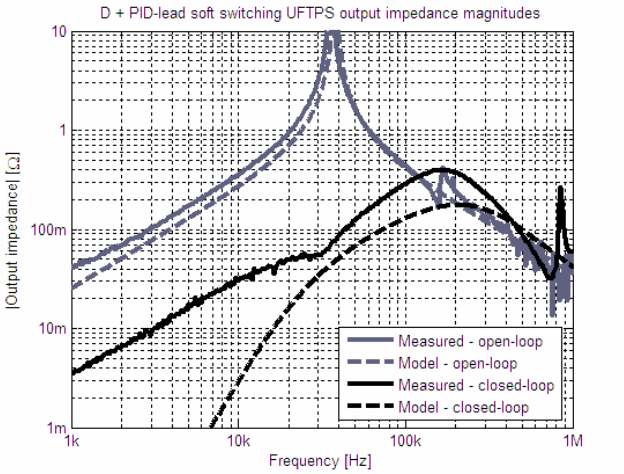


Figure 12 Modeled an measured open-loop (grey) and closed-loop (black) output impedances. Closed-loop performance deviates strongly at LF, partially due to gain loss in closed inner loop.

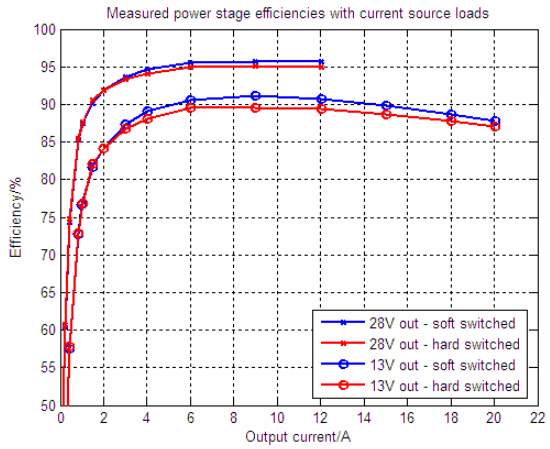


Figure 13 Measured prototype efficiency with and without soft switching. Soft switching circuitry provides an improvement of 0.5-2 percentage points when DC output current exceeds the ripple current in L_1.

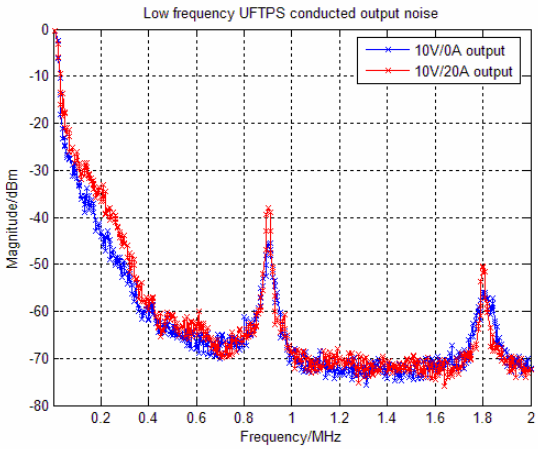


Figure 14 Measured output ripple spectra during no-load (blue) and full-load conditions with f_{sw}=900kHz; ripple fundamental stays below -39dBm (≈10mV$_{pp}$.)

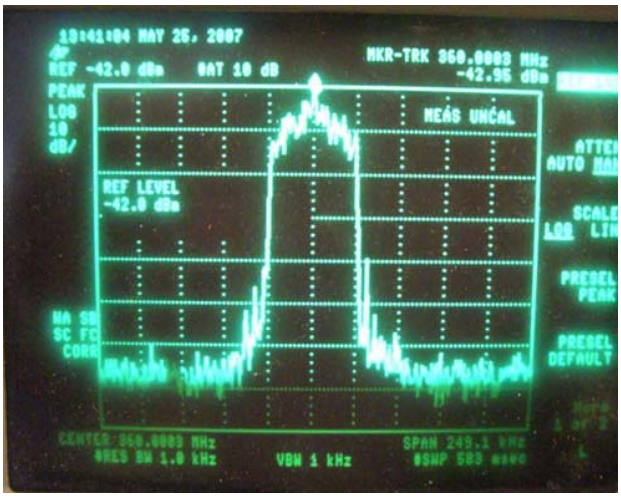


Figure 15 Measured input QAM signal spectrum. Dynamic range is large and distortion low, so that RFPA distortion will be dominant.

Figure 16 Measured RFPA output spectrum with fixed supply (28V); avg. output RF power was 5.0W, DC input power was 57W; 8.8% overall efficiency.

Figure 17 Measured RFPA output spectrum with tracking supply (12V-28V); avg. RF output power was 4.6W, DC input power was 29W; 15.9% overall efficiency.

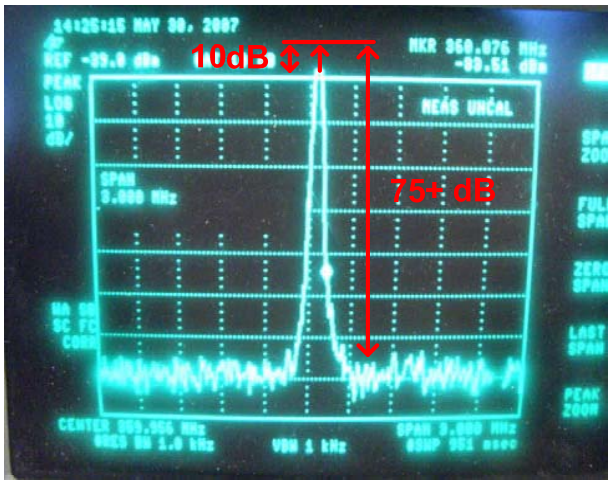


Figure 18 Measured RFPA output spectrum with tracking supply (12V-28V.) Ripple intermodulation products are below the -75dBc noise floor of spectrum analyzer and/or RF signal.

With variable supply (with a 12V minimum limit imposed), similar distortion (see Figure 17) was achieved at 4.6W output power. The DC input power in this case was 29W, so the overall efficiency was 15.9%. The use of envelope tracking thus nearly doubled overall efficiency, saving around 25W (estimated for identical output powers) of RFPA power dissipation, without detrimental effects on the RFPA output spectrum. RF signal pre-distortion [1] could probably be used to increase the available output power for a given distortion level, leading to a further increase in overall efficiency. The effect of ripple on the RFPA output ripple spectrum is too low to be measured with the used equipment, as indicated in Figure 18. The RF carrier is 10dB above-scale, so the measurement noise floor is at around -75dBc. There are no ripple intermodulation spurs to be seen, so given the .-90dBc wideband noise level specified for Tetra2, it is safe to say the UFTPS ripple is within 15dB of the required level.

IIX. CONCLUSION

A low-cost, high-efficiency DC/DC topology suitable for medium-bandwidth, low-ripple envelope tracking applications at high power levels has been presented. This has been shown (by efficiency measurements and thermal imaging) to provide increased efficiency, and, also useful, thermal stress reduction in the high-side MOSFET through zero-current switching at high output currents. The low-cost potential of the topology has been demonstrated through the use of a single-phase buck and stock magnetic components.

A suitable voltage control scheme, providing relatively low output impedance from the 4^{th} order output filter has also been modeled and demonstrated. The prototype power supply has been shown to allow substantial power consumption savings in an 80W class-AB RF power amplifier in a 50kHz 64-QAM Tetra2 transmission application.

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A 0.35µm 50V CMOS Sliding-Mode Control IC for Buck Converters

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***Abstract* – This paper presents a hysteretic (sliding mode) control IC for a buck DC/DC converter for use as an envelope tracking power supply to increase the efficiency of an RF power amplifier. The IC integrates a high-bandwidth error amplifier, a comparator with hysteresis, and a high-side driver for an external N-channel power MOSFET. The total control loop delay using the implemented IC is 35ns, this is shown to be a 30% reduction compared to a state-of-the-art discrete IC based solution. The presented results also show that it is viable to integrate a 100MHz operational amplifier on the same die as a high-voltage MOSFET driver operating with slew rates in excess of 5V/ns. The IC is demonstrated in a tracking power supply with 30W output power and 3µs rise/fall time, running from a 40V input. The complete IC, including pads, takes up 4mm^2 in a 0.35µm 50V CMOS process.**

I. INTRODUCTION

Switch-mode DC/DC power converters represent a highly useful and interesting class of electronic circuits. Controlling such systems can be a complex task in itself, which is reflected by the abundance of integrated switch-mode control circuits. However, for high-performance applications, such as envelope tracking power supplies [1] for RF power amplifiers, non-standard control schemes can provide advantages over the usual clocked PWM and current-mode schemes implemented with stock control ICs. One very useful alternative is hysteretic (sliding-mode) control with PID (Proportional-Integral-Derivative) voltage feedback [2], where the control system oscillates by itself. This can be shown [3] to lead to a superior loop gain since the control system is basically an oscillator, forcing (due to the well-known Barkhausen criteria for oscillation) the loop crossover frequency to be equal to the switching frequency. The performance of this class of control systems is directly influenced by the loop time delay, which is determined by the hysteretic comparator, the driver circuit and the power switches.

This paper presents an ASIC that addresses the need for minimum-delay hysteretic control of a buck DC/DC converter at appreciable power levels (10W+) and medium voltage levels (5-40V.) The DC/DC power switch components are kept external to allow the converter output power to be scaled as desired. In addition to enabling higher overall performance, an IC solution also offers a reduction of component count.

The considered ASIC application is shown in Figure 1. The shown hysteretic topology is known as a "GLIM" (Global Loop Integrating Modulator [2]), referring to the fact that the loop filter (output LC filter and PID compensator as a whole) is designed to exhibit an integrator-like frequency

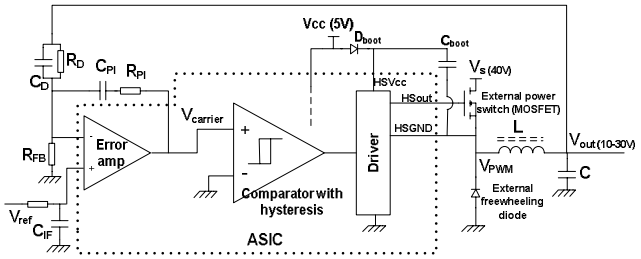

Figure 1. Considered ASIC application – a GLIM hysteretic self-oscillating switch-mode control system.

response. The PID compensator components are external for flexibility, but these could be easily integrated if desired [4]. The AMS 0.35µm 50V H35B4 CMOS process was chosen for the design due to the availability of small, fast, floating 5V MOSFETs for analog and digital signal processing as well as devices with 50V drain-source capability for high-voltage level shifting.

In comparison with prior art, which uses clocked control, a hysteretic control ASIC will be much more vulnerable to noise from the high currents and steep voltage transitions (dV/dt) from the gate driver, since the error ("carrier") signal is exclusively derived from signals outside the IC. Additionally, the need to create the triangular carrier signal from the small sinusoidal ripple on the DC/DC converter output voltage means that the error amplifier bandwidth has to be substantially higher than the switching frequency, further increasing the potential for switching noise pickup. Therefore, coupling of noise from the gate driver to the error amplifier and its input terminals has to be considered in this type of ASIC design. The increased difficulty in implementing a GLIM is, however, offset by its superior performance [3].

II. IMPORTANCE OF LOW DELAY

A hysteresis-mode self-oscillating control system with a triangular carrier signal (as resulting from having an integrator-like loop filter) will oscillate at the following frequency [5]:

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{hyst}}{K} + t_d}$$

where D is the steady-state duty cycle of the PWM signal, V_{hyst} is the hysteresis window, K is defined as twice the carrier dV/dt at $D=0.5$ and t_d is the total time delay in the oscillating loop. It is obvious that time delay limits the maximum switching frequency, limiting the application range of a given comparator and power stage

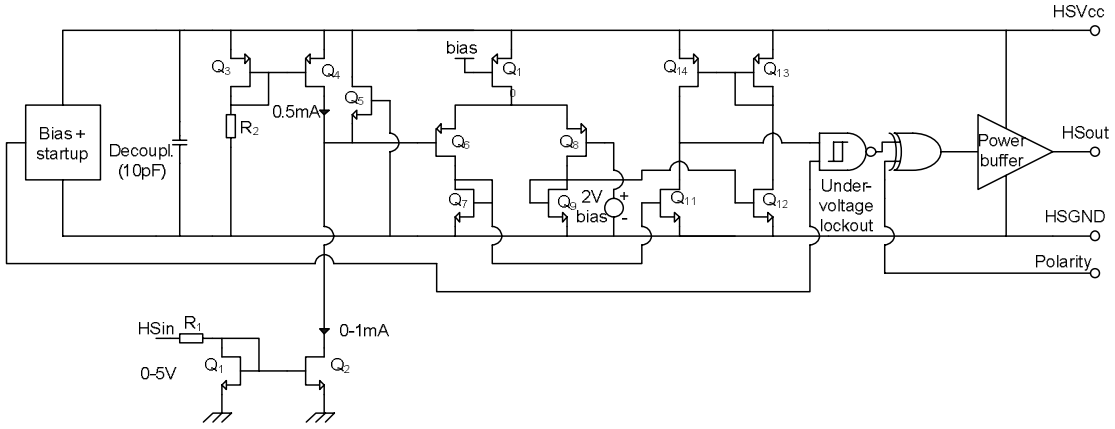

Figure 2. Implemented high-speed, high-side MOSFET driver

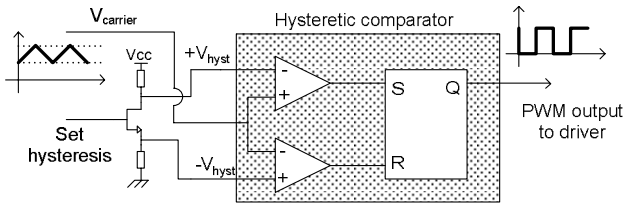

Figure 3. Comparator with voltage-controlled hysteresis.

implementation. By increasing the maximum switching frequency, higher RF tracking bandwidths are enabled.

For the best-case total delay of 50ns with a discrete design (see Table 1 in results section), this limits the switching frequency of a GLIM to 5MHz at *D=0.5*.

For low frequencies (significantly lower than the switching frequency), the loop gain of the GLIM loop with the shown implementation can be approximated as [3]:

$$G_{loop,GLIM,LF} \cong \frac{1}{1+s\frac{L}{R_{load}}+s^2LC}\cdot\frac{(1+sR_DC_D)\cdot(1+sR_{PI}C_{PI})}{sR_DC_{PI}}\cdot\frac{LC}{R_{PI}C_Dt_d}$$

where R_{load} is the load resistance seen by the converter. Note that the low-frequency loop gain of the GLIM loop is inversely proportional to the control loop time delay. Minimizing the loop time delay is therefore an effective way of further increasing the loop gain when the output filter and PID compensator have been optimized.

III. CIRCUITRY DESIGN

A 2-stage CMOS opamp was used for the error amplifier, with cascoding added to the input stage to increase the bandwidth to 100MHz. Additionally, a bipolar NPN device was used for the output buffer since this allows a greater positive output voltage swing. To maximize flexibility, the opamp was conservatively compensated to be unity-gain stable with 90º phase margin.

The hysteretic comparator is based on a comparator design using a differential pair with a slight positive feedback for speeding up transitions. Hysteresis was implemented by the use of 2 comparators and an SR latch (see Figure 3), which allows the hysteresis to be adjusted from 0 to Vcc via a single voltage input. Typically, a hysteresis of 50mV-500mV is appropriate for a GLIM design, as a trade-off between switching noise susceptibility and easily handled signal levels.

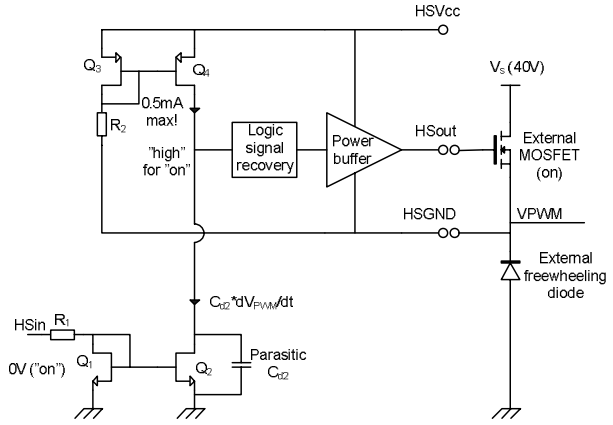

Figure 4. Parasitic negative feedback mechanism in implemented driver. If parasitic capacitance charge current exceeds 0.5mA, signaling will be disrupted.

The most difficult block in the ASIC design is the high-side (floating) MOSFET driver, since it has to handle voltages from 1-2V below ground (substrate) to 50V. In particular, the level shifting of the on/off signaling voltage from substrate level to the floating driver level has to be handled carefully. Many solutions are possible, including 2-way pulsed level shifting (used in many commercial drivers) and 4-way pulsed level shifting [6]. The implemented design (Figure 2) uses a simple 1-way continuously operating level shifter. The continuous signaling has the advantage over pulsed signaling that the requested driver state can never be ambiguous. This can be a problem when the requested state is stored in an SR latch, as is typically done with pulsed signaling.

A ground-level 0-1mA switchable current sink (R_1, Q_1, Q_2) along with a driver level 0.5mA current source (R_2, Q_3, Q_4) creates a +/-0.5mA current signal which is converted into a voltage at driver level by node capacitances. The 50V capability of the process is required for Q_2, since it has to handle the full HSVcc potential (4.3V to 44.3V) at its drain. Q_1 is also implemented as a high-voltage device for matching purposes. R_1/R_2 and Q_3/Q_4 are similarly matched to produce a symmetrical current signal.

The driver is polarized so that "on" is signaled with a 0mA current, hence there will be minimal voltage across Q_2 when it is conducting, thereby minimizing power dissipation. The disadvantage to this approach is that a negative feedback mechanism (see Figure 4) exists from the HSGND node to the level shift node voltage; when Q_2 turns

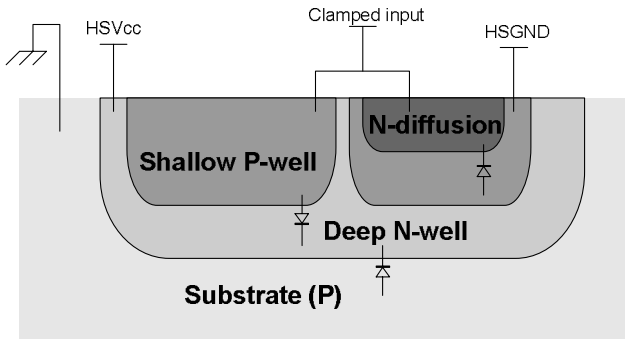

Figure 7. ESD clamp structure used for floating "Polarity" input.

off, the power MOSFET will eventually turn on, causing HSGND to rise towards V_s, pulling the current $I_{Cd,Q2}$ into the parasitic drain capacitance of Q_2, $C_{d,Q2}$:

$$I_{Cd,Q2} = C_{d,Q2} \cdot \frac{dV_{PWM}}{dt}$$

where $I_{D,Q4}$ is the drain current of Q_4. In this type of design, the dV/dt of the PWM signal must therefore be kept lower than:

$$\frac{dV_{PWM}}{dt} < \frac{0.5mA}{C_{d,Q2}}$$

Hence, in order to preserve signal integrity, the following must apply:

$$I_{Cd,Q2} < I_{D,Q4}$$

The use of an IC allows $C_{d,Q2}$ to be low enough to ensure that this potentially dangerous mechanism is kept inactive with the reasonably low $I_{D,Q4}$ of 0.5mA.

The level shifted voltage is sensed by a comparator (Q_6-Q_{14} in Figure 2) with a threshold level of ≈2V to ensure proper operation even when the driver ground (HSGND) is below the bulk substrate potential. Since all the devices in the floating part of the driver are implemented in a large, deep N-well (DNTUB) held at HSVcc (clamped to Vcc by the external bootstrap diode D_{boot}), this does not cause latch-up. Transistor Q_5 performs the role of clamping device, ensuring that the level shift node potential does not drop more than a MOS threshold voltage beneath HSGND, effectively safeguarding the 7V gate oxide of Q_4 and Q_6. Positive clamping is provided by the parasitic diode formed between the P-well used for Q_5 and the DNTUB.

The implemented driver cell also features invertible polarity to enable the use of an external buffer. This is because there can be an appreciable physical distance between the ASIC and the power MOSFET, so PCB trace inductance can cause problematic ringing in the MOSFET gate-source voltage. Polarity inversion is achieved using an XOR gate with one of the inputs routed to an external pin. ESD protection for this input (which of course has to float with the driver potential) was provided using the parasitic diodes formed between a DNTUB, a P-well and a shallow N-well in the P-well (see Figure 7.) Although this structure forms a parasitic NPN device, it has proven very useful as an ESD-only clamping device.

At layout level, the prototype IC design uses guard rings around each subcomponent. For the driver section, special care was taken to minimize substrate coupled noise from affecting the low-voltage components through the use of a guard ring and a top metal layer ground shield which is decoupled to a separate ground pin.

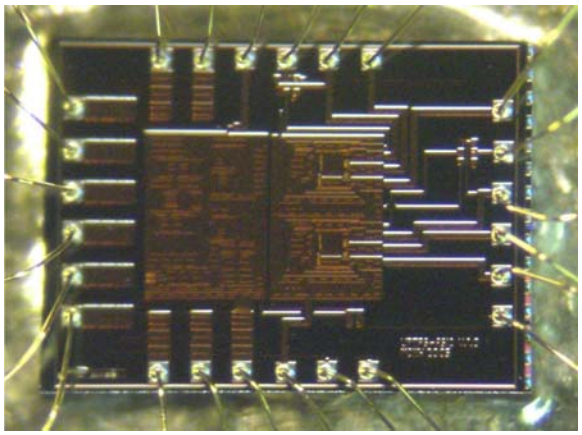

Figure 5. Die photo. Die size is 4mm^2. Top metal layer was used to screen low voltage section (left) from high-voltage section (right).

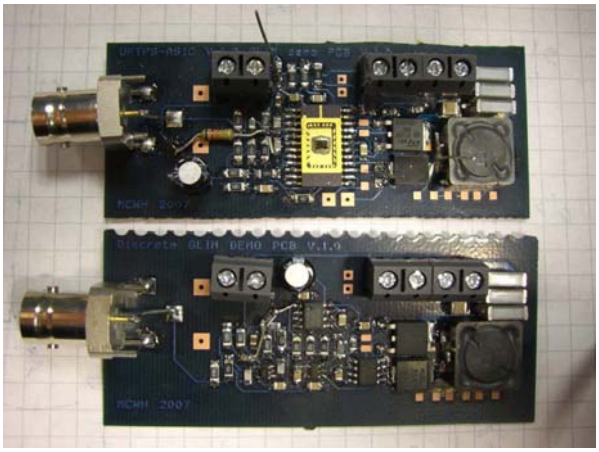

Figure 6. GLIM controlled buck converter prototypes using ASIC (top) and discrete circuitry (bottom.) ASIC replaces 4 discrete ICs.

IV. EXPERIMENTAL RESULTS

A photo of the prototype ASIC die is shown in Figure 5, while prototype DC/DC converters with ASIC and discrete controllers are shown in Figure 6. The use of a relatively small power MOSFET means that an external driver buffer is not necessary. The ASIC uses a quiescent current of around 10mA from a 5V supply, almost a 50% reduction compared to the 8mA from 12V of the discrete design. The difference in total control loop delay between the discrete and ASIC designs can be assessed from Figure 8. The delay is measured as the time is takes between the hysteresis threshold crossing of the error amplifier (EA) output and the 50% transition at the external power MOSFET gate. Note that the discrete MOSFET driver is specified to run off a 12V supply. The measurements show that the ASIC on average is about 15ns faster than the discrete design. The slightly lower slew-rate of the ASIC error amplifier (as reflected by the rise/fall times) is not a problem in the GLIM control application where its output is normally a triangle waveform. The ASIC exhibits a 25ns (or less) total propagation delay; subtracting the simulated 5ns of the

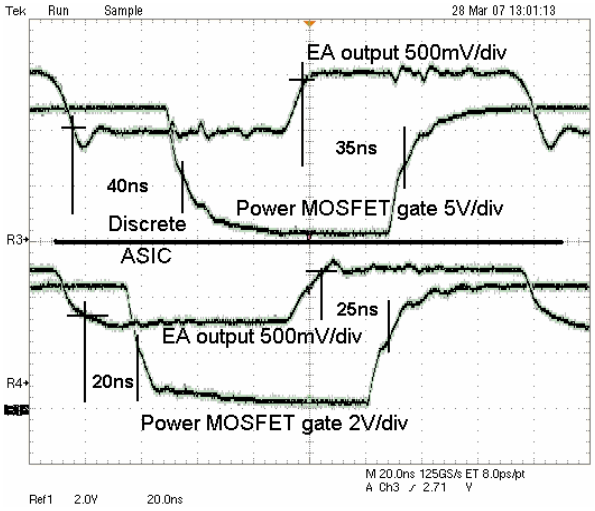

Figure 8. Measured total propagation delays in discrete (top) and ASIC (bottom) GLIM designs. ASIC is faster by approximately 15ns.

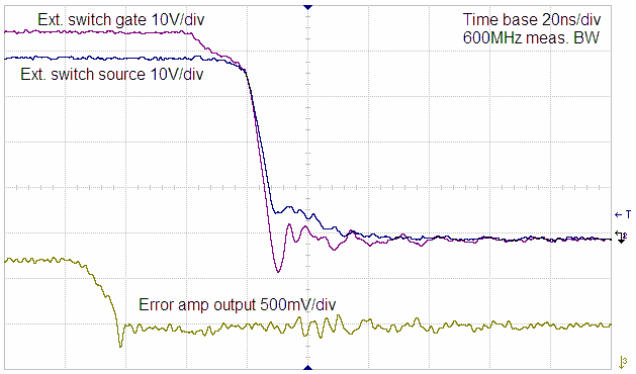

Figure 9. Measured waveforms during power switch turn-off. High dV/dt transition has negligible influence on error amplifier output.

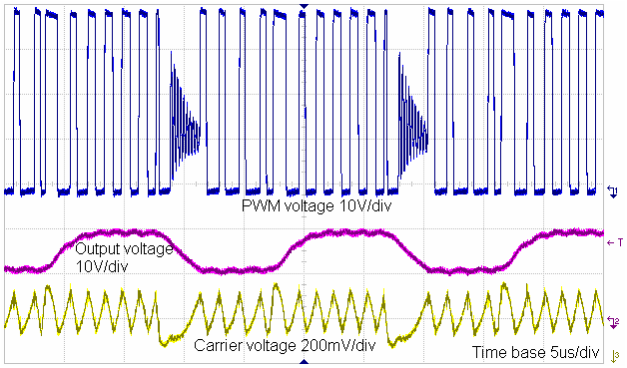

Figure 10. Measured waveforms in GLIM buck converter using ASIC. Control system oscillates as intended while providing the desired converter output voltage. Average output power ≈30W and output voltage rise/fall times are around 3µs.

hysteretic comparator, this suggests a driver propagation delay of about 20ns.

The issue of crosstalk to the error amplifier output can be examined from Figure 9. During a high-dV/dt (around 5V/ns), the error amplifier output ripples with a few tens of mV, which is not a problem in the GLIM configuration. Figure 10 confirms this, showing key waveform measurements with the ASIC controlled prototype converter stepping between 10V and 20V output. Notably, the ASIC operates correctly with -1V to 40V on the HSGND (connected to the PWM signal) terminal, and the carrier voltage is clean and almost triangular, as it should be. The high performance of the hysteretic control scheme is evident; the output voltage settles to a steady value in about 2-3 switching cycles, corresponding to around 3µs.

The delay budgets for the ASIC and discrete controller designs are compared in Table 1. Clearly, most of the advantage of the ASIC comes from the faster MOSFET driver. Since the presented ASIC is a first, conservatively designed prototype, further delay reductions should be possible, especially if the power switches are integrated on-chip, as has already been demonstrated for power levels as high as hundreds of watts [6], [7].

Table 1. Control loop delay budgets in GLIM designs

Contributor	Discrete design	ASIC based design
Comparator	*7.5ns (LMV7219)*	*5ns*
Driver circuit	*35ns (HIP2101)*	*20ns*
Power switch	*10ns*	*10ns*
Total	*≅50ns*	*≅35ns*

V. CONCLUSION

It has been experimentally demonstrated that the control and MOSFET driving circuitry for noise sensitive hysteretic control schemes can be implemented with very useful results on a monolithic IC. The driving factor for IC implementation of such control systems is two-fold; in addition to the natural component count and cost reduction, there is also a performance benefit to be reaped. This has been demonstrated by comparison of the implemented ASIC with a comparable discrete design based on some of the best components currently available. The implemented ASIC enables lower output impedance and faster switching and response times in envelope tracking power supplies through the reduced time delay in the control loop.

ACKNOWLEDGEMENT

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Accurate Sliding-Mode Control System Modeling for Buck Converters

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Keywords

Sliding mode control, modeling

Abstract

This paper shows that classical sliding mode theory fails to correctly predict the output impedance of the highly useful sliding mode PID compensated buck converter. The reason for this is identified as the assumption of the sliding variable being held at zero during sliding mode, effectively modeling the hysteretic comparator as an infinite gain. Correct prediction of output impedance is shown to be enabled by the use of a more elaborate, finite-gain model of the hysteretic comparator, which takes the effects of time delay and finite switching frequency into account. The demonstrated modeling approach also predicts the self-oscillating switching action of the sliding-mode control system correctly. Analytical findings are verified by simulation as well as experimentally in a 10-30V/3A buck converter.

Introduction

Sliding mode control (SMC) for DC/DC converters is a topic that has been covered in numerous publications during the last decade or so [1],[2],[3]. Originating from the control engineering field [4], sliding mode techniques are well described and many advanced implementations are possible. For most DC/DC applications, low controller complexity is desirable (to reduce cost and simplify design and implementation), and generally, simple control schemes such as PD [6] or PID voltage-mode [6],[7], are preferable. The sliding mode PID voltage controller is particularly useful, due to its high performance and simple implementation. To increase the applicability of the solution, proper modeling tools are needed so that the closed-loop control system performance can be predicted, analyzed and optimized. This paper starts out linking the PID compensator to a state-feedback system, resulting in an easy-to-use table of equivalent gain constants. Since s-domain analysis is used for parts of the paper, an equivalent s-domain model of the hysteretic comparator is derived based on the basic sliding mode theory. This is used to analyze the closed-loop output impedance of the buck converter, demonstrating a problem with the combination of PID feedback and conventional sliding mode theory. An improved state-space modeling approach is proposed, and experimental data supporting the proposed modeling approach is given at the end.
Two control systems are considered in this paper; Figure 1 shows a sliding mode controller using full state feedback, output current feed-forward, and output voltage error integration for eliminating steady-state errors. If implemented with actual current sensing (rather than estimation), this is a quite complicated way to implement a sliding mode controller for a buck converter. A similar but simpler solution is shown in Figure 2; this relies on a PID compensator for estimating the output and load currents as will be shown.

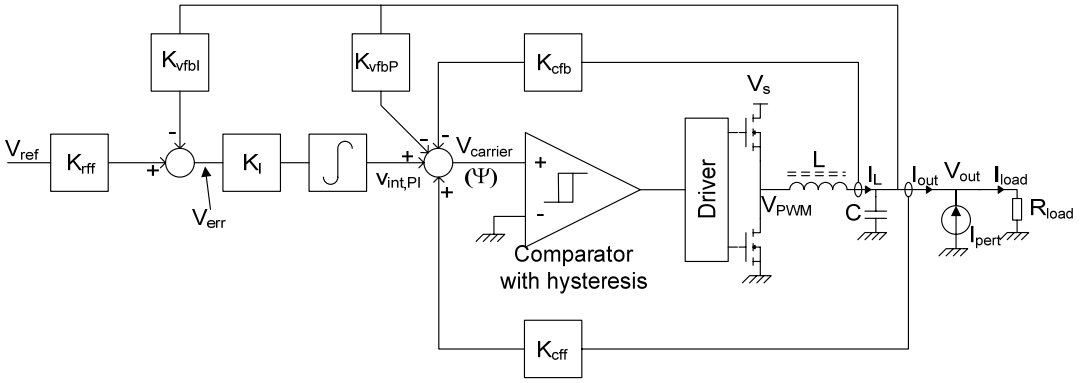

Figure 1 Generic sliding mode controller with output voltage error integration for a buck converter.

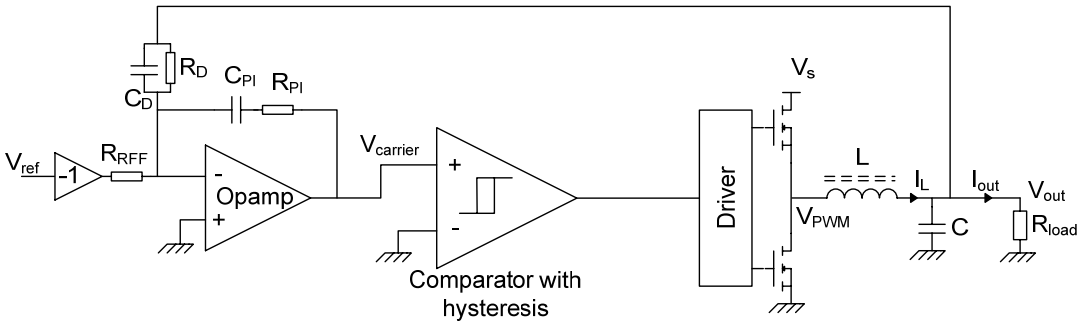

Figure 2 Easily implemented sliding mode PID controller for a buck converter [8].

PID controller equivalent model

To simplify analysis, the PID compensator is considered as cascaded PD and PI compensators. For the PD compensated buck converter output voltage, following relationship is found:

$$V_{out,PD}(s) = -V_{out}(s) \cdot \frac{R_D}{R_{PI}}\left(1 + sR_D C_D\right) + V_{ref}\frac{R_{rff}}{R_{PI}}$$

Using the basic description of a capacitor and Kirchhoff's current law leads to:

$$V_{out,PD} = -V_{out} \cdot \frac{R_{PI}}{R_D} - \frac{R_{PI}}{R_D}\frac{R_D C_D}{C} \cdot \left[I_L - I_{load} + I_{pert}\right] + V_{ref} \cdot \frac{R_{PI}}{R_{rff}}$$

This suggests that the PD compensated buck converter output voltage feedback system is functionally equivalent to a full state-feedback control system with ideal output current feed-forward compensation (as illustrated in Figure 3) – the output current is fed back with equal gain but opposite polarity compared to the inductor current. Using the constants given in Table 1, this can be rewritten to:

$$V_{out,PD} = -K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot \left(I_{load} - I_{pert}\right)$$

The PI part of the compensator introduces an extra state to the system, the output of the integrator part, $v_{int,PI}$ is chosen for this state. The relationship between input and output of the PI compensator is:

$$V_{carrier}(s) = V_{out,PD} \cdot \frac{1 + sR_{PI}C_{PI}}{sR_{PI}C_{PI}} = V_{out,PD}\left(1 + \frac{1}{s} \cdot \frac{1}{R_{PI}C_{PI}}\right)$$

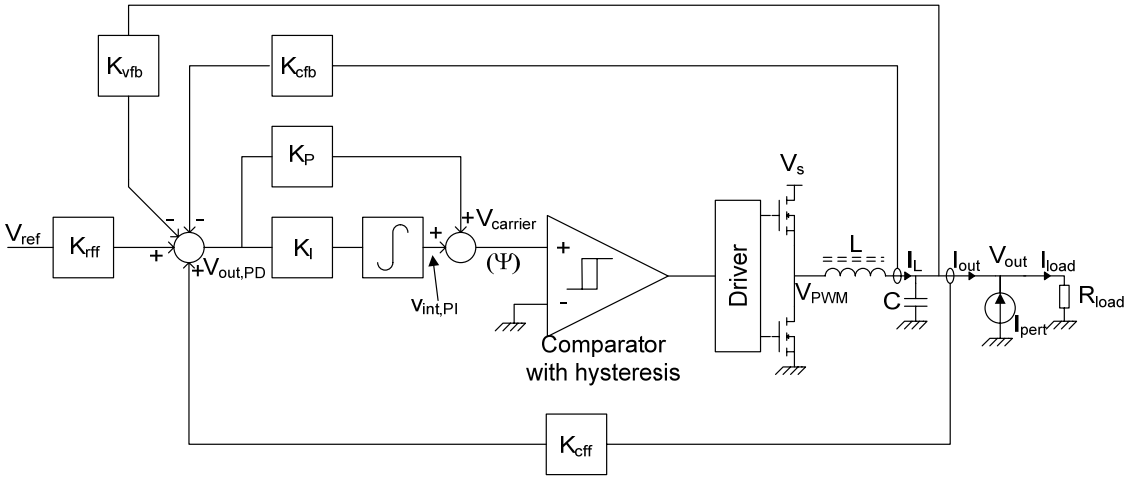

Figure 3 Derived model of a sliding mode PID voltage-mode control (SMC PID) system for a buck converter.

The integrator output is then given by:

$$v_{\text{int},PI} = V_{out,PD} \cdot \frac{1}{sR_{PI}C_{PI}}$$

This leads to the following state equation for $v_{int,PI}$:

$$\dot{v}_{\text{int},PI} = K_I \left[- K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot I_{out} + K_{rff} \cdot V_{ref} \right]$$

The found expressions for the constants in the PID controller equivalent model are listed in Table 1.

Table 1 Gains in PID controller equivalent model

Parameter		Expression
Output voltage feedback gain	K_{vfb}	$\frac{R_{PI}}{R_D}$
Inductor current feedback gain	K_{cfb}	$\frac{R_{PI}C_D}{C}$
Output current feed-forward gain	K_{cff}	$\frac{R_{PI}C_D}{C}$
Reference summation gain	K_{rff}	$\frac{R_{PI}}{R_{rff}}$
PI compensator proportional gain	K_P	1
PI compensator integral gain	K_I	$\frac{1}{R_{PI}C_{PI}}$

s-domain model of ideal sliding mode

One of the most fundamental assumptions made in classical sliding mode theory [4] is that the sliding variable (ψ, "carrier") is forced to zero by the control system switching/chattering action:

$$\psi = 0$$

In the buck converter, ψ is the input to the comparator/power stage block, which has the output V_{PWM}. When the control system is in sliding-mode, the average of V_{PWM} can assume any value in the range of:

$$\langle V_{PWM} \rangle_{T_{sw}} \in]0, V_s[$$

If the comparator/power stage is considered a gain block G_{HC}, the gain can be found using a simple describing function:

$$G_{HC} \equiv \frac{\partial \langle V_{PWM} \rangle_{T_{sw}}}{\partial \psi} = \infty$$

It is thus apparent that invoking the ideal sliding mode assumption in the buck converter is the same as assuming the comparator/power stage block to have an infinite gain [4]. However, this will be restricted to small signals since $\psi = 0$ is only guaranteed in sliding mode.

Sliding mode small-signal analysis

For the SMC PID buck converter operating in sliding mode, the following will apply:

$$\psi = 0 = v_{\text{int},PI} + K_P \left[-K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot I_{out} + K_{rff} \cdot V_{ref} \right]$$

The closed-loop output impedance of the converter can be found from this by expressing the dependency of V_{out} on I_{pert} [1]. Inserting $I_{out} = V_{out}/R_{load} - I_{pert}$, and Laplace transforming the resulting differential equation leads to:

$$0 = \frac{K_I}{s} \left[-K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot \left(\frac{V_{out}}{R_{load}} - I_{pert} \right) + K_{rff} \cdot V_{ref} \right] + K_P \left[-K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot \left(\frac{V_{out}}{R_{load}} - I_{pert} \right) + K_{rff} \cdot V_{ref} \right]$$

This equation only balances if:

$$-K_{vfb} \cdot V_{out} - K_{cfb} \cdot I_L + K_{cff} \cdot \left(\frac{V_{out}}{R_{load}} - I_{pert} \right) + K_{rff} \cdot V_{ref} = 0$$

I_L can be substituted by:

$$V_{out} = \frac{1}{sC} \left[I_L + I_{pert} - \frac{V_{out}}{R_{load}} \right] \Rightarrow I_L = sCV_{out} - I_{pert} + \frac{V_{out}}{R_{load}}$$

Additionally, since $K_{cfb}=K_{cff}$ in the PID:

$$\begin{aligned} &-K_{vfb} \cdot V_{out} - K_{cfb} \cdot (sCV_{out}) \\ &+ K_{rff} \cdot V_{ref} = 0 \end{aligned}$$

Thus, V_{out} only depends on the reference voltage V_{ref}:

$$\begin{aligned} &V_{out}(s) \left[-K_{vfb} - sCK_{cfb} \right] + V_{ref}(s) K_{rff} = 0 \\ &\frac{V_{out}(s)}{V_{ref}(s)} = \frac{K_{rff}}{K_{vfb} + sCK_{cfb}} = \frac{R_D}{R_{rff}} \cdot \frac{1}{1 + sR_D C_D} \end{aligned}$$

The reference-to-output transfer function found here is identical to the one derived using an infinite gain to model the hysteretic comparator [8], supporting the idea that assuming $\psi=0$ is equivalent to assuming $G_{HC}=\infty$. The output impedance is obviously predicted as:

$$Z_{out}(s) \equiv \frac{V_{out}(s)}{I_{pert}(s)} = 0$$

This is not exactly a good prediction since zero output impedance cannot be expected from any DC/DC converter.

s-domain output impedance analysis

To shed some light on the reason for the result found in the above, output impedance is calculated for an arbitrary hysteretic comparator small-signal gain, G_{HC}. The generic sliding mode controller is used for this calculation, since output current feed-forward is optional in this case as opposed to built-in, like in the PID.

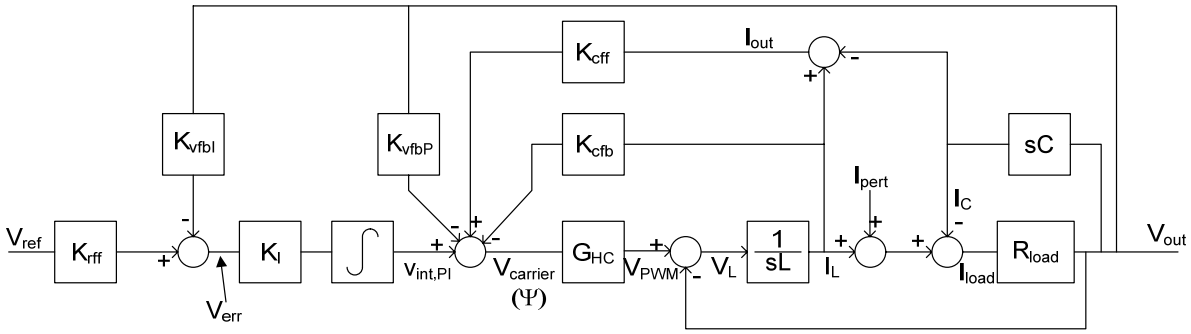

Figure 4 s-domain model of sliding-mode controlled buck converter (Figure 1) for analytical determination of output impedance.

Calculating the transfer function from perturbation current input to output voltage in the sliding-mode controlled buck converter leads to the following expression for the output impedance:

$$Z_{out,SMC}(s) \equiv \frac{V_{out}(s)}{I_{pert}(s)} = \frac{s^2 L + sG_{HC}\left(K_{cfb} - K_{cff}\right)}{s^3 LC + s^2\left(CG_{HC}\left(K_{cfb} - K_{cff}\right) + \frac{L}{R_{load}} + CG_{HC}K_{cff}\right) + s\left(\frac{G_{HC}\left(K_{cfb} - K_{cff}\right)}{R_{load}} + 1 + G_{HC}K_{vfbP}\right) + G_{HC}K_{vfbI}K_I}$$

The key point to observe here is the structural difference between the cases with no output current feed-forward ($K_{cff} = 0$) and with ideal output current feed-forward ($K_{cff} = K_{cfb}$):

$$Z_{out,SMC}(s)\big|_{K_{cff}=0} = \frac{\frac{s^2 L}{G_{HC}} + sK_{cfb}}{\frac{s^3 LC}{G_{HC}} + s^2\left(CK_{cfb} + \frac{L}{R_{load}G_{HC}}\right) + s\left(\frac{K_{cfb}}{R_{load}} + \frac{1}{G_{HC}} + K_{vfbP}\right) + K_{vfbI}K_I}$$

$$Z_{out.SMC}(s)\big|_{K_{cff}=K_{cfb}} = \frac{s^2 L}{s^3 LC + s^2\left(\frac{L}{R_{load}} + CG_{HC}K_{cff}\right) + s\left(1 + G_{HC}K_{vfbP}\right) + G_{HC}K_{vfbI}K}$$

In the case with ideal output current feed-forward, the low-frequency output impedance can be expressed simply as:

$$Z_{out.SMC}(s)\big|_{K_{cff}=K_{cfb},LF} \cong \frac{s^2 L}{G_{HC}K_{vfbI}K}$$

Thus, the output impedance at a given frequency is inversely proportional to the hysteretic comparator/power stage gain. Using an infinite gain to model the hysteretic comparator will therefore result in a very unrealistic prediction of the output impedance; 0 ohms at any frequency. Another way of looking at the problem is to consider the output impedances predicted with infinite hysteretic comparator gain:

$$\lim_{G_{HC}\to\infty} Z_{out,SMC}(s) = \frac{sK_{cfb}}{s^2C + s\left(\frac{K_{cfb}}{R_{load}} + K_{vfbP}\right) + K_{vfbI}K_I}$$

$$\lim_{\substack{G_{HC}\to\infty \\ K_{cff}=K_{cfb}}} Z_{out,SMC}(s) = 0$$

This also points towards the fact that infinite hysteretic comparator gain, as resulting from the assumption of $\psi = 0$, leads to unrealistic output impedance predictions with ideal output current feed-forward. Using the same techniques, this can also be shown to apply for the PID solution, leading to the result found above using classical sliding mode theory. Therefore, a more accurate description of the hysteretic comparator is needed when working with the highly useful hysteretic PID voltage-mode control solution.

Hysteretic comparator model

A more accurate hysteretic comparator small-signal model has recently been proposed [9], modeling the hysteretic comparator as a finite gain and a pole. This approach differs from prior art [10],[11] in that it uses separate describing functions at DC and the switching frequency, linking these together with a 1st order transfer function. With zero time delay, the model corresponds with the single-frequency describing function derived for analysis of oscillators based on hysteresis [12]. Note that to simplify the describing function analysis, the carrier signal was assumed to be piecewise linear.

Table 2 Parameters and expressions in new hysteretic comparator model [9]

Power stage supply voltage	V_s
2*[Carrier signal slope at $D= 0.5$]	$K_{carrier}$
Total control loop time delay	t_d
Hysteresis voltage (hysteresis window is +/-V_{hyst})	V_{hyst}
Duty cycle	D
Derived model pole	τ_p
Hysteretic loop switching frequency	f_{sw}

$$G_{HC}(s) \equiv \frac{V_{pwm}(s)}{V_{carrier}(s)} = \frac{V_s}{K_{carrier}\cdot t_d}\cdot\frac{1}{1+\tau_p s}$$

$$\tau_p = \frac{1}{2\pi f_{sw}}\sqrt{\frac{4}{\pi^2}\left(\frac{V_{hyst}+\frac{1}{2}K_{carrier}\cdot t_d}{\frac{1}{2}K_{carrier}\cdot t_d}\right)^2 - 1}$$

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{hyst}}{K_{carrier}} + t_d}$$

State-space buck converter model

Based on [13], the following basic model of the buck converter with synchronous rectification is used:

$$\begin{bmatrix}\dot{V}_{out}\\ \dot{I}_L\end{bmatrix} = \begin{bmatrix}-\frac{1}{CR_{load}} & \frac{1}{C}\\ -\frac{1}{L} & -\frac{R_s}{L}\end{bmatrix}\cdot\begin{bmatrix}V_{out}\\ I_L\end{bmatrix} + \begin{bmatrix}0 & \frac{1}{C}\\ \frac{V_s}{L} & 0\end{bmatrix}\cdot\begin{bmatrix}u\\ I_{pert}\end{bmatrix}$$

To allow subsequent output impedance analysis, a perturbation current input has been added, while inductor/switch series resistance has been included via R_s to get good accuracy on output impedance predictions. The PWM input to the system is modeled via u, which can assume average values in the range of 0 to 1. The simplicity of the model comes naturally since the dynamics of the buck converter with synchronous rectification can be considered independent of the state of the switching network.

State-space model of buck with sliding mode PID

The pole introduced by the hysteretic comparator model effectively adds an extra system state. Choosing the comparator output V_{PWM} (here defined as the average value of the PWM signal) as the new state, the state equation can be written as:

$$\dot{V}_{PWM} = \frac{V_s}{K_{carrier} \cdot t_d \cdot \tau_p} \cdot V_{carrier} - \frac{1}{\tau_p} \cdot V_{PWM}$$

Since $K_{carrier}$ is determined by the controller structure, which is fixed in the description shown, $K_{carrier}$ can be dissolved into a function of the existing constants. This is done as follows:

$$K_{carrier} \equiv 2 \cdot \dot{V}_{\substack{carrier \\ D=0.5}} = 2\left(\dot{v}_{\text{int},PI} + K_p\left[K_{vfb}\dot{V}_{out} + K_{cfb}\dot{I}_L - K_{cff}\dot{I}_{out}\right]\right)$$

Since $K_{cff} = K_{cfb}$ in the PID solution, this reduces to:

$$K_{carrier} = 2\left(\dot{v}_{\text{int},PI} + K_p\left[K_{vfb}\dot{V}_{out} + K_{cfb}\dot{I}_L\right]\right)$$

Remembering that $K_{carrier}$ is defined for $D=0.5$ and applying the small-ripple approximation, V_{out} is assumed to be a constant $0.5V_s$. If the output voltage is assumed constant, $\dot{V}_{out}$ is zero. Likewise, assuming the integral term in the PID compensator to be negligible, $\dot{v}_{\text{int},PI}$ can be approximated as zero. These approximations result in a very simple, but useful, expression:

$$K_{carrier} \cong 2K_P K_{cfb}\dot{I}_L = \frac{2K_P K_{cfb}}{L}\left(V_s - \frac{V_s}{2}\right) = \frac{K_P K_{cfb} V_s}{L}$$

After constructing and applying an appropriate feedback matrix, the closed-loop model of the SMC PID buck converter, incorporating the new hysteretic comparator model can be written as:

$$\begin{bmatrix} \dot{V}_{out} \\ \dot{I}_L \\ \dot{v}_{\text{int},PI} \\ \dot{V}_{PWM} \end{bmatrix} = \begin{bmatrix} -\frac{1}{CR_{load}} & \frac{1}{C} & 0 & 0 \\ -\frac{1}{L} & -\frac{R_s}{L} & 0 & \frac{1}{L} \\ -K_I K_{vfb} + \frac{K_I K_{cff}}{R_{load}} & -K_I K_{cfb} & 0 & 0 \\ -\frac{L}{K_{cfb} \cdot t_d \cdot \tau_p}\left[K_{vfb} - \frac{K_{cff}}{R_{load}}\right] & -\frac{L}{t_d \cdot \tau_p} & \frac{L}{K_P K_{cfb} \cdot t_d \cdot \tau_p} & -\frac{1}{\tau_p} \end{bmatrix} \cdot \begin{bmatrix} V_{out} \\ I_L \\ v_{\text{int},PI} \\ V_{PWM} \end{bmatrix} + \begin{bmatrix} \frac{1}{C} & 0 \\ 0 & 0 \\ -K_{cff}K_I & K_{rff}K_I \\ -\frac{L \cdot K_{cff}}{K_{cfb} \cdot t_d \cdot \tau_p} & \frac{L \cdot K_{rff}}{K_{cfb} \cdot t_d \cdot \tau_p} \end{bmatrix} \cdot \begin{bmatrix} I_{pert} \\ V_{ref} \end{bmatrix}$$

Note that V_s is absent from the equation. Thus, in spite of the departure from the ideal sliding-mode model ($\psi=0$), one of the chief advantages of sliding-mode control (invariance to plant proportional gain) is maintained. From another perspective, this also serves to validate the used small-signal model of the hysteretic comparator by complying with well-established theory.

Table 3 SMC PID buck prototype design parameters

Component	Parameter	Value in prototype	Remarks
Output inductor	L	$10\mu H$	
Output capacitance	C	$0.99\mu F$	3x330nF for low parasitic L
Inductor/switch series R	R_s	$100m\Omega$	
Total time delay	t_d	*60ns*	LMV7219+HIP2101
PID component	R_D	$10k\Omega$	
PID component	C_D	*180pF*	
PID component	R_{PI}	$1k\Omega$	
PID component	C_{PI}	*10nF*	
Ref. injection resistor	R_{RFF}	$1k\Omega$	

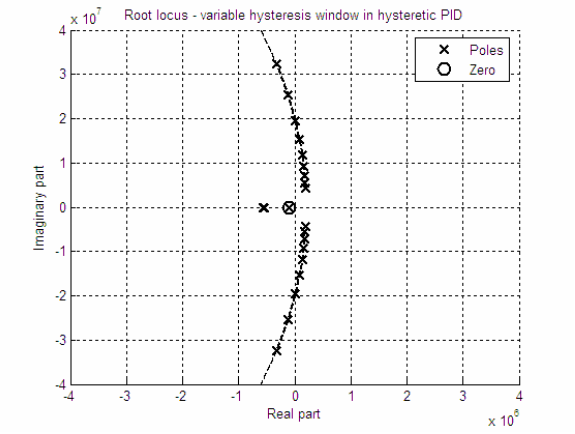

Figure 5 Prototype design pole-zero map with variable V_{hyst}. Dominant pole is fixed while switching frequency changes.

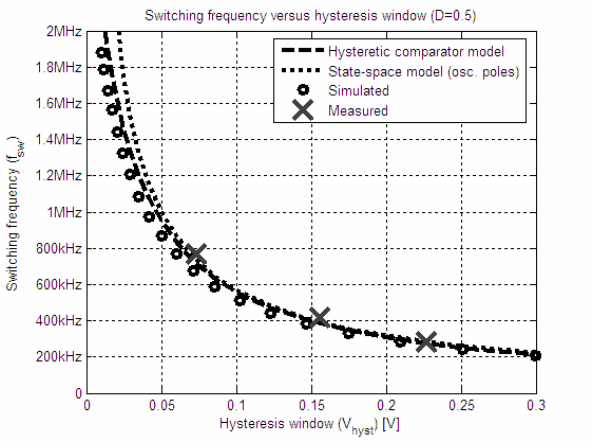

Figure 6 Modeled, simulated and measured f_{sw} for $D=0.5$ with variable V_{hyst} in prototype design.

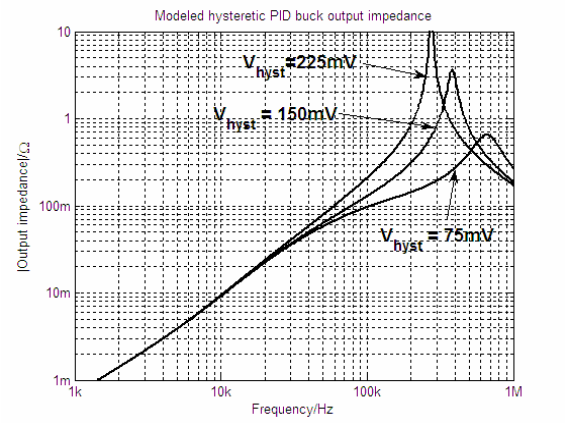

Figure 7 Modeled output impedances for prototype design.

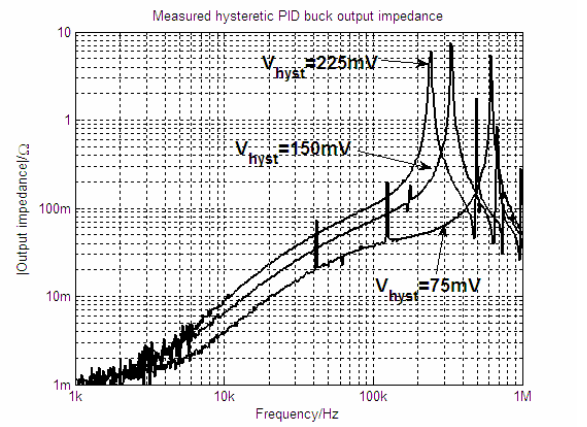

Figure 8 Measured output impedances for prototype design. V_{hyst} influences Z_{out} due to non-constant carrier slope (see below.)

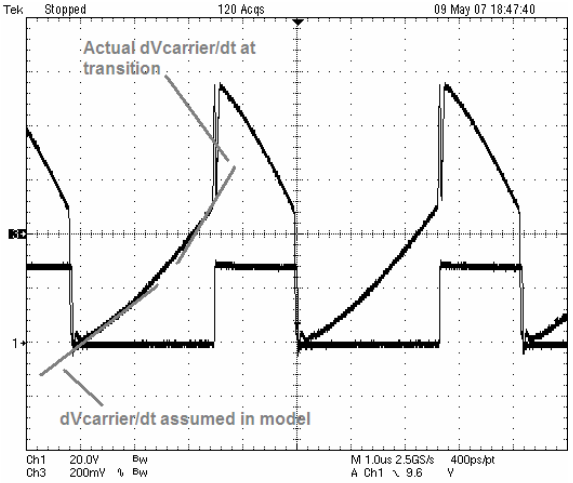

Figure 9 Measured comparator input (top) and PWM signal (bottom) for V_{hyst}=225mV. Carrier has non-constant slope; slope increases towards transition points, decreasing $G_{HC}(0)$.

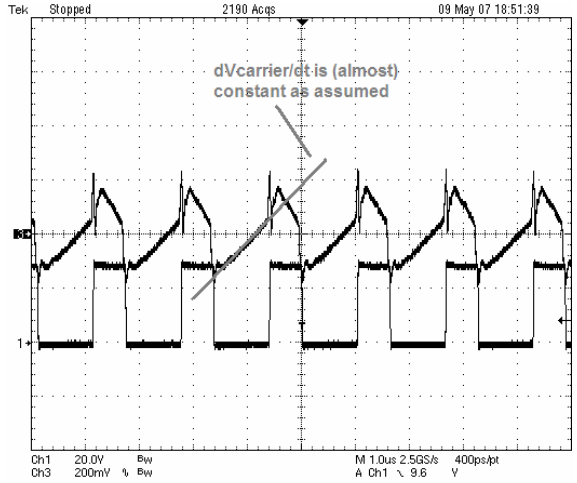

Figure 10 Measured comparator input (top) and PWM signal (bottom) for V_{hyst}=75mV. Linear-carrier assumption is more reasonable.

Modeled, simulated and experimental results

The SMC PID buck converter was implemented in a design with parameters as listed in Table 3. All measurements were performed with $V_s=30V$ and $R_{load}=5\Omega$. Hysteresis was implemented using positive

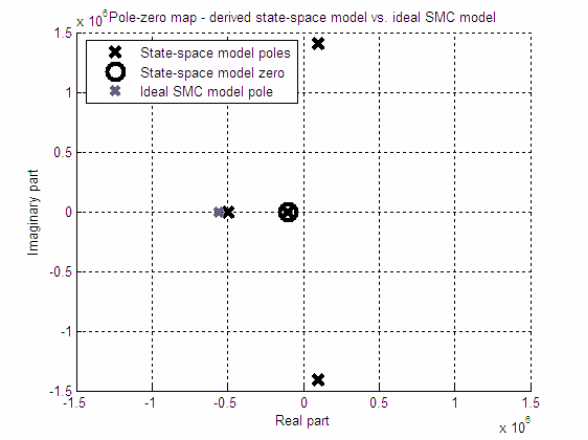

Figure 11 Pole-zero map of prototype design with V_{hyst}=150mV as found from state-space model; ideal SMC model pole is shown for comparison.

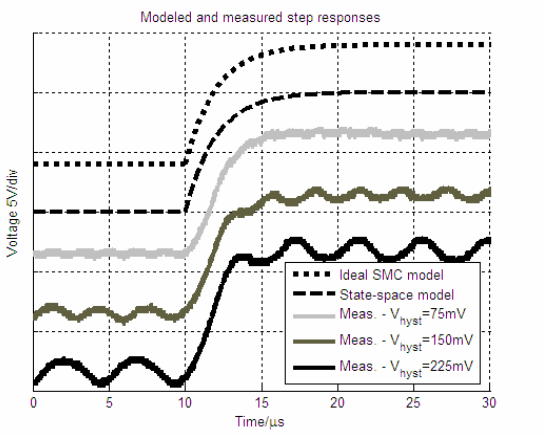

Figure 12 Modeled and measured step responses; models are very similar. Measured step responses show identical rise times as expected. Notice 2-cycle step-and-settle with V_{hyst}=225mV.

feedback around a comparator. The shown state-space model was typed into Matlab along with the shown τ_p expression. V_{ref}-to-V_{out} and I_{pert}-to-V_{out} transfer functions were extracted as needed. A switching Simulink model using the same input parameters provided simulated data. Fine stepping (2ns) was found necessary to minimize the effect of the single-step delays associated with certain Simulink blocks.

Initially, the effect of hysteresis in the closed-loop model poles was examined. Since the state-space model shown cannot accommodate time delays, t_d was set to 0. As can be seen from the model root-locus in Figure 5, the model has a set of almost purely imaginary poles as can be expected from what is basically an oscillator. The poles slide up and down the imaginary axis with varying V_{hyst} as could be expected. Note that the dominant pole in the model is largely unaffected by the variable hysteresis, which was also predicted by the ideal sliding-mode model.

When time delay is added, the poles move to the left half-plane, since the time delay is an essential part of the oscillation action. However, with time delay added, the high-frequency poles are still very representative of the switching frequency that can be expected from the system, as shown in Figure 6. With t_d set to its correct value (*60ns*), the switching frequency predicted by the hysteretic comparator model, the frequency of the high-frequency closed-loop poles and the simulated switching frequency match very well; the measurements shown also follow this trend.

The real value of the proposed approach is its ability to predict the effect of external disturbances in cases where classical sliding mode theory ($\psi=0$) suggests zero effect. The output impedance predicted by the derived model for the prototype design with three different hysteresis levels is shown in Figure 7. It is worth noting that the peaking at f_{sw} increases with V_{hyst}, reflecting that the influence of t_d decreases, hereby increasing the accuracy of the delay-free state-space model. Corresponding measurements made on the prototype are shown in Figure 8. There is a proportional displacement between the curves, unexpected from the modeled results. This deviation can be attributed to inaccuracy in the assumption of having a constant-sloping carrier signal, as made in the hysteretic comparator model derivation [9]. As can be seen from Figure 9 and Figure 10 (which show the triangular carrier signal with square-shaped positive feedback added), the carrier signal slope is reasonably constant with V_{hyst}=75mV, whereas it changes significantly with V_{hyst}=225mV. Since the slope at the threshold crossings increase with the hysteresis window, the duty cycle dependent DC offset to the carrier signal can be expected to increase, reducing the DC gain of the hysteretic comparator [9]. However, the output impedance prediction made with the presented state-space model is generally a lot better than what can be done with classical sliding mode theory. Peaking at f_{sw} is observed as expected, with the very high peaks reflecting the fact that the system is oscillating.

An easier mechanism to model is the closed-loop step response, even the infinite-gain hysteretic comparator model or classical sliding mode theory works in this case. The state-space model captures this correctly as well, as evident from Figure 12. There is a slight difference between the dominant pole frequency prediction made by the state-space model and ideal SMC theory as shown in Figure 11,

however, this is of little practical importance as shown in Figure 12. Also showcased in Figure 12 is the potentially very fast response of the SMC PID; with $V_{hyst}=225mV$, the output voltage steps and settles in about 2 switching cycles, as also demonstrated in [6].

Conclusion

It has been shown that classical SMC theory cannot be used for predicting the output impedance in buck converters when the feedback system incorporating ideal output current feed-forward. This class of feedback systems is important since it contains the PID voltage-mode hysteretic control scheme, which is simple to implement as well as effective. An improved modeling approach, incorporating a finite-gain, frequency dependent model of the hysteretic comparator has been devised instead, and demonstrated in the state-space theory domain. The new modeling approach allows accurate prediction of switching frequency, step response and output impedance, the latter being troublesome with the classical sliding mode theory. As an interesting bonus, the switching frequency of the control loop can be found just by inspecting the poles of the linear model. For practical purposes, the presented modeling approach is highly useful when designing DC/DC converters with low output capacitance (such as envelope tracking power supplies); in such cases the output impedance can only be lowered by maximizing control system effectiveness, which means that sliding-mode control is essential [14]. Some weak points of the proposed modeling approach have also been demonstrated; the non-constant slope of the carrier signal in a practical design limits the accuracy of the hysteretic comparator model used. Also, the absence of time delay in the state-space model limits accuracy of switching frequency predictions in designs where delay contributes significantly to oscillatory behavior. Still, this paper shows that the proposed modeling approach performs well for high-performance SMC PID buck designs.

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A Comparative Study of Analog Voltage-mode Control Methods for Ultra-Fast Tracking Power Supplies

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Abstract – **This paper presents a theoretical and experimental comparison of the standard PWM/PID voltage-mode control method for single-phase buck converters with two high-performance self-oscillating (a.k.a. sliding mode) control methods. The application considered is ultra-fast tracking power supplies (UFTPSs) for RF power amplifiers, where the switching converter needs to track a varying reference voltage precisely and quickly while maintaining low output impedance. The small-signal analyses performed on the different controllers show that the hysteretic-type controller can achieve the highest loop gain, leading to superior output impedance performance in the UFTPS application; this is explained using a recently proposed small-signal model for the hysteretic comparator. The analytical findings are verified experimentally as well as by simulation. Experimentally, the use of hysteretic self-oscillating control is shown to reduce the worst-case UFTPS output impedance by a factor of 10.**

I. INTRODUCTION

This work presented here is motivated by the requirement for effective control for a DC/DC power supply with fast reference voltage tracking capability, low output ripple voltage and high efficiency. Such a power supply (abbreviated UFTPS, Ultra-Fast Tracking Power Supply) is a crucial component in RF power amplification systems using envelope tracking for increasing the overall system efficiency [1], [2], [3], [4].

Most published work on UFTPSs [1], [2], [3], [4] uses clocked control solutions, but other viable UFTPS control solutions exist (as demonstrated in [5]) where advantage is taken of the seemingly superior performance obtainable by using self-oscillating control as also claimed in [6], for an audio power amplification application. Note that in the fields of control system engineering [7] and DC-DC power electronics [8], [9], the term "sliding mode" is used to characterize self-oscillating control systems, i.e. control systems that oscillate without an external clock signal. Most publications on sliding-mode control use a state-space representation of the power converter as the theoretical base – this level of mathematical complexity it not always necessary, as will be shown. The goal of the work presented here is thus to compare the standard fixed-frequency PWM voltage mode control solution with less-known self-oscillating control methods and present conclusions based on s-domain modeling of the control systems. The study performed emphasizes loop gain and output impedance since these turn out to be profoundly influenced by the choice of control topology. In the UFTPS application, output impedance is a relevant parameter to optimize, since the UFTPS will be required to maintain the desired output voltage in spite of load current variations.

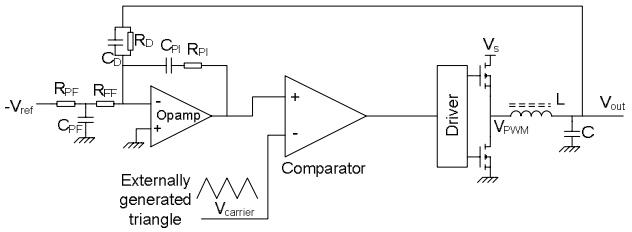

Figure 1 Buck UFTPS using standard clocked PWM/PID voltage-mode control scheme as implemented in this study.

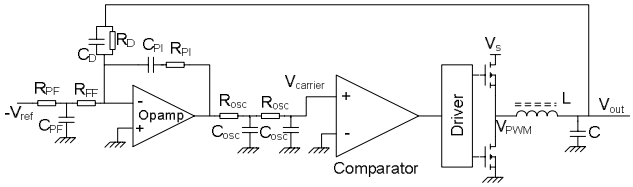

Figure 2 Buck UFTPS using phase-shift self-oscillating PID voltage-mode ("GCOM" [10]) control scheme as implemented in this study.

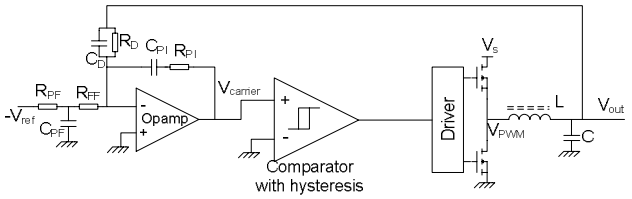

Figure 3 Buck UFTPS using hysteretic self-oscillating PID voltage-mode ("GLIM" [11]) control scheme as implemented in this study.

II. COMPARED CONTROL TECHNIQUES

Figures 1-3 show the compared control techniques as implemented. The basic point worth observing here is that PID compensation is provided in identical manner in all cases, whereas the mechanisms causing switching behavior are different.

A standard PWM/PID control solution is shown in Figure 1, while a phase-shift self-oscillating solution (described in [10] as a "Global-loop Controlled Oscillation Modulator"-GCOM) is shown in Figure 2. Finally, a similar hysteretic self-oscillating control solution (described in [6] and [11] as a "Global Loop Integrating Modulator" – GLIM) is shown in Figure 3.

Both of the self-oscillating techniques originate from the field of class-D audio power amplification, which is why they are not very well-known in the general power electronics field.

A major difference between the shown GLIM/GCOM control topologies and standard sliding mode controllers is that the error ("carrier") signal is generated from a single,

filtered/compensated system state (the output voltage), rather than a linear combination of system states [8], [9]. However, it can be easily shown that the PID compensated output voltage is equivalent to a PI-compensated linear combination of the output voltage and the inductor current, with ideal output current feed-forward compensation added. Starting with expressing the PID compensator output as a function of the converter output voltage leads to:

$$V_{\substack{out,PID \\ V_{ref}(s)=0}}(s) = V_{out}(s) \cdot \frac{(1+sR_DC_D)(1+sR_{PI}C_{PI})}{sR_DC_{PI}}$$

Appreciating that multiplication by s is equivalent to a differentiation and applying the I/V relation for a capacitor leads to:

$$s \cdot V_{out}(s) \equiv \frac{dV_{out}(s)}{dt} = \frac{1}{C} \cdot I_C(s) = \frac{1}{C}(I_L(s) - I_{out}(s))$$

And hereby:

$$V_{\substack{out,PID \\ V_{ref}(s)=0}}(s) = \frac{(1+sR_{PI}C_{PI})}{sR_DC_{PI}}\left[V_{out}(s) + \frac{R_DC_D}{C} \cdot I_L(s) - \frac{R_DC_D}{C} \cdot I_{out}(s)\right]$$

Thus, the GLIM control method is solidly linked to well-described sliding mode control techniques [9]. Its advantages are also clear; it has the dynamics of a full-state-feedback sliding-mode control system with error integration and ideal output current feed-forward while being very simple to implement.

III. DESIGNS FOR COMPARISON

The 3 different designs that are compared have been designed using identical power stages (switching devices and filter) and PID compensators. In all cases, the nominal switching frequency was set to 400kHz and a 23kHz output filter is used. The PID compensators were made identical as well, with both zeros placed at 10kHz. In the fixed-frequency PWM solution the crossover frequency was adjusted to ¼ of the switching frequency (very close to the maximum possible, 1/π [12]), while the oscillation poles and hysteresis window of the self-oscillating designs were used to set the nominal switching frequency.

The approach of using identical PID compensators was adopted to allow a clear comparison between the fundamental properties of the considered control topologies. This is the most fair option to the PWM solution since this (as will be demonstrated) has the lowest crossover frequency and additionally requires a significant phase margin to yield a satisfactory step response, as opposed to the self-oscillating designs.

For all the designs, the series combination of the LC output filter and PID compensator have the transfer function:

$$G_{ctrl}(s) \equiv \frac{V_{PID}(s)}{V_{PWM}(s)} = -\frac{1}{1+s\frac{L}{R_{load}}+s^2LC} \cdot \frac{(1+sR_DC_D)\cdot(1+sR_{PI}C_{PI})}{sR_DC_{PI}}$$

At high frequencies, this transfer function converges towards:

$$\lim_{s\to\infty} G_{ctrl}(s) = -\frac{R_{PI}C_D}{sLC}$$

This means that the compensated filter is basically an integrator at high frequencies (such as the switching frequency), providing a -270° phase shift when including the -180° shift resulting from negative feedback. In the GCOM controller, oscillation will occur when:

$$\angle \frac{V_{carrier}(s)}{V_{PWM}(s)} = 0$$

This should come as no surprise; all oscillators oscillate at the point where the open loop phase ensures positive feedback. The fact that the loop gain magnitude has to be 0dB at the oscillation frequency (one of the well-known Barkhausen criteria for oscillation) provides an opportunity for indirectly estimating the comparator small-signal gain. The remaining -90° phase shift needed for oscillation (ignoring comparator/power stage delay) is supplied by the phase-shift network, which has the transfer function:

$$G_{osc}(s) \equiv \frac{V_{carrier,GCOM}(s)}{V_{PID}(s)} = \frac{1}{1+s\cdot 3R_{osc}C_{osc}+s^2R_{osc}^2C_{osc}^2}$$

This will produce a -90° phase shift at a frequency of

$$f_{osc,GCOM} \cong \frac{1}{2\pi} \cdot \frac{1}{R_{osc}C_{osc}}$$

This is thus an approximate expression for the switching frequency of the shown GCOM implementation.

Note that this cannot account for observed duty cycle dependency of the switching frequency – an issue that is still open for exploration in the frequency domain.

For a hysteretic-type controller with an integrator as loop filter, the following applies [14]:

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{hyst}}{K}+t_d}$$

K is defined as:

$$K \equiv 2\frac{dV_{carrier}}{dt}_{D=0.5}$$

This can be used for the GLIM since $G_{ctrl}(s)$ converges towards integrator behavior. In steady state, with $D=0.5$, K can be approximated as:

$$K_{GLIM} \cong V_s \cdot step(G_{ctrl}(s))$$

Here, *step* refers to the unit step response. This leads to:

$$K_{GLIM} \cong \frac{V_sR_{PI}C_D}{LC}$$

Thus, the switching frequency of the considered GLIM UFTPS implementation can be approximated as:

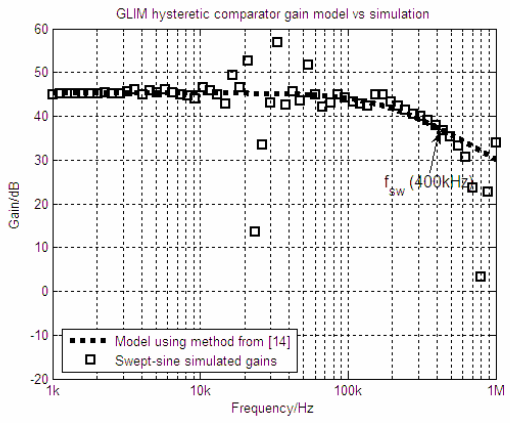

Figure 4 Modeled vs. simulated gain of hysteretic comparator. The used model is accurate from DC to f_{sw}. Deviations around 20-50kHz is due to poor simulation SNR around output filter resonance.

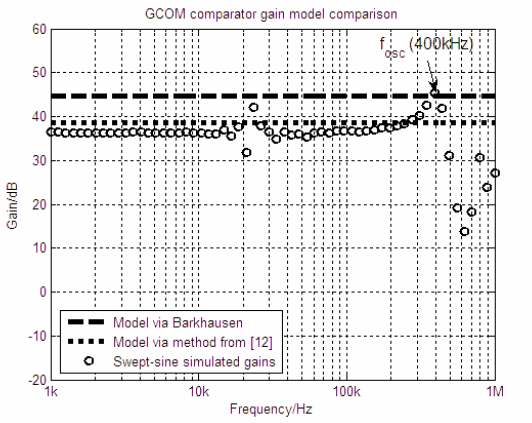

Figure 5 Comparison of models for the gain of the GCOM comparator with swept-sine simulation. A more precise model would have to obey both Barkhausen and the general-purpose comparator model from [12].

$$f_{sw,GLIM} \cong \frac{D(1-D)}{2\frac{V_{hyst}}{V_s}\cdot\frac{LC}{R_{PI}C_D}+t_d}$$

This can then be used to select the hysteresis window for obtaining a given nominal switching frequency.

IV. SMALL-SIGNAL ANALYSIS

Since all the examined solutions share identical supply voltages, output filters and PID compensators, only the blocks between the PID output and driver input are different.

In the case of the fixed-frequency PWM solution, it is well-known [13] that the comparator can be simply modeled as a constant gain.

Based on a recently published model [14], the hysteretic comparator is modeled as a single-pole system where the total control loop time delay t_d is the key quantity limiting the DC small-signal gain:

$$G_{HC}(s) \equiv \frac{V_{PWM}(s)}{V_{carrier}(s)} = \frac{V_s}{K\cdot t_d}\cdot\frac{1}{\tau_p s+1}$$

Where V_s is the power stage supply voltage and τ_p is a derived time constant. The accuracy of this modeling approach can be assessed from Figure 4.

The overall loop gain of the GLIM controlled buck converter, neglecting the parasitic power stage/output inductor series resistance R_s, is found to be:

$$G_{loop,GLIM} = G_{ctrl}\cdot\frac{2V_s}{K_{GLIM}\cdot t_d}\cdot\frac{1}{\tau_p s+1} \cong G_{ctrl}\cdot\frac{LC}{R_{PI}C_D t_d}\cdot\frac{1}{\tau_p s+1}$$

Thus it is apparent that the hysteretic comparator DC small-signal gain is un-affected by the supply voltage; for a given filter/controller design it can only be increased by reducing the time delay – perhaps surprisingly, hysteresis plays no part in determining the DC gain.

If the compensator zeros and output filter poles are assumed to cancel, it is evident that the GLIM loop gain has a 40dB/decade slope at high frequencies – over a range determined by the control loop time delay (since t_d heavily influences τ_p.) This potentially leads to superior loop gain for the GLIM control solution – as evident in this study.

In the GCOM implementation, assuming a flat comparator small-signal gain G_C, the loop gain will be given by:

$$G_{loop,GCOM}(s) = G_{ctrl}(s)\cdot G_{osc}(s)\cdot G_C$$

A general method for finding the gain of any comparator in a switch-mode control loop is given in [12]:

$$G_C = \frac{4V_s f_{osc}}{\dot{c}_0}$$

Where $\dot{c}_0$ is the slope of the carrier signal at the zero crossing. This model can be shown [12] to correspond with the standard comparator model in [13]. In the shown GCOM implementation, the carrier signal is almost-sinusoidal (due to shaping by the loop filter), this means that the steady-state carrier signal can be described as:

$$V_{carrier,GCOM}(t) \cong \frac{4}{\pi}V_s\cdot\left|G_{ctrl}(j2\pi f_{osc})\cdot G_{osc}(j2\pi f_{osc})\right|\cdot\sin(2\pi f_{osc}t)$$

This allows the carrier slope to be found:

$$\frac{dV_{carrier,GCOM}}{dt} \cong 8V_s f_{osc}\cdot\left|G_{ctrl}(j2\pi f_{osc})\cdot G_{osc}(j2\pi f_{osc})\right|\cdot\cos(2\pi f_{osc}t)$$

Since the carrier and PWM signal are in phase at f_{OSC}, the carrier slope at the zero crossing can be approximated as:

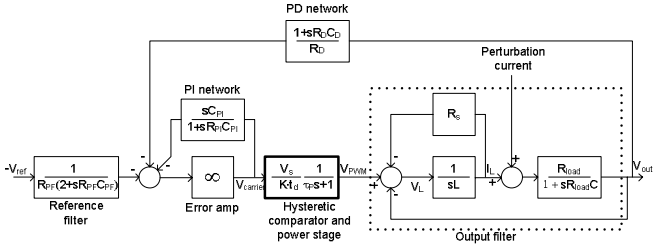

Figure 6 Complete small-signal model of the GLIM controlled UFTPS for predicting loop gain and output impedance.

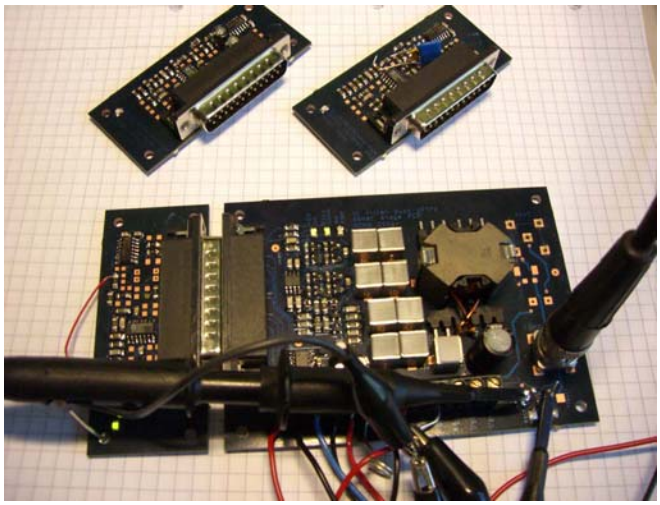

Figure 7 Prototype hardware; the 3 different controllers were implemented on individual PCBs, sharing a common power stage PCB.

$$\dot{c}_0 \cong 8V_s f_{osc} \cdot \left|G_{ctrl}(j2\pi f_{osc}) \cdot G_{osc}(j2\pi f_{osc})\right|$$

This leads to the comparator gain:

$$G_C \cong \frac{1}{2\left|G_{ctrl}(j2\pi f_{osc}) \cdot G_{osc}(j2\pi f_{osc})\right|}$$

This suggests a loop gain magnitude of -6dB at the switching frequency, as stated in [12]. However, applying Barkhausen's criterion of 0dB loop gain at f_{osc} leads to:

$$G_C \cong \frac{1}{\left|G_{ctrl}(j2\pi f_{osc}) \cdot G_{osc}(j2\pi f_{osc})\right|}$$

Obviously, there is a severe disagreement between the two approaches. It is beyond the scope of this paper to sort out this disagreement, but simulated and experimental results indicate that both models are correct in a limited frequency span; the GCOM comparator seems to have a gain that varies with frequency, just like the hysteretic comparator in a GLIM.

In this paper, the lower of the two comparator gain estimates is used for the GCOM model, since this appears to be the best approximation at low frequencies (see Figure 5.) Experimentally, the comparator behaves as shown in Figure 9 – although not spot-on, the measurements support the variable-gain theory.

Due to the approximate nature of the already derived switching frequency expression, an accurate expression for G_C cannot be obtained by insertion of f_{osc}. The loop gain can still be found by empirically measuring the switching frequency f_{sw} of the loop and evaluating the expression:

$$G_{loop,GCOM}(s) = G_{ctrl}(s) \cdot G_{osc}(s) \cdot \frac{1}{2\left|G_{ctrl}(j2\pi f_{osc}) \cdot G_{osc}(j2\pi f_{osc})\right|}$$

This was the approach adopted for the modeled GCOM loop results shown in this paper.

For all the considered implementations, closed-loop output impedance will be given by:

Figure 8 Measured loop gain and associated phase characteristics (1kHz-1MHz) of a "GLIM" controlled UFTPS prototype. Phase margin is non-existent, reflecting the fact that the loop oscillates (switches) naturally at the crossover frequency of 400kHz.

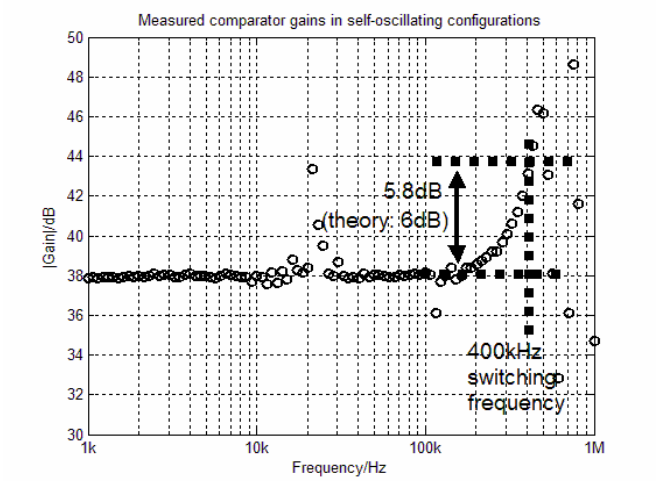

Figure 9 Measured GCOM comparator gain. A 6dB rise in magnitude response near oscillation frequency observed as expected.

$$Z_{out}(s) = R_s \frac{1 + s\frac{L}{R_s}}{1 + s\frac{L}{R_s} + s^2 LC} \cdot \frac{1}{1 + G_{loop}(s)}$$

Here, R_s models series resistance in power MOSFETs and the output inductor, this was found important for correctly predicting the LF output impedance.

Likewise, this was the expression that provided data for output impedance model results.

Summing up, the self-oscillating control schemes can be expected to have superior loop gain since:

- The crossover frequency is equal to the switching frequency as a fundamental part of oscillatory behavior
- Loop gain is allowed to (has to) have a higher slope at high frequencies than in the PWM/PID since the loop has to oscillate

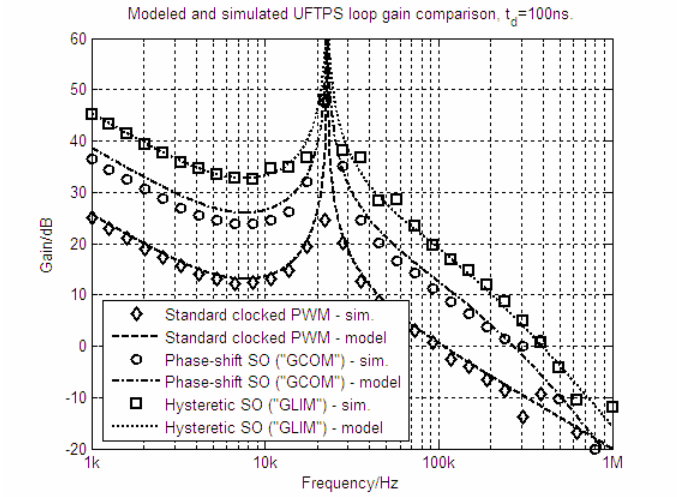

Figure 10 Calculated and simulated loop gains of the 3 designs. The hysteretic-type design provides almost 20dBs of extra loop gain below 100kHz when compared to the fixed-frequency PWM design. Modeled and simulated loop gains correspond well.

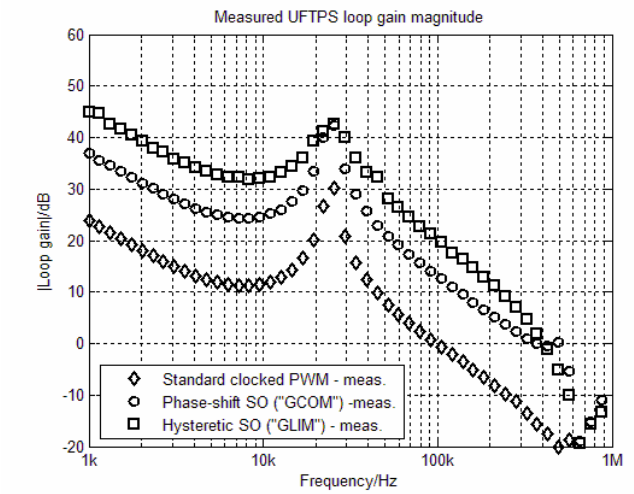

Figure 11 Measured loop gain (data was imported into Matlab) for of the 3 prototype designs. Correspondence is very good with simulated and modeled results. Self-oscillating solutions clearly outperform the clocked PWM.

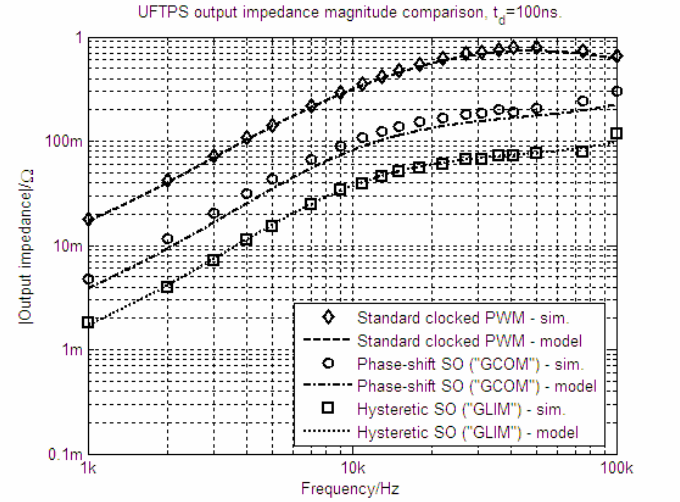

Figure 12 Calculated and simulated output impedance magnitude of the 3 designs. The high loop gain of the hysteretic design improves UFTPS output impedance by an order of magnitude in comparison with the fixed-frequency PWM solution.

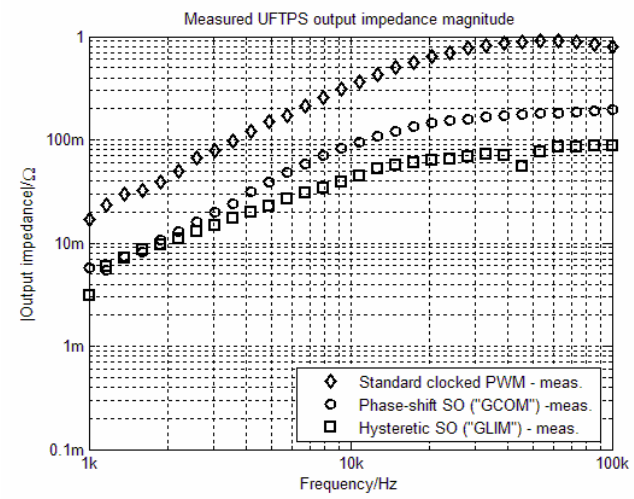

Figure 13 Measured output impedance magnitude of the 3 prototype designs. The GLIM control topology reduces worst-case output impedance by 20dB when compared to the fixed-frequency PWM solution. DC parasitics cause LF convergence of output impedances.

V. EXPERIMENTAL RESULTS

Analytical results presented here are based on the derived small-signal models of the controllers. The different control solutions were modeled in Simulink, and Matlab was used to control the

multiple simulations required (one per frequency point per model) to obtain accurate swept-sine results. The resulting software setup works a lot like a gain-phase analyzer and is a quite "bullet proof" way of simulating the control system performance if a system model is uncertain or unavailable. Variable perturbation levels were used to avoid injection locking of the switching frequency to the perturbation frequency. A $10V_{peak}$ perturbation level was used at 1kHz, decreasing logarithmically towards $1mV_{peak}$ at 1MHz for the loop gain simulations, the range was 1.77V decreasing to 1.25mV for the corresponding measurements. All simulations and measurements were performed with a quiescent operating duty cycle of *D=50%*.

An AP Instruments Model 200 impedance/gain-phase analyzer provided the corresponding experimental data (except for the HP4194A screen shot in Figure 8.)

Analytical and simulated UFTPS loop gain and output impedance characteristics are compared in Figure 10 and Figure 12, agreement is generally very good. The high performance of the self-oscillating controllers is a direct result of their self-oscillating nature as explained earlier.

Corresponding measurements are shown in Figure 11 and Figure 13, the only deviations from models/simulations are the higher damping of the filter resonance and the convergence of GLIM and GCOM output impedances at low frequencies, probably due to parasitic resistance outside the feedback loop.

The extra-high performance of the hysteresis-based solution can be attributed to the small-signal characteristics of the hysteretic comparator; its gain at high frequencies slopes at 20dB/decade, lifting the LF loop gain correspondingly. The found performance advantage of the hysteretic solution corresponds well with conclusions in prior art [6], [15], [16].

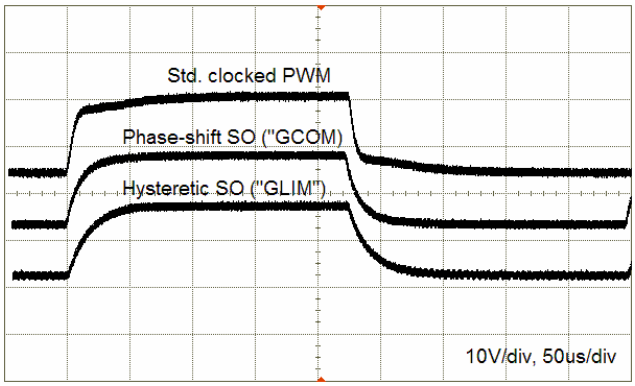

Figure 14 Measured step responses of the three designs. Supply voltage and output filter cut-off are the dominant factors limiting rise/fall times.

The increase in loop gain obtained via hysteresis-based control can be used practically in a number of ways; either as a means for producing a more "stiff" output voltage with a given filter, or simply for increasing the filter design options when designing for a given output impedance. In any case, the ten-fold low-frequency loop gain increase is very useful and comes practically for free – the power stage components are significantly more expensive than the control system components. Note however, that in the UFTPS designs considered, the output voltage slew rate will be largely un-affected by the higher loop gain and crossover frequency – filter, load and input voltage determine the large-signal response if the control system is fast enough, as is demonstrated in Figure 14. The difference between the self-oscillating and clocked designs can probably be explained by the difference in crossover frequency.

The GCOM solution could presumably be improved by increasing the split between the oscillation poles in order to provide a steeper loop gain slope below the oscillation frequency. This corner of the solution space is, however, still relatively unexplored territory.

The major drawback inherent to simple self-oscillating control solutions, variable switching frequency, is of course still a potential cause of concern. This can be at least partially amended by the use of feedback based switching frequency control [5].

Note that the final 2-3dBs of precision of the GLIM model were obtained by numerical computation of K_{GLIM}, taking the not perfectly straight slope of the carrier into consideration.

Corrections also had to be made for the simulation time step (10ns), which effectively added a 10ns delay to the loop for every simulation loop element with "memory" (such as transfer functions) when calculating the corresponding model transfer function.

VI. CONCLUSION

An emerging power electronics application that places extreme demands on power converter control effectiveness has been presented along with 3 perhaps seemingly similar control solutions. However, it is shown theoretically and experimentally that the use of self-oscillating instead of clocked control allows the power electronics designer to obtain extra performance from the UFTPS power components. In particular, the use of hysteretic-type rather than standard fixed-frequency PWM control has been demonstrated to provide a significant reduction (20dB) of worst-case output impedance for a given choice of switching frequency and power components. The reason for the superior performance of self-oscillating controllers has also been clearly demonstrated in the frequency domain; the loop crossover frequency is exactly equal to the switching frequency. Finally, the problem of modeling the comparator in a phase-shift oscillating controller such as the GCOM has been discussed. For the UFTPS application this problem is not a major obstacle; the hysteretic-type control schemes can perform better and good models are available.

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Ultrafast Tracking Power Supply With Fourth-Order Output Filter and Fixed-Frequency Hysteretic Control

Mikkel C. W. Høyerby and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—A practical solution is presented for the design of a non-isolated dc/dc power converter with very low output ripple voltage and very fast output voltage step response. The converter is intended for use as an envelope tracking power supply for a radio frequency power amplifier (RFPA) in a TETRA enhanced data service (TEDS) base station. A simple and effective fixed-frequency hysteretic control scheme for the converter (buck with fourth-order output filter) is developed and analyzed. The proposed approach is verified experimentally by a 500 W output prototype, capable of delivering any voltage in the range of 10–30 V within 10 μs with 10 mVpp of output ripple and efficiencies in the 88%–95% range.**

***Index Terms*—Comparator modeling, envelope tracking, fourth-order filter, high-bandwidth, hysteretic control, self-oscillating.**

I. Introduction

THE USE of envelope tracking power supplies for radio frequency power amplifiers (RFPAs) is an emerging application for high-bandwidth power converters. By adjusting the RFPA supply voltage in accordance with the RFPA output voltage envelope, substantial efficiency improvements are possible with a linear (class A or AB) RFPA. The variable supply voltage can be utilized in different schemes; in the most aggressive scheme [envelope elimination and restoration (EER)], the instantaneous RFPA output level is directly governed by the supply voltage provided, since amplitude information is removed from the RFPA input. In this scheme, it is of utmost importance that the supply voltage is generated quickly and precisely enough, so the power supply control bandwidth has to be significantly faster than the RF modulation bandwidth [1], [2].

A less aggressive solution is envelope following [2], where the RFPA input is the full amplitude/phase modulated signal, and the RFPA is powered with a supply voltage that tracks the instantaneous RFPA output envelope [3]–[5].

The solution considered in this paper is to simply supply a voltage to the RFPA that is high enough at any given time to avoid excessive compression/clipping, This scheme is generally known as envelope tracking [2] and is illustrated in Fig. 1. In this scheme, the power supply can principally be as slow as desired, provided that sufficient look-ahead is implemented in the preceding modulator/envelope detector to let the supply voltage ramp up to the necessary level. In this case, the power supply response speed specification can be relaxed, albeit at the cost of reduced RFPA efficiency.

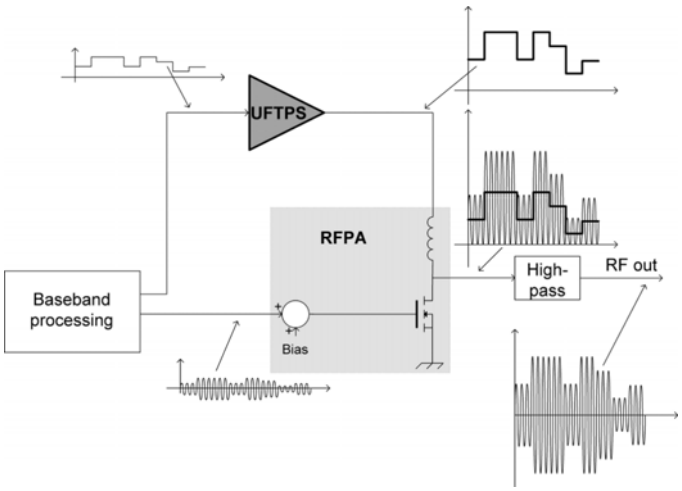

Fig. 1. RFPA system with envelope tracking UFTPS and idealized waveforms.

This paper discusses the implementation and optimization of a power converter (in this work named UFTPS, ultrafast tracking power supply) capable of producing the variable supply voltage for the RFPA in a TETRA enhanced data service (TEDS) base station. Compared to prior art, this can be classified as a high-power, low-bandwidth application.

II. System Specifications

The 50-kHz quadrature amplitude modulation (QAM) [6] transmission mode in the TEDS standard is considered here, although several other modes exist. The QAM modulated signal presented to the RFPA has a high peak-to-average ratio—11.5 dB (x3.586) as indicated in the amplitude distribution shown in Fig. 2. In order to achieve a high efficiency improvement, 50 kHz of large-signal control bandwidth is targeted for the tracking power supply. The RFPA supply voltage may swing between 10 and 30 VDC, with the supply current ranging from 1 to 18 A. The RFPA is assumed to present a load comprising a resistance of greater than 2.6 Ω in parallel with a current sink to the UFTPS.

Simple spectral measurements using an early UFTPS prototype have been performed on a representative RFPA in order to determine the conversion ratio of ripple into sideband products [1], [3], [7]. It was found that 100 mVpp [7] of ripple causes side band products of -65 dBc at offsets corresponding to the switching frequency. This indicates that approximately 5 mVpp of ripple will be required to meet the -90 dBc sideband product limit in the 1-MHz region specified by the Tetra (and drafts

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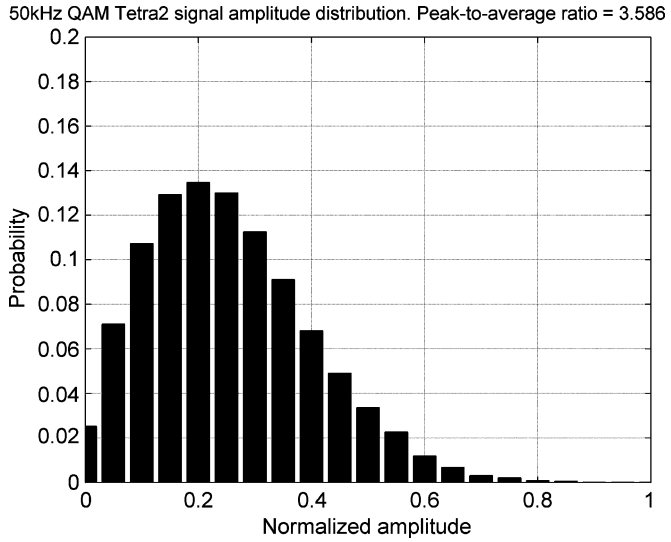

Fig. 2. Calculated amplitude distribution of 50-kHz bandwidth QAM modulated TEDS signal. The RFPA operates around 10%–50% of full output voltage amplitude most of the time.

for the TEDS) spectral masks. The design considered targets 10 mVpp of ripple, since it is assumed that the ripple spectrum can be flattened by the use of switching frequency modulation techniques, as well as by the natural dynamic switching frequency variation in the control scheme adopted.

The demand for ripple voltage this low from a high (30–50 V) supply voltage along with the high output power and a reasonable bandwidth makes the design and implementation of a suitable UFTPS an issue worthy of consideration.

III. Tracking Converter Topology

Due to the relatively low bandwidth required from the UFTPS (compared to [1], [3]–[5]), a pure switch-mode (rather than a combined linear/switch mode [5]) UFTPS solution is realistic. The synchronous rectified buck topology is selected due to its low cost, simple dynamics, and symmetrical slew-rate capability. The requirement for a control bandwidth in excess of 50 kHz suggests the use of a switching frequency in excess of $5 \cdot 50$ kHz $= 250$ kHz [8]. The output filter cutoff frequency should be 50 kHz or more to allow 50 kHz of large-signal control bandwidth. To estimate switching frequency required for maintaining sufficiently low ripple with standard second-order output filtering, consider the Fourier series representing a $D = 0.5$ PWM signal:

$$V_{\mathrm{PWM}}(t) = \frac{4}{\pi}\sin(2\pi f_{sw}t) + \frac{4}{3\pi}\sin(3\cdot 2\pi f_{sw}t) + \frac{4}{5\pi}\sin(5\cdot 2\pi f_{sw}t) + \ldots \quad (1)$$

If the $D = 0.5$ PWM signal is approximated to be free of higher harmonics, it can thus be represented as a sine wave with frequency f_{sw} and amplitude

$$V_{\mathrm{fund,PWM}} = \frac{4}{\pi}\cdot V_s. \quad (2)$$

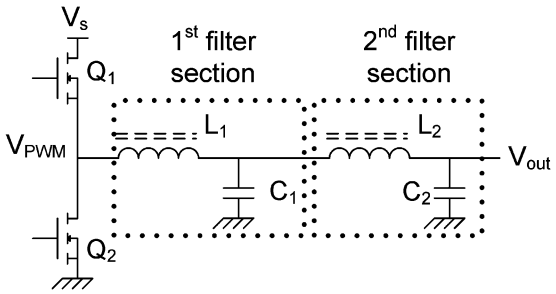

Fig. 3. Buck converter with fourth-order output filter.

A complex pole pair (as found in an LC filter) has the transfer function

$$G(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{\omega_0 Q} + 1} \quad (3)$$

If the applied signal frequency is well above ω_0, this can be simplified to

$$\underset{\omega \gg \omega_0}{G(j\omega)} \cong \frac{1}{\left(\frac{j\omega}{\omega_0}\right)^2} \quad (4)$$

which leads to the magnitude response

$$\underset{\omega \gg \omega_0}{|G(j\omega)|} \cong \left(\frac{\omega_0}{\omega}\right)^2. \quad (5)$$

In the case of a buck UFTPS with a single 50-kHz output filter switching at more than 1 MHz, this approximation should hold, leading to the approximate ripple voltage

$$\Delta V_{\mathrm{out,pp}} \approx \frac{4}{\pi}\frac{V_{\mathrm{PWM,pp}} \cdot f_{\mathrm{filter}}^2}{f_{sw}^2} \quad (6)$$

where $V_{\mathrm{PWM,pp}}$ is the peak-peak amplitude of the PWM signal, f_{sw} is the switching frequency, and f_{filter} is the output filter cutoff frequency. Solving for f_{sw} yields

$$f_{sw} \approx f_{\mathrm{filter}}\sqrt{\frac{4}{\pi}\frac{V_{\mathrm{PWM,pp}}}{\Delta V_{\mathrm{out,pp}}}}. \quad (7)$$

It follows that 10 mVpp of ripple requires a switching frequency of around 3.6 MHz, given a 50-kHz filter and an input voltage of 40 V. This is clearly much higher than what is required for adequate dynamic performance and certainly beyond what is optimal for efficiency (due to switching losses.)

One solution for reducing the switching frequency while maintaining low ripple is higher order filtering, implemented by a second *LC* filter on the buck converter, as shown in Fig. 3.

The fourth-order output filter has two complex pole pairs, similarly leading to an approximate ripple voltage of

$$\Delta V_{\mathrm{out,pp}} \approx \frac{4}{\pi}\frac{V_{\mathrm{PWM,pp}} \cdot f_{p1}^2 \cdot f_{p2}^2}{f_{sw}^4}. \quad (8)$$

Solving for f_{sw} leads to

$$f_{sw} \approx \sqrt{f_{p1}\cdot f_{p2}} \cdot \sqrt[4]{\frac{4}{\pi}\frac{V_{\mathrm{PWM,pp}}}{\Delta V_{\mathrm{out,pp}}}}. \quad (9)$$

In this case, having pole pairs at, say, 50 kHz and 375 kHz and maintaining the 10-mV_{pp} ripple requirement leads to a switching frequency of 1.15 MHz—much more manageable than the 3.6 MHz of the single-filter solution. A different approach for ripple reduction from a single-phase buck is to use a multilevel converter [9], although this has the disadvantage of requiring extra power switches.

Finding and implementing an optimal, low-cost solution to controlling the buck converter with fourth-order output filter is the focus of the work presented here.

IV. Linear Model of Power Converter

Only the output filter dynamics of the fourth-order filtered buck converter are considered here. Output filter capacitors are assumed to be very low-ESR (such as ceramic or polypropylene), types, which ensures that ESR-capacitance zeros lie outside the frequency range of interest. The transfer functions from PWM signal to the filter outputs, disregarding parasitics, form the main part of the model; they are calculated as follows:

$$G_{\text{filter1}}(s) \equiv \frac{V_{C1}(s)}{V_{\text{PWM}}(s)} = \frac{\frac{1}{sC_1} \| \left(sL_2 + \left[\frac{1}{sC_2} \| R_{\text{load}} \right] \right)}{sL_1 + \frac{1}{sC_1} \| \left(sL_2 + \left[\frac{1}{sC_2} \| R_{\text{load}} \right] \right)} \tag{10}$$

$$G_{\text{filter,tot}}(s) \equiv \frac{V_{out}(s)}{V_{\text{PWM}}(s)} = G_{\text{filter1}} \cdot \frac{\frac{1}{sC_2} \| R_{\text{load}}}{sL_2 + \frac{1}{sC_2} \| R_{\text{load}}} \tag{11}$$

which can be solved to yield equations (12)–(14), shown at bottom of page.

V. Control System Implementation

For a standard buck converter, excellent control system implementations are possible, such as the hysteresis-based PID [10], [11] control implementation shown in Fig. 4, which forms the basis for further discussion presented here. The dynamic advantages of hysteretic control (sliding mode control) are often cited [10], [12]–[14]. In [15], the dynamic advantage is argued to arise from the observation that a sliding mode control system is an oscillator, with an associated control loop crossover frequency that is equal to the switching/oscillation frequency. The need for optimal dynamics in the considered UFTPS application lead to the choice of the hysteresis based control approach.

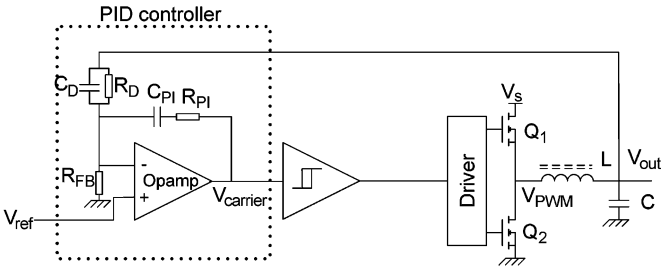

Fig. 4. PID voltage mode hysteretic controller for a buck converter [8], [9].

This controller in Fig. 4 has poles and zeros at the following frequencies:

$$f_{\text{pole,PI}} = 0 \tag{15}$$

$$f_{\text{zero,PI}} = \frac{1}{2\pi R_{\text{PI}} C_{\text{PI}}} \tag{16}$$

$$f_{\text{zero,D}} = \frac{1}{2\pi R_D C_D}. \tag{17}$$

In this implementation, the two controller zeros can be used to partially cancel the output filter poles while the integral term provides the necessary LF loop gain and HF roll-off.

Since the load impedance is not necessarily constant and well-defined, adding a second filter stage leads to a problem with filter damping, since optimal filter damping is required for optimal step response. Two fundamental approaches to controlling the output filter Q exist:

- passive damping via a dissipative device;
- active damping via the control system.

If the assumption is made that the load impedance is higher than the output filter impedance (Q is high), the use of dissipative damping means that most of the energy moved in or out of C_2 during a step, will pass through the dissipative element. This results from the definition of Q:

$$Q \equiv \frac{W_{\text{tot}}}{\Delta W} \tag{18}$$

where W_{tot} is the energy contained in the oscillation and ΔW is the energy removed from the oscillating system per oscillation cycle. When charging or discharging a capacitor between V_1 and V_2 through a resistive element, an energy amount equal to the energy moved or removed from the capacitor is lost in the resistive element. Therefore, when the UFTPS output voltage

$$G_{\text{filter1}}(s) = \frac{s^2 L_2 C_2 + s\frac{L_2}{R_{\text{load}}} + 1}{s^4 L_1 L_2 C_1 C_2 + s^3 \frac{L_1 L_2 C_1}{R_{\text{load}}} + s^2 (L_1 C_2 + L_1 C_1 + L_2 C_2) + s\frac{L_1 + L_2}{R_{\text{load}}} + 1} \tag{12}$$

$$G_{\text{filter,tot}}(s) = \frac{1}{s^4 L_1 L_2 C_1 C_2 + s^3 \frac{L_1 L_2 C}{R_{\text{load}}} + s^2 (L_1 C_2 + L_1 C_1 + L_2 C_2) + s\frac{L_1 + L_2}{R_{\text{load}}} + 1} \tag{13}$$

$$G_{\text{filter2}} \equiv \frac{V_{out}(s)}{V_{c1}(s)} = \frac{1}{s^2 L_2 C_2 + s\frac{L_2}{R_{\text{load}}} + 1} \tag{14}$$

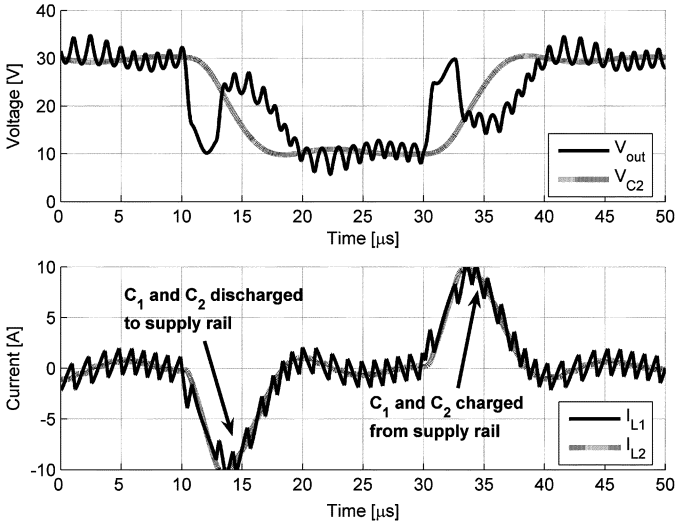

Fig. 5. Simulated filter voltages and currents in actively damped UFTPS design stepping with no output load. The average current in L_1 is 0, indicating that no energy is lost during stepping.

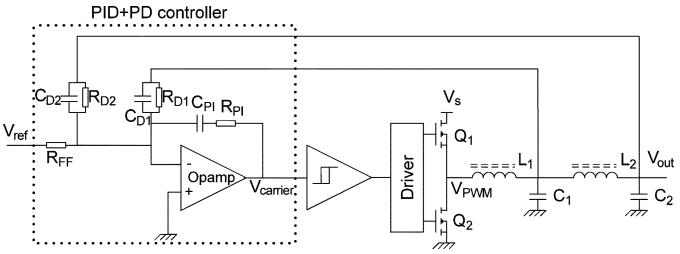

Fig. 6. Inner PID + outer PD voltage mode hysteretic controller for a buck converter with fourth-order output filter.

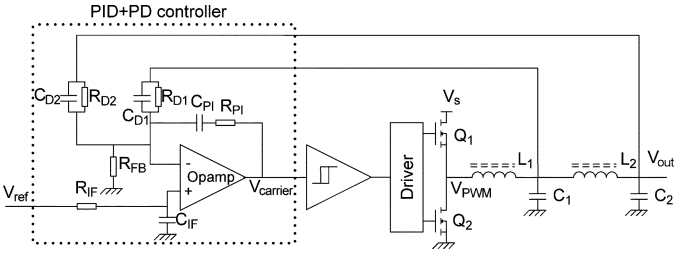

Fig. 7. Proposed PID+PD voltage mode hysteretic controller implementation with noninverting reference input.

is stepped, the following energy is dissipated in the damping device:

$$W_{\text{damp}} = \left|\frac{1}{2}C_2V_1^2 - \frac{1}{2}C_2V_2^2\right| = \frac{1}{2}C_2\left|V_1^2 - V_2^2\right|. \quad (19)$$

When the converter output voltage is pulsating between V_{bot} and V_{top} with frequency f_{step}, the power lost will be

$$P_{\text{damp}} = f_{\text{step}} \cdot 2 \cdot W_{\text{damp}} = f_{\text{step}} \cdot C_2\left(V_{\text{top}}^2 - V_{\text{bot}}^2\right). \quad (20)$$

Assuming a 50-kHz square output stepping between 20 and 30 V and $C_2 = 2.2\ \mu$F, the power dissipated will be around 55 W, which would have to be dissipated in a sizable power resistor. This power dissipation would directly reduce the full-load converter efficiency by more than ten percentage points, and this would be even more pronounced in a lower-current application. Therefore, passive damping is not a realistic or attractive option in the considered UFTPS application.

With active damping, the damped energy will be returned to the supply rail, ideally eliminating the extra power loss associated with damping. However, the active damping process will increase RMS currents in the filter and power stage components. This is evident from the simulation in Fig. 5, where the inductor currents peak at $+/-10$ A during an output voltage step, even though there is no load connected to the UFTPS output terminal. Additionally, it can be seen that the average supply current of the UFTPS (which is equal to the average current in L_1 or L_2) is zero, indicating that there are no power losses in the filter. Thus, principally, the damping process is lossless, while in practice, the filter components are stressed more than in steady-state.

Adding a feedback path from the second output filter allows very simple active damping using the already existing opamp in the controller. By using a parallel RC (R_{D2}, C_{D2}) network as shown in Fig. 6, an open-loop zero is added

$$f_{z,d2} = \frac{1}{2\pi R_{D2}C_{D2}}. \quad (21)$$

This zero is used to reduce open-loop phase lag and thereby improve closed-loop stability. The zero introduced effectively makes the outer control loop a PD (proportional-derivative) loop.

A disadvantage with the controller implementations shown in Figs. 4 and 6 is that both have inverting inputs, so that the reference voltage is inverted on the output. This can be amended by moving the reference signal injection point to the opamp noninverting input. This will be shown to affect the closed loop transfer function, but not more than can be corrected using a simple RC (R_{IF}, C_{IF}) input filter as shown in Fig. 7.

Additionally, resistor R_{FB} is added to control the closed-loop gain. The closed-loop DC gain of the UFTPS, A_V, will behave as expected for a noninverting operational amplifier

$$A_V \equiv \frac{V_{\text{out,DC}}}{V_{\text{ref,DC}}} = 1 + \frac{R_{D1}||R_{D2}}{R_{FB}}. \quad (22)$$

VI. Switching Frequency Stabilization

An additional issue that needs to be considered is the effect of switching frequency variation, a mechanism inherent to most hysteretic controllers. Since the magnitude response of the fourth-order output filter has a 24 dB/octave slope around the switching frequency, any reduction of the switching frequency will dramatically increase the ripple voltage. To suppress this mechanism, a switching frequency control loop is implemented around the hysteretic comparator, as shown in Fig. 8. The basic idea is that an MMV (monostable multivibrator or one-shot) provides frequency-to-voltage conversion, which forms the basis for a simple integrating control loop, where the error output from the integrator is phase-split to give the hysteresis window. Similar approaches are found in prior art; [12] uses parameter feed-forward instead of feedback, [13] uses a PLL to control a variable delay for fixing the switching frequency, [16] presents the use of synchronization pulses, and [17] proposes

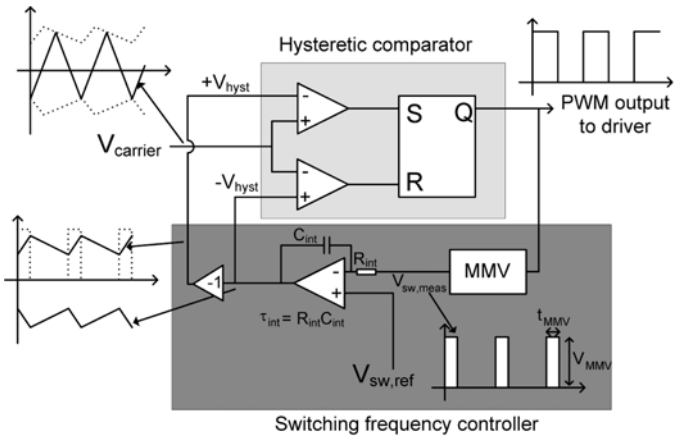

Fig. 8. Proposed constant-frequency hysteretic comparator building block.

the use of a feedback system to control the hysteresis window in the standard capacitor-ESR based hysteretic voltage controller.

The approach adopted here is thus very similar to [17], but with a different type of power converter and voltage control system. Compared to the feed-forward solution in [12] the feedback based approaches have the advantage of providing a very precise steady-state switching frequency, although the dynamic performance is probably not as good.

In order to allow simple calculation of the hysteretic control loop switching frequency, it is very useful to simplify the error amplifier output voltage $V_{\rm carrier}$ to a triangular waveform. It is hard to argue from intuition that the square PWM signal is converted into a triangular carrier signal through the two paralleled feedback loops, so this has to be analyzed via the effective controller transfer function [17], defined as the total transfer function from the switch node to the carrier input of the hysteretic comparator

$$G_{\rm ctrl}(s) \equiv \frac{V_{\rm carrier}(s)}{V_{\rm PWM}(s)} \tag{23}$$

$$G_{\rm ctrl}(s) = \frac{1+sR_{PI}C_{PI}}{sC_{PI}}\left[\frac{1+sR_{D2}C_{D2}}{R_{D2}} + \frac{1+sR_{D1}C_{D1}}{R_{D1}} \cdot \left(s^2L_2C_2 + s\frac{L_2}{R_{\rm load}} + 1\right)\right] \cdot G_{\rm filter,tot}(s) \tag{24}$$

For any positive-valued set of control loop components, $G_{\rm ctrl}(s)$ will converge towards integrator behavior at high frequencies, since it contains four zeros and five poles (all normally in the left half-plane) In a proper design, the control system will oscillate at a frequency well above pole/zero eigenfrequencies, thereby allowing the carrier signal to be assumed more or less triangular. For finding the carrier slope at $D = 0.5$ (which turns out to be a very useful parameter in the control system analysis), $G_{\rm ctrl}(s)$ is approximated to be an integrator at high frequencies

$$G_{\rm ctrl,approx}(s) = \lim_{s\to\infty} G_{ctrl}(s). \tag{25}$$

The following applies for the effective controller function:

$$\lim_{s\to\infty} G_{ctrl}(s) = \frac{R_{PI}C_{PI}}{C_{PI}}\left[\frac{sR_{D1}C_{D1}}{R_{D1}} \cdot (s^2L_2C_2)\right] \cdot \frac{1}{s^4 \cdot L_1L_2C_1C_2}. \tag{26}$$

The effective controller transfer function thus converges towards

$$\lim_{s\to\infty} G_{ctrl}(s) = \frac{R_{PI}C_{D1}}{sL_1C_1}. \tag{27}$$

Note that this expresses the fact that only the inner feedback loop is active at high frequencies. The unit step response of this integrator is then

$$V_{\rm ctrl,step}(t) = \frac{R_{PI}C_{D1}}{L_1C_1} \cdot t. \tag{28}$$

When the controller is subjected to a PWM signal transition at $D = 0.5$, the carrier signal will approximately respond with the output

$$V_{\rm carrier,approx}(t) = \frac{V_s}{2} \cdot \frac{R_{PI}C_{D1}}{L_1C_1} \cdot t. \tag{29}$$

The constant K, defined as twice the carrier dV/dt at $D = 0.5$, turns out to be useful

$$K \equiv 2 \cdot \left.\frac{dV_{\rm carrier}}{dt}\right|_{D=0.5} \cong V_s \cdot \frac{R_{PI}C_{D1}}{L_1C_1}. \tag{30}$$

To allow proper design of the switching frequency control loop, a small-signal model is needed. For the hysteretic comparator, the relationship between switching frequency and hysteresis window can be approximated [19] as

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{\rm hyst}}{K} + t_d} \tag{31}$$

where t_d is the combined comparator/power stage delay (turn-on and turn-off delays are assumed to be identical.) In the derivation of this expression, it has been assumed that the carrier signal is triangular and that the hysteresis window is symmetrical and constant.

Modelling the hysteretic comparator in the switching frequency control loop as a gain, the transfer function from hysteresis window input to switching frequency output is

$$G_{\rm hyst,sw} \equiv \frac{\partial f_{sw}}{\partial V_{\rm hyst}} = -\frac{2D(1-D)}{K\left(\frac{2V_{\rm hyst}}{K} + t_d\right)^2}. \tag{32}$$

The MMV produces a fixed pulse per positive transition in the PWM signal. The average output voltage from the MMV in a switching period is therefore

$$\langle V_{sw,\rm meas}\rangle_{T_{sw}} = \frac{t_{\rm MMV}}{T_{sw}} \cdot V_{\rm MMV} = t_{\rm MMV} \cdot V_{\rm MMV} \cdot f_{sw} \tag{33}$$

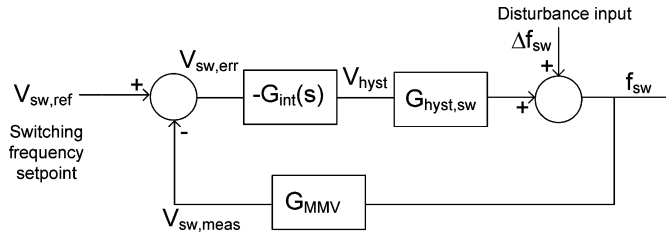

Fig. 9. Small-signal model of the switching frequency control loop.

where $V_{\rm MMV}$ is the MMV output pulse amplitude and $t_{\rm MMV}$ is the MMV pulse length. The gain from switching frequency to MMV output voltage is simply

$$G_{\rm MMV} \equiv \frac{\partial \langle V_{sw,\rm meas}\rangle_{T_{sw}}}{\partial f_{sw}} = t_{\rm MMV}\cdot V_{\rm MMV}. \tag{34}$$

The integrator block is described as usual for an integrator

$$G_{\rm int}(s) \equiv \frac{V_{\rm hyst}(s)}{V_{sw,\rm meas}(s)} = -\frac{1}{sR_{\rm int}C_{\rm int}} = -\frac{1}{\tau_{\rm int}s}. \tag{35}$$

The total small-signal model of the switching frequency control loop is shown in block diagram form in Fig. 9. To allow design for a specific loop bandwidth, the open-loop transfer function is needed. This is easily found to be

$$\begin{aligned} G_{OL,sw}(s) &\equiv G_{\rm int}(s)\cdot G_{hyst,sw}\cdot G_{\rm MMV} \\ &= -\frac{2D(1-D)\cdot t_{\rm MMV}\cdot V_{\rm MMV}}{\tau_{\rm int}\cdot K\left(\frac{2V_{\rm hyst}}{K}+t_d\right)^2\cdot s}. \end{aligned} \tag{36}$$

The crossover frequency of the switching frequency control loop is

$$f_{0,sw} = \frac{D(1-D)\cdot t_{\rm MMV}\cdot V_{\rm MMV}}{\pi\cdot\tau_{\rm int}\cdot K\left(\frac{2V_{\rm hyst}}{K}+t_d\right)^2}. \tag{37}$$

This crossover frequency directly determines the response time of the loop when the switching frequency is disturbed, for example by a duty cycle change. The exact relationship is evident when calculating the transfer function from disturbance input to switching frequency output

$$G_{\rm dist}(s) \equiv \frac{f_{sw}(s)}{\Delta f_{sw}(s)} = \frac{2\pi}{f_{0,sw}}\cdot\frac{s}{1+s\frac{2\pi}{f_{0,sw}}}. \tag{38}$$

Thus, it will take the loop the time of $1/f_{o,sw}$ to recover 63% from a step-shaped switching frequency disturbance. From the derived expressions it is also apparent that the switching frequency control loop loses its effectiveness at the extremes of duty cycle and that its bandwidth/gain varies nonlinearly with the hysteresis window voltage. The presence of the time delay t_d prevents the loop bandwidth from converging towards infinity (leading to instability in practice) for very small hysteresis windows. The relationship between switching frequency set point voltage $V_{sw,ref}$ and the steady-state switching frequency is easily found since the loop integrator removes any steady-state error, leading to

$$f_{sw}(V_{sw,ref}) = \frac{V_{sw,ref}}{t_{\rm MMV}\cdot V_{\rm MMV}}. \tag{39}$$

The switching frequency control loop thus converts the entire switching power converter into a linear voltage controlled oscillator (VCO), providing an easy opportunity for implementing frequency-hopping or similar techniques for flattening and spreading the output ripple voltage spectrum. The VCO functionality alternatively allows synchronization to a fixed clock with a phase-locked loop. (PLL)

VII. Control System Design

When modeling the hysterertic control system, the main problem lies in the nonlinear core of the system: the hysteretic comparator. Various solutions exist, such as using a describing function at the switching frequency [20], [21] in a sinusoidal-carrier system, or considering it to be a block that generally forces its own input average value to zero [22] due to the sliding-mode control action. In triangular-carrier systems, a method is also presented in [19] where a describing function approach is used to find the gains at dc and at the switching frequency separately. For this paper, an infinite gain is used to model the hysteretic comparator [18]; this is equivalent to assuming that the hysteretic comparator average input is zero as in [22], since only an infinite gain can produce a finite output from zero input. This is, of course, not entirely accurate since infinite gains do not exist. However, in the same way that an infinite gain can be useful when dealing with opamp circuits, it also turns out to be useful in hysteresis-based control systems.

The inner control loop has to be significantly faster than the second filter stage dynamics if proper damping is to be achieved. In the design shown, the second filter stage has a cutoff frequency equal to the required bandwidth (50 kHz) to make small-signal bandwidth equal to power bandwidth at minimum output ripple. The first filter stage is made significantly faster (cutoff at 375 kHz), providing sufficient power bandwidth from the inner control loop to allow effective control of the second filter stage.

A consequence of the approximation used is that the bandwidth of the inner control loop is infinite (due to the infinite gain assigned to the hysteretic comparator.) Hereby, the closed-loop transfer function (from $V_{\rm out}$ side of R_{D2} to V_{C1}, with $C_{D2}=0$) is determined solely by the placement of the zero in the feedback network

$$G_{\rm inner,CL} \cong -\frac{R_{D1}}{R_{D2}}\cdot\frac{1}{1+sR_{D1}C_{D1}}. \tag{40}$$

This assumption is only valid in the real system as long as the time constant $R_{D1}C_{D1}$ is not too short, loosely reflecting that the closed loop cannot be expected to respond faster than within a few switching cycles.

The zeros of the PID controller are as the only significant compensator parameters placed near the output filter cutoff frequency. The proportional gain of the compensator is principally irrelevant to system dynamics since the constant-frequency

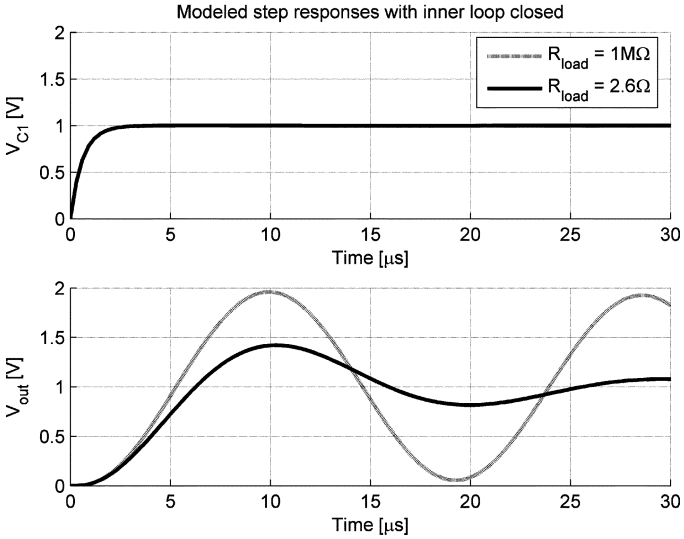

Fig. 10. Modeled closed-loop step response with the PID (inner) loop closed. Second filter stage needs damping.

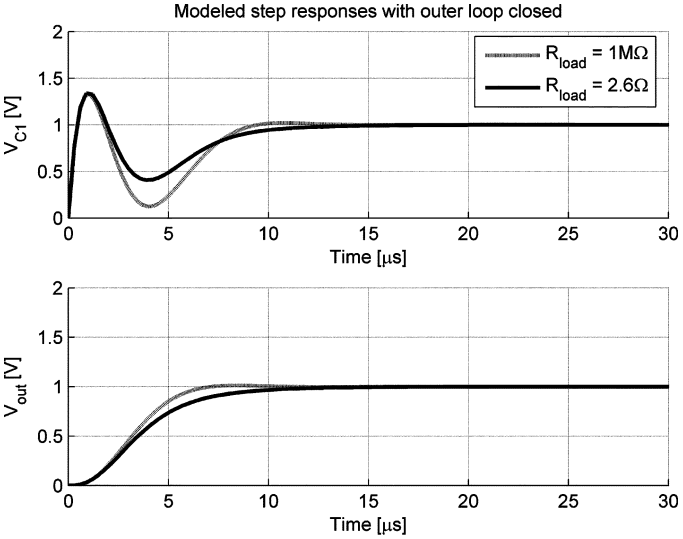

Fig. 12. Modeled closed-loop step response (from inverting input) of the basic prototype design.

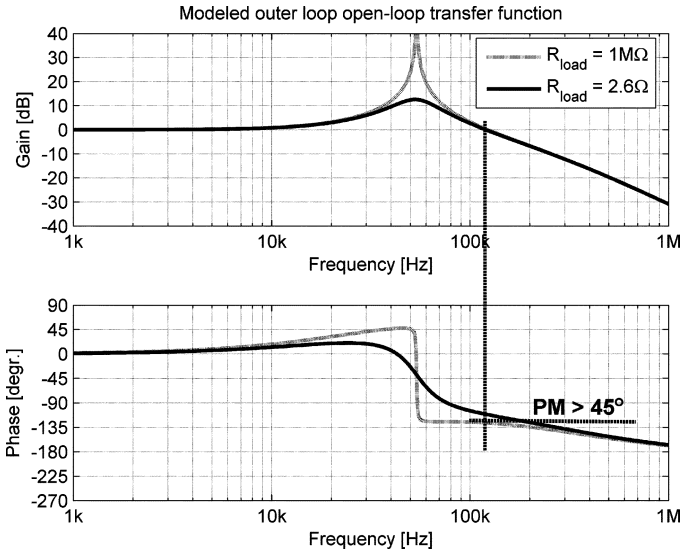

Fig. 11. Open-loop bode plot of PD (outer) control loop. Phase margin is good, ensuring a well damped closed-loop response.

TABLE I
SWITCHING FREQUENCY CONTROL LOOP PARAMETERS IN PROTOTYPE

Parameter	Value
t_{MMV}	*300ns*
V_{MMV}	*5V*
τ_{int}	*18.3μs*
K	*4.34V/μs*
$f_{o,sw}$	*55kHz*

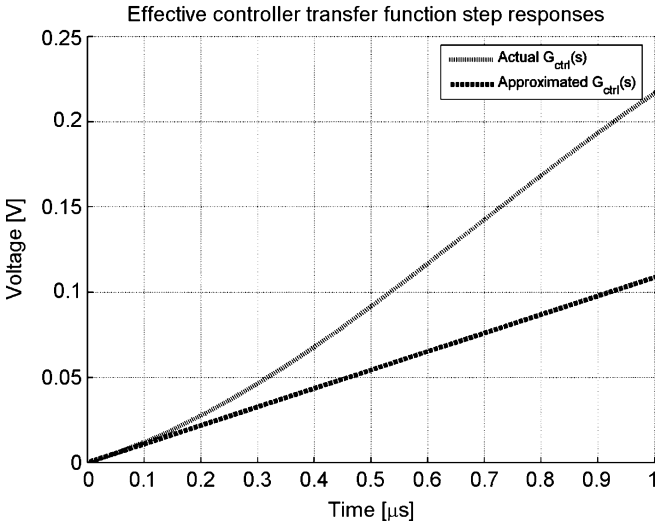

Fig. 13. Actual and approximated G_{ctrl} step responses in prototype design. The carrier signal will be monotonic within a switching cycle time frame (1 μs), ensuring proper oscillation with a hysteretic comparator.

hysteretic comparator automatically adjusts the hysteresis window to provide the desired switching frequency. Since the power converter with the hysteretic control system is basically an oscillator, fixing its switching (oscillation) frequency is (according to Barkhausen) equivalent to fixing the open-loop crossover frequency.

Using this technique, the closed-loop step response of the converter will appear as shown in Fig. 10. It is apparent that the inner loop responds quickly regardless of load and that the second filter stage needs damping.

Positive phase boost is achieved with the proposed implementation by placing the zero of the PD compensator close to the second output filter section cutoff frequency, leading to the open-loop bode plot in Fig. 11 and the closed-loop step response shown in Fig. 12. The LF loop gain is unity, but the resonant action of the undamped filter and the introduced zero provides the HF loop gain required for effective damping.

With the components determining the effective controller transfer function fixed, the switching frequency control loop can now be designed. A good starting point is to make the loop as fast as the switching frequency variations disturbing it. Thus, with a 50-kHz QAM signal, a nominal switching frequency controller bandwidth of 50 kHz is reasonable. A discussion of any adverse effects of choosing a higher bandwidth is left as a topic for future research. The parameters listed in Table I lead to this bandwidth at $D = 0.5$ according to (37). Here, the K

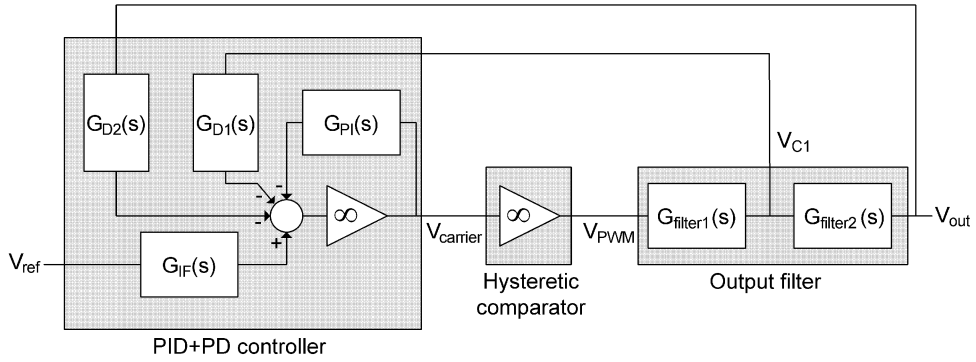

Fig. 14. Complete small-signal block diagram model of the converter with the proposed hysteretic voltage output control solution.

TABLE II
COMPENSATOR BLOCK TRANSFER FUNCTIONS IN PROPOSED CONTROL SOLUTION

$$G_{PI}(s)=\frac{s(R_{FB}\parallel R_{D1}\parallel R_{D2})C_{PI}}{1+s\cdot k_{PI,Den1}+s^2\cdot k_{PI,Den2}} \tag{41}$$

$$G_{D1}(s)=\frac{R_{D1}\parallel R_{D2}}{(R_{D1}\parallel R_{D2})+R_{PI}}\cdot\frac{1+s(R_{PI}C_{PI}+R_{D1}C_{D1})+s^2(R_{PI}R_{D1}C_{PI}C_{D1})}{1+s\cdot k_{D1,Den1}+s^2\cdot k_{D1,Den2}} \tag{42}$$

$$G_{D2}(s)=\frac{R_{D1}\parallel R_{D2}}{(R_{D1}\parallel R_{D2})+R_{PI}}\cdot\frac{1+s(R_{PI}C_{PI}+R_{D2}C_{D2})+s^2(R_{PI}R_{D2}C_{PI}C_{D2})}{1+s\cdot k_{D2,Den1}+s^2\cdot k_{D2,Den2}} \tag{43}$$

$$G_{IF}(s)=\frac{1}{1+sR_{IF}C_{IF}} \tag{44}$$

$$k_{PI,Den1}=\left((R_{FB}\parallel R_{D1}\parallel R_{D2})(C_{D1}+C_{D2}+C_{PI})+R_{PI}C_{PI}\right) \tag{45}$$

$$k_{PI,Den2}=R_{PI}(R_{FB}\parallel R_{D1}\parallel R_{D2})C_{PI}(C_{D1}+C_{D2}) \tag{46}$$

$$k_{D1,Den1}=\frac{(R_{D2}\parallel R_{FB})R_{PI}C_{PI}+(R_{D2}\parallel R_{FB})R_{D1}(C_{D1}+C_{PI})+R_{D1}R_{PI}C_{PI}}{(R_{D2}\parallel R_{FB})+R_{D1}} \tag{47}$$

$$k_{D1,Den2}=\frac{(R_{D2}\parallel R_{FB})R_{PI}R_{D1}(C_{PI}C_{D1}+C_{PI}C_{D2})}{(R_{D2}\parallel R_{FB})+R_{D1}} \tag{48}$$

$$k_{D2,Den1}=\frac{(R_{D1}\parallel R_{FB})R_{PI}C_{PI}+(R_{D1}\parallel R_{FB})R_{D2}(C_{D2}+C_{PI})+R_{D2}R_{PI}C_{PI}}{(R_{D1}\parallel R_{FB})+R_{D2}} \tag{49}$$

$$k_{D2,Den2}=\frac{(R_{D1}\parallel R_{FB})R_{PI}R_{D2}(C_{PI}C_{D2}+C_{PI}C_{D1})}{(R_{D1}\parallel R_{FB})+R_{D2}} \tag{50}$$

value is found using the integrator approximation—as can be seen from Fig. 13 this is a rough approximation in the prototype design. However, the integrator approximation provides a K value relatively easily. The resulting loop dynamics are examined in the section on experimental results.

Note that since $G_{\mathrm{ctrl}}(s)$ has a monotonic step response (as also shown in Fig. 13), proper hysteresis-mode oscillation is intuitively ensured, since the carrier will always seek towards the "right" hysteresis threshold. An analysis based on the well-established existence and hitting conditions [22] used for sliding-mode control system design could also be used.

When moving the reference injection point, the controller open-loop transfer functions will still be the same, while the closed-loop transfer function changes.

Therefore, the closed-loop transfer function of the designed controller must be recalculated for the proposed solution shown in Fig. 7. A complete small-signal model of the proposed solution is shown in Fig. 14, where the error amplifier and hysteretic comparator are modeled as infinite gains. The four controller transfer functions are listed in Table II, working from the schematic in Fig. 7.

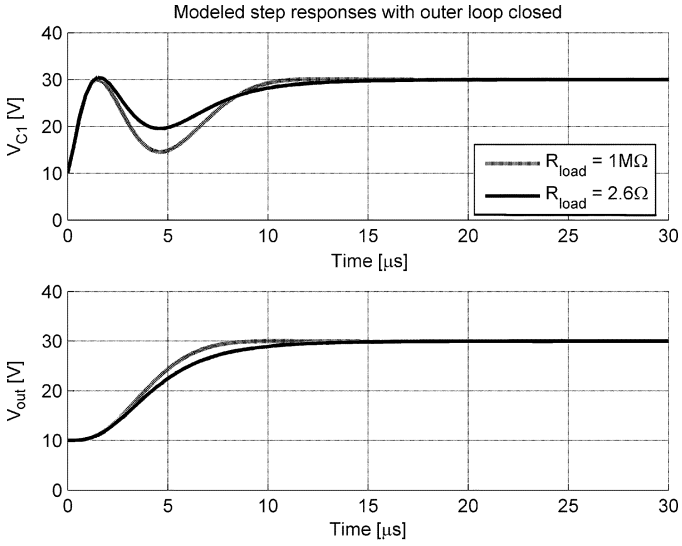

Fig. 15. Modeled (using linear system model shown in Fig. 14) closed-loop step response from noninverting reference input of UFTPS prototype design.

Using the control system model shown, the overall closed-loop response can be easily calculated numerically. Adding a reference input pole leads to the step response shown in Fig. 15. Using the same model blocks (within the Matlab/Simulink environment), replacing the hysteretic comparator model with a real hysteretic comparator leads to the simulated results shown in Fig. 16. Correspondence between results is very good, underlining the usefulness of the linear control system model for rapid control loop design. The results presented are reproducible using the control loop parameters listed in Table III.

VIII. EXPERIMENTAL RESULTS

A prototype envelope tracking power supply was constructed, using the proposed control scheme and the shown controller design. The step response of the prototype was measured and is displayed in Fig. 17 (data was imported into Matlab) for easy comparison with the corresponding modeled and simulated results.

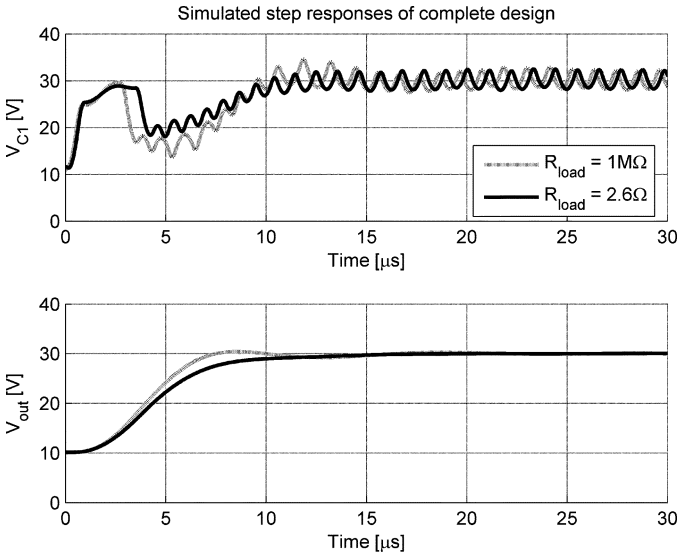

Fig. 16. Simulated (using a switching system model) closed-loop step response from noninverting reference input of UFTPS prototype design.

TABLE III
PROTOTYPE FILTER AND VOLTAGE CONTROL SYSTEM COMPONENT VALUES

Component	Value	Component	Value
L_1	3.3μH	R_{D2}	18kΩ
C_1	100nF	C_{D2}	330pF
L_2	4μH	R_{FB}	1kΩ
C_2	2.2μF	R_{P1}	1kΩ
R_{D1}	18kΩ	C_{P1}	470pF
C_{D1}	33pF	R_{IF}	1kΩ
		C_{IF}	1.5nF

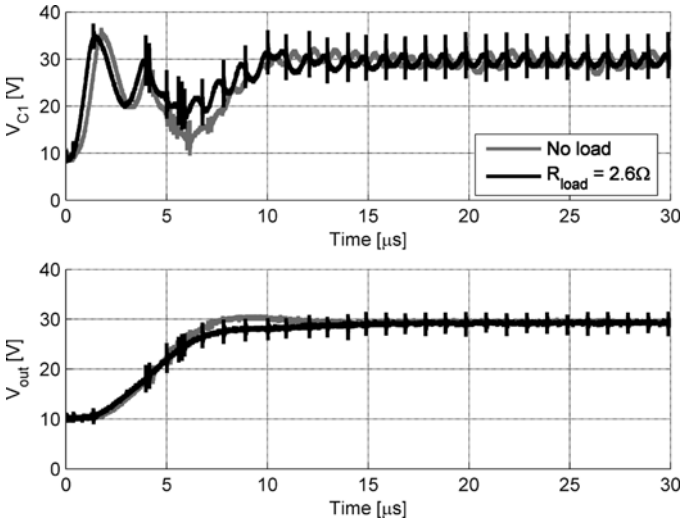

Fig. 17. Measured prototype UFTPS step responses (data imported from oscilloscope.) Output voltage behaves as expected; compare to Figs. 15 and 16. Hard-switched high-side turn-on causes noise spikes with the 2.6 Ω load.

The measured switching patterns are slightly different from simulated ones (as evident from V_{c1}), but the overall output voltage responses match very well.

A picture of the prototype is shown in Fig. 18, and key specifications are summarized in Table IV. The prototype used ground planes extensively, the power stage decoupling was handled by plane capacitance and 17.6 μF of low-inductance polyester capacitance.

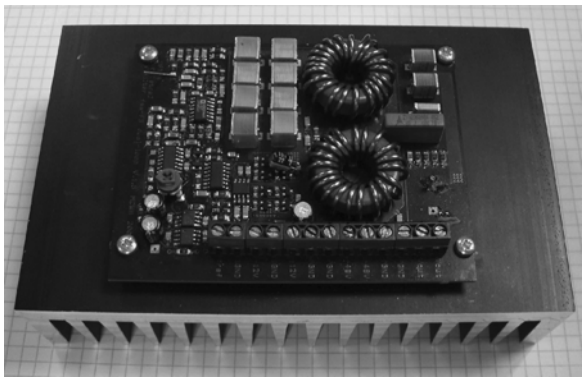

Fig. 18. UFTPS prototype for experimental verification. Die-size SMD Power MOSFETs are mounted on the PCB bottom side, gap filler pads provide thermal interfacing with the heat sink.

TABLE IV
KEY PROTOTYPE SPECIFICATIONS

Input voltage	20 – 60V
Output voltage @ 40V input	10 – 30V
Output ripple voltage (p-p)	<10mV
Output current	0 – 18A
Efficiency @ 18A output current	88 – 95%
Idle power stage losses	750mW
Power bandwidth	50kHz

A fast 100-V half-bridge driver IC provided the gate signals, additional low-inductive pull-down capability was added using discrete bipolar transistors. A relatively large low-permeability iron-powder core was used for the first filter inductor to minimize the core loss caused by the considerable ripple current. Due to the low ratio of dc-to-ac inductor current, this inductor had a saturation current of 100 A. A gapped ferrite cored inductor could be made smaller due to the reduced core loss per flux swing.

A key feature of the implemented UFTPS prototype is its high efficiency in spite of the high switching frequency. This increase in efficiency is the result of the use of new component technology—namely die-size packaged SMD power MOSFETs. The extremely low package inductances of such devices allow high switch-node dV/dt without parasitic turn-on, leading to fast switching times and low power stage delay. The low delay is instrumental in allowing effective control of the switching frequency over a wide duty cycle range. These observations are clear when a comparison is made with the very similar UFTPS design published in [23], which uses TO-220 packaged devices with associated package inductances. The use of new power devices leads to higher efficiency (Fig. 19) while operating at higher switching frequencies (Fig. 20) and producing much less ripple (Fig. 21). Satisfactory performance has hereby been obtained without resorting to more complex multiphase power conversion. The cost increase associated with extra filtering components in the fourth-order filter is arguably more than compensated for since power transistors and high-speed silicon drivers have costs per item similar to that of a power inductor. Additionally, each phase of a multiphase converter needs its own inductor. The extra PCB area necessary to accommodate the fourth-order output filter is not a major concern in base station applications.

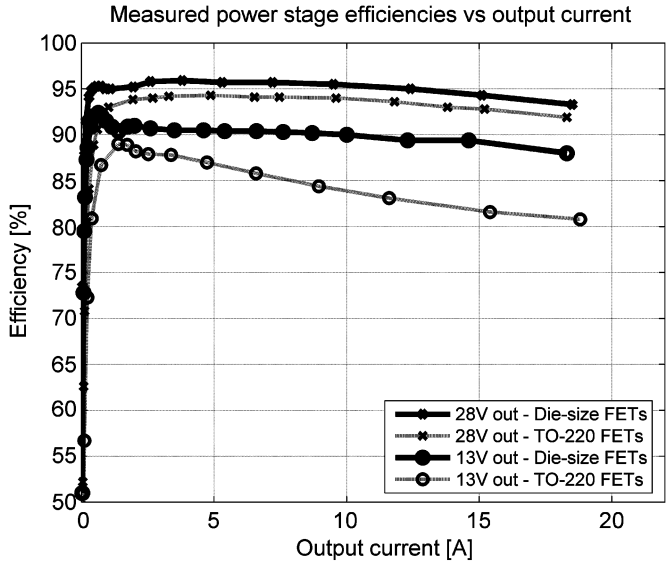

Fig. 19. Measured (using Voltech PM3000A power analyzer) power stage efficiency of UFTPS prototype using die-size power MOSFETs, compared against prototype design using TO-220 power devices [23].

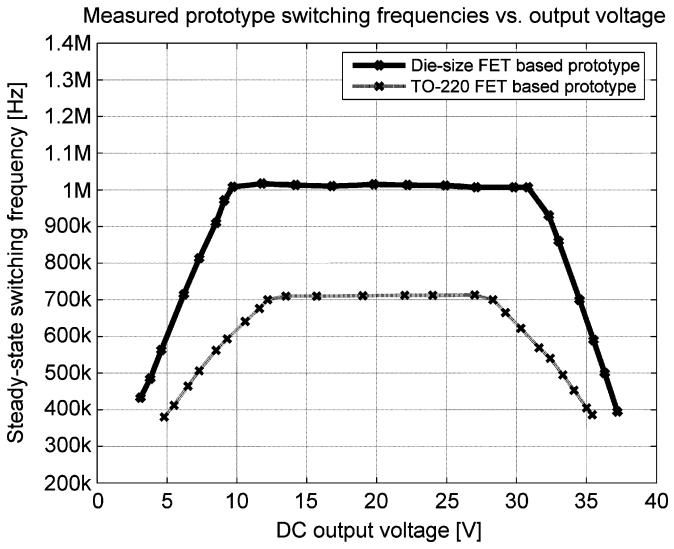

Fig. 20. Measured switching frequency of UFTPS prototype using die-size power MOSFETs, compared against prototype design using TO-220 power devices [23].

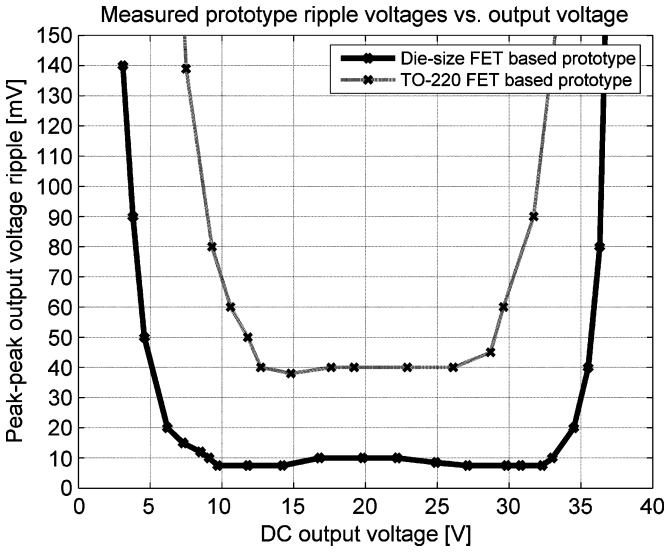

Fig. 21. Measured ripple voltage of UFTPS prototype using die-size power MOSFETs, compared against prototype design using TO-220 power devices [23].

TABLE V
COMPARATOR/POWER STAGE COMPONENTS USED IN DIE-SIZE MOSFET PROTOTYPE

Power MOSFETs	IRF6644 (IR)	10mΩ/100V
MOSFET driver	HIP2101 (Intersil)	2A/100V/45ns
Comparator	NE521 (ST)	12ns
SR latch	74AC74	5ns

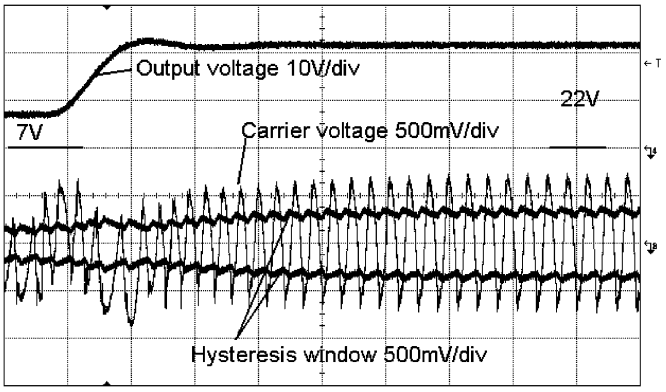

Fig. 22. Measured carrier and hysteresis window voltages during output voltage step (time base 5 μs/div). Switching frequency control loop readjusts the switching frequency in about 20 μs. Steady-state switching frequency is set to 600 kHz for waveform clarity.

Note that the efficiencies measured do not account for power loss in the power MOSFET gate drivers (around 1 W), as well as the remaining control circuitry (around 200 mW.)

The faster switching enabled by the use of die-size MOSFETs also makes the switching frequency control loop more ideal. Inspecting Fig. 20, the prototype is capable of maintaining 1-MHz switching frequency for D in the range of [0.25, 0.75], ensuring low ripple (10 mV_{pp} or less) for output voltages in the intended range of 10–30 V, as evident from Fig. 21. The components used for achieving the low time delay are listed in table Table V. Additionally, a 50-ns fixed dead time was inserted to avoid shoot-through.

The dynamic performance of the implemented switching frequency control loop is demonstrated in Fig. 22. Following an output voltage step from 7 V ($D = 0.175$) to 22 V ($D = 0.55$), the hysteresis window opens up to maintain the switching frequency, reaching a new steady state in about 20 μs, roughly reflecting the control bandwidth of 55 kHz.

When operating with the intended TEDS envelope signal (which is similar to the idealized waveforms shown in Fig. 1), the UFTPS responds as shown in Figs. 23 and 24. Regardless of load (as long as it is above 1–2 Ω) the UFTPS quickly and accurately reproduces the reference voltage.

Finally, since the UFTPS is basically an amplifier, it can also be characterized it by its frequency response. Calculated and

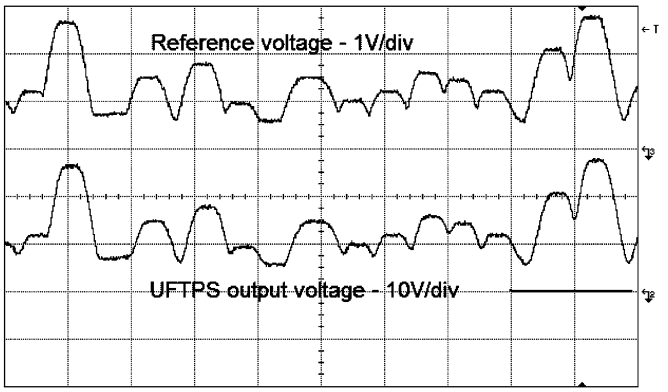

Fig. 23. Measured UFTPS prototype output with 50-kHz QAM envelope tracking—no load. Time base 50 μs/div.

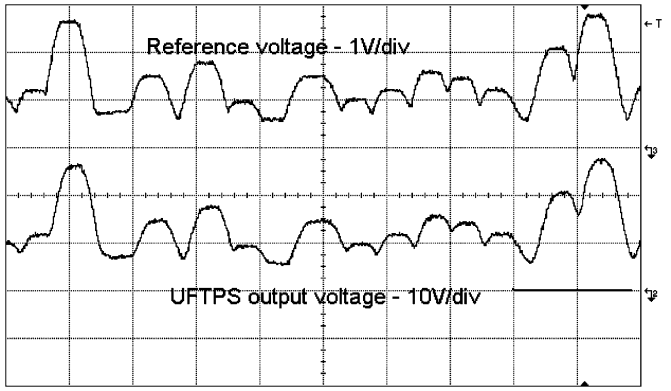

Fig. 24. Measured UFTPS prototype output with 50-kHz QAM envelope tracking—2.6 Ω load. Time base 50 μs/div.

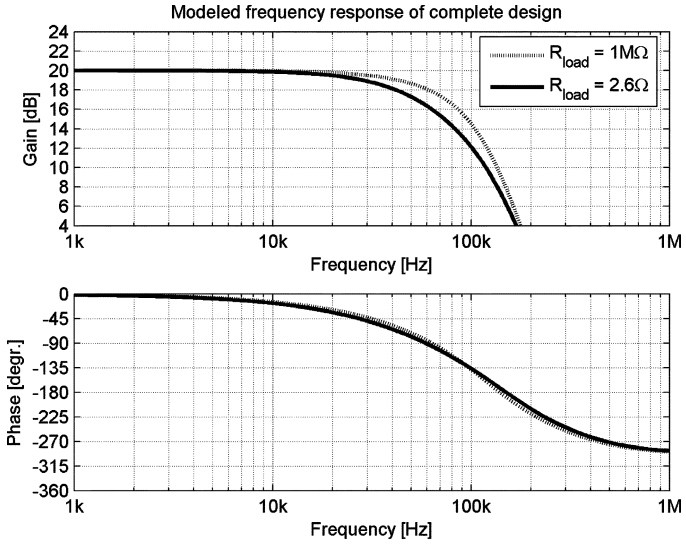

Fig. 25. Modeled UFTPS prototype small-signal frequency responses.

measured frequency responses are compared in Figs. 25 and 26; again the model is a good predictor of measured behavior and the design has the well-damped, load-independent frequency response that could be expected from the step response results.

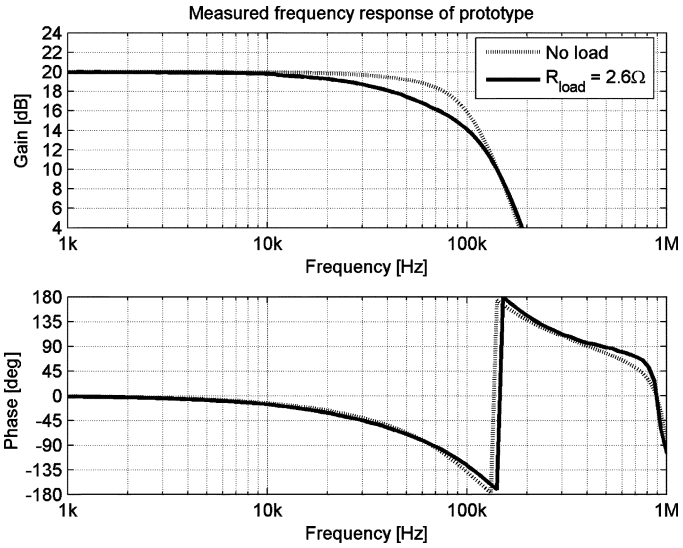

Fig. 26. Measured UFTPS prototype small-signal frequency responses.

IX. Conclusion

An effective solution for implementing high-efficiency, low-ripple, high-bandwidth dc-dc converters for powering RFPAs has been introduced, along with a set of modeling and design tools. The solution was demonstrated in a 10–30 V output UFTPS, capable of 18-A output current and 10-μs response time, while maintaining output ripple below 10 $\mathrm{mV_{pp}}$, and providing 88%–95% efficiency from a single-phase buck converter. The performance presented was enabled by the combination of higher-order filtering, a new and simple loop compensation scheme, constant-frequency hysteretic control and new power device technology.

The success of this particular combination is due to the effective synergy between solutions; new power devices allow fast-switching, efficient single-phase buck power stages while hysteretic control allows this power stage to provide optimal dynamic performance due to the very high loop bandwidth. The ripple/efficiency penalty from using a single-phase buck is mitigated by the use of fourth-order filtering, while the switching frequency control loop eliminates detrimental effects otherwise resulting from the use of hysteretic control with fourth-order filtering. The net result is a simple UFTPS solution, providing very high overall performance without resorting to the use of a more expensive multiphase power stage.

A practical approach for modeling the hysteretic control system in the s-domain has been developed and demonstrated, enabling accurate prediction and optimization of the closed-loop dynamics of the UFTPS. Additionally, the loop dynamics of the switching frequency control loop have been analyzed, based on the proposed method of approximating the effective controller transfer function as an integrator at high frequencies.

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A small-signal model of the hysteretic comparator in linear-carrier self-oscillating switch-mode controllers

Mikkel C. W. Høyerby, Michael A. E. Andersen

***Abstract*—This paper presents a small-signal model for the hysteretic comparator, a vital but not very well-understood component often used in controllers for high-performance switching power converters. It will be shown that comparator/power stage delay is the key limiting factor on loop gain in linear-carrier hysteretic controllers, which is ideally infinite at DC. The reasoning behind the model is explained, and the model is verified against simulated and measured gain-phase plots. The presented model allows precise calculation of the LF loop gain in the linear-carrier class of self-oscillating hysteretic controllers, which is particularly useful in the design of switching amplifiers.**

***Index Terms*—Hysteretic control, comparator model, self-oscillating, small-signal**

INTRODUCTION

The term hysteretic control encompasses a wide variety of control schemes usable in many power electronics applications from switch-mode audio amplification to DC/DC converters [1-5]. The key component in any hysteretic controller is the hysteretic comparator; this device ensures that the control loop error voltage (carrier) oscillates between well-defined limits, thereby ensuring switching action and zero average error. Although highly non-linear, the hysteretic comparator is used in highly linear audio amplifiers, which suggests that it can be modeled very well as a linear component. In this context it should be noted that the hysteretic comparator behaves differently from the standard PWM modulator described in the literature [6], as shown in [5] and [7].

This paper presents an approach for modeling the hysteretic comparator as a linear, continuous-time transfer function.

STARTING POINT – A VERY SIMPLE MODEL

The modeling of the hysteretic comparator was considered in [5], where the aim was to allow prediction of the dynamic behavior of a closed-loop system. For this purpose, the concept of simply modeling the hysteretic comparator as an infinite gain was introduced, and proved very useful. It has since been used in a rather different configuration [8] with equal success.

The model rests on the argument that in a system without DC feedback (such as the bandpass current-mode control loop shown in Figure 1), an infinitely small DC perturbation on the hysteretic comparator input will cause the carrier to not reach one of the hysteresis limits, saturating the comparator output (see Figure 1.)

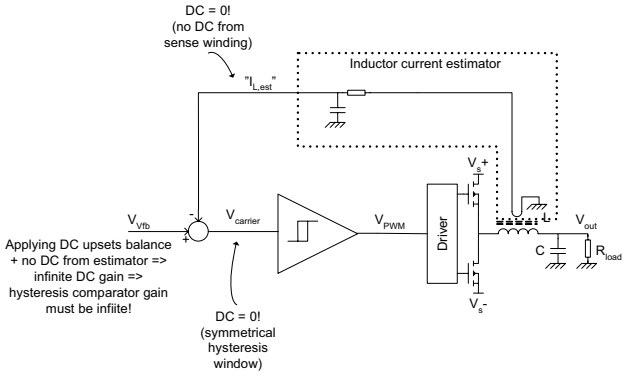

Figure 1. Derivation of the "infinite-gain" hysteretic comparator model in a band-pass current-mode (BPCM) loop (from [8].)

The problem with this very simple model is that infinite gains do not exist, and having an infinite gain within a control loop would lead to infinite loop gain and zero errors, which was certainly not the case in [5]. The actual gain-phase characteristics of a hysteretic comparator was measured in [8] and shown in Figure 2.

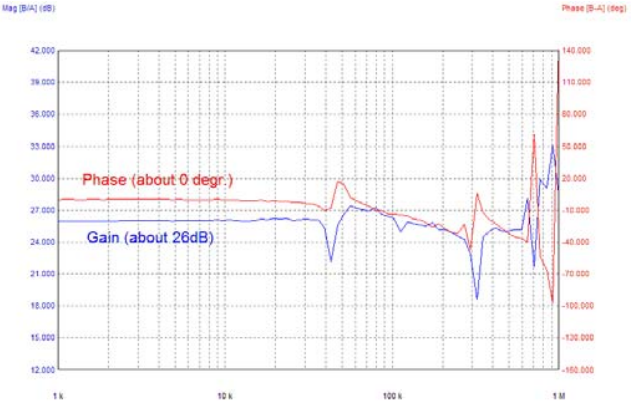

Figure 2. Example of measured hysteretic comparator gain-phase plot (from [8].) Gain is far from infinite.

It can be argued that a flat 26dBs of gain is quite far from infinite, and therefore the aim of the work presented in this paper was to identify the reason behind this discrepancy and

reassess the validity of the "infinite-gain" hysteretic comparator model.

THE EFFECT OF DELAY--A MORE ELABORATE MODEL

Inspection of the shape of the carrier signal under dynamic conditions (see measurement in [8] or simulated waveforms for an AIM[9] controller in Figure 3 and Figure 4) reveals an important clue: The mean value of the carrier signal (averaged over one switching cycle) isn't actually zero, and it varies with the duty cycle. This means that a change in the DC carrier voltage is required to effect a DC change in the PWM output voltage, which by definition means that the hysteretic comparator must have finite DC gain.

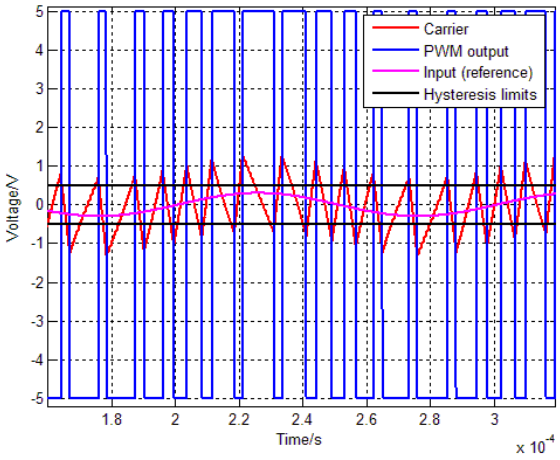

Figure 3. Simulated input (carrier) and output (PWM) from hysteretic comparator in an AIM control loop with significant delay; the delay causes carrier to exceed the hysteresis limits in a duty-cycle dependent way.

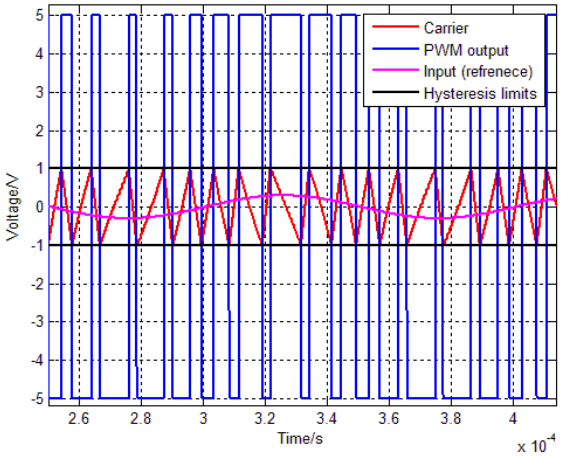

Figure 4. Simulated input (carrier) and output (PWM) from hysteretic comparator in an AIM control loop with negligible delay; carrier stays within the hysteresis window.

A more exact study of the DC relations between the carrier signal and the PWM output voltage is carried out, based on the carrier signal description shown in Figure 6. The idea is to use the DC small-signal gain together with the calculated gain at the switching frequency, and tying these two gains together with a 1st order transfer function to obtain a complete small-signal model for frequencies from DC to the switching frequency. This is quite an "ad hoc" approach compared to "describing function" analysis, but the effectiveness of this approach in the considered case will be demonstrated. To allow relatively easy analysis of a range of systems, the carrier signal is assumed to be linear (i.e. it is triangular with constant slopes). The simplest hysteretic controller with such a carrier is the AIM (Astable Integrating Modulator), as shown in Figure 5.

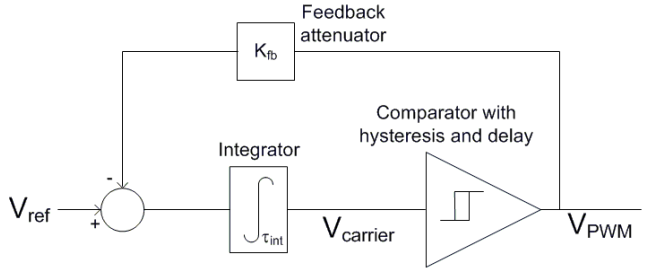

Figure 5. The considered system in its simplest form – an AIM (a.k.a. "analog sigma-delta") control loop.

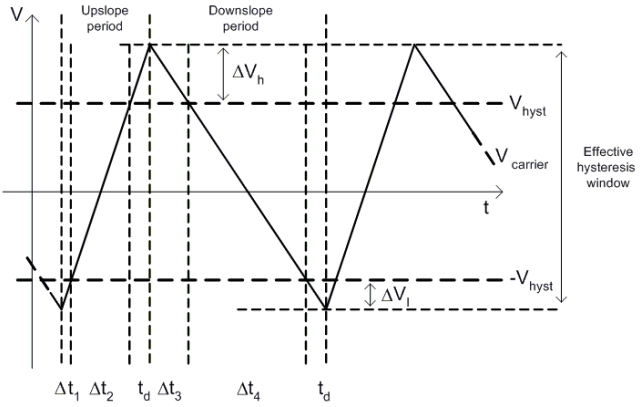

Figure 6. Definitions used for describing the carrier signal under steady-state conditions in a linear-carrier hysteretic controller with delay.

The carrier signal slopes are key quantities in the DC analysis, with a number of controller parameters wrapped into the constant *K* the slopes can simply be written as:

$$\frac{dV_{carrier,upslope}}{dt} = K \cdot D$$

$$\frac{dV_{carrier,downslope}}{dt} = -K \cdot (1-D)$$

K is defined as twice the carrier *dV/dt* at *D=0.5*:

$$K \equiv 2\frac{dV_{carrier}}{dt}, D = \frac{1}{2}$$

The switching frequency is per definition given by:

$$f_{sw} \equiv \frac{1}{\Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 + 2t_d}$$

The remaining key quantities can be expressed as:

$$\Delta V_h = t_d \cdot \frac{dV_{carrier,upslope}}{dt} = t_d \cdot K \cdot D$$

$$\Delta V_l = t_d \cdot \frac{dV_{carrier,downslope}}{dt} = t_d \cdot K \cdot (1-D)$$

$$\Delta t_1 = \frac{\Delta V_l}{\frac{dV_{carrier,upslope}}{dt}} = t_d \cdot \frac{1-D}{D}$$

$$\Delta t_3 = \frac{\Delta V_h}{\frac{dV_{carrier,downslope}}{dt}} = t_d \cdot \frac{D}{1-D}$$

$$\Delta t_2 = \frac{2V_{hyst}}{\frac{dV_{carrier,upslope}}{dt}} = \frac{2V_{hyst}}{K \cdot D}$$

$$\Delta t_4 = \frac{-2V_{hyst}}{\frac{dV_{carrier,downslope}}{dt}} = \frac{2V_{hyst}}{K \cdot (1-D)}$$

Note that determining the carrier over/undershoot and the individual time segments would be considerably tougher for most other waveforms.

The switching frequency is thus given as:

$$f_{sw} = \frac{D(1-D)}{2\frac{V_{hyst}}{K} + t_d}$$

Assuming that the carrier slopes are linear, the time delay introduces a *D*-dependent DC offset to the hysteresis window and thereby the carrier:

$$V_{offset,carrier} = \frac{(V_{hyst} + \Delta V_h) + (-V_{hyst} + \Delta V_l)}{2}$$

$$V_{offset,carrier} = \frac{1}{2}(\Delta V_h + \Delta V_l)$$

$$V_{offset,carrier} = K \cdot t_d \left(D - \frac{1}{2} \right)$$

Note: Zero offset at *D=0.5*. The DC signal present on the comparator input is determined *only* by constants and D. The DC offset is effectively found by finding the mean value of one cycle of the carrier signal; this would again be significantly harder for most other waveforms.

The small-signal DC gain of the hysteretic comparator and power stage is by definition the ratio of output DC change to input DC change. Therefore:

$$A_{V,hyst,DC} \equiv \frac{\Delta V_{PWM,DC}}{\Delta V_{offset,carrier}}$$

$$\Delta V_{offset,carrier} = K \cdot t_d \cdot \Delta D$$

Since the relationships between *D* and DC value of the PWM signal are different in single-supply and dual (+/-) supply cases, an expression for the DC gain of the hysteretic comparator is derived in each case:

Single-supply (+V_s):

$$V_{PWM,DC} = V_s \cdot D$$

$$\Delta V_{PWM,DC} = V_s \cdot \Delta D$$

$$A_{V,hyst,DC} = \frac{V_s \cdot \Delta D}{K \cdot t_d \cdot \Delta D} = \frac{V_s}{K \cdot t_d}$$

Dual-supply (+/-V_s):

$$V_{PWM,DC} = 2V_s \cdot \left(D - \frac{1}{2} \right)$$

$$\Delta V_{PWM,DC} = 2V_s \cdot \Delta D$$

$$A_{V,hyst,DC} = \frac{2V_s \cdot \Delta D}{K \cdot t_d \cdot \Delta D} = \frac{2V_s}{K \cdot t_d}$$

Note that the DC gain is found to be independent of the hysteresis window (as also concluded in [7]) and that loops with zero time delay will have infinite DC gain, as concluded in [5]. The key factor in limiting the hysteretic comparator low-frequency small-signal gain to less than infinity is therefore undoubtedly time delay. Also worth noting is that although reducing K seems to be a way to increase the DC gain, doing so will also reduce the feedback path gain accordingly, so that the total LF loop gain remains constant. The time delay (or time delay to supply voltage ratio) is therefore the all-important factor to reduce when the loop gain of an AIM loop is to be maximized for a given switching frequency.

Assuming the hysteretic comparator to be operating linearly, its gain at the switching frequency is equal to the ratio of PWM signal fundamental amplitude to carrier signal fundamental amplitude:

$$A_{V,hyst,fsw} \equiv \frac{V_{PWM,fsw}}{V_{carrier,fsw}}$$

Using the Fourier series for the square PWM (assuming single-supply) and the triangular carrier, assuming *D=0.5*:

$$V_{PWM,fsw} = \frac{4}{\pi} \cdot \frac{1}{2} \cdot V_s = \frac{2V_s}{\pi}$$

$$V_{carrier,fsw} = \frac{8}{\pi^2} \cdot (V_{hyst} + \Delta V_h) = \frac{8}{\pi^2} \left(V_{hyst} + \frac{K \cdot t_d}{2} \right)$$

$$A_{V,hyst,fsw} = \frac{\pi}{4} \cdot \frac{V_s}{V_{hyst} + \frac{K \cdot t_d}{2}}$$

Which only applies for *D=0.5*. A more complex expression can be derived for other *D* values, which will be shown later in this paper.

Similarly for dual-supply:

$$V_{PWM,fsw} = \frac{4}{\pi} \cdot V_s$$

$$A_{V,hyst,fsw} = \frac{\pi}{2} \cdot \frac{V_s}{V_{hyst} + \frac{K \cdot t_d}{2}}$$

Making an assumption about the controller used may allow replacement of *K* with something that contains V_s so that the influence of V_s becomes clearer. This is the case with an AIM:

$$K_{AIM} = 2 \cdot \frac{\frac{1}{2} V_s K_{fb}}{\tau_{\text{int}}} = \frac{V_s K_{fb}}{\tau_{\text{int}}}$$

$$A_{V,hyst,AIM,DC} = \frac{\tau_{\text{int}}}{K_{fb} \cdot t_d}$$

Here it is again important to note that the fundamental limiting factor to the LF small-signal gain of the AIM control loop is the time delay. Simply increasing τ_{int} will not increase to overall LF loop gain of the AIM loop since the increase in hysteretic comparator gain will be exactly offset by the decreased integrator gain. Additionally, the small-signal DC gain of the hysteretic comparator is found to be independent of the supply configuration.

$$A_{V,hyst,AIM,fsw} = \frac{\pi}{4} \cdot \frac{V_s}{V_{hyst} + \frac{V_s K_{fb} \cdot t_d}{2\tau_{\text{int}}}} = \frac{\pi}{4} \cdot \frac{1}{\frac{V_{hyst}}{V_s} + \frac{K_{fb} \cdot t_d}{2\tau_{\text{int}}}}$$

$$f_{sw,AIM}(D) = \frac{D(1-D)}{2\frac{V_{hyst}\tau_{\text{int}}}{V_s K_{fb}} + t_d}$$

For D = 0.5:

$$f_{sw,AIM}(0.5) = \frac{0.25}{2\frac{V_{hyst}\tau_{\text{int}}}{VK_{fb_s}} + t_d} = \frac{1}{8\frac{V_{hyst}\tau_{\text{int}}}{V_s K_{fb}} + 4t_d}$$

Similarly for dual-supply:

$$K_{AIM} = 2 \cdot \frac{V_s K_{fb}}{\tau_{\text{int}}} = \frac{2V_s K_{fb}}{\tau_{\text{int}}}$$

$$A_{V,hyst,AIM,DC} = \frac{\tau_{\text{int}}}{K_{fb} \cdot t_d}$$

$$A_{V,hyst,AIM,fsw} = \frac{\pi}{2} \cdot \frac{V_s}{V_{hyst} + \frac{V_s K_{fb} \cdot t_d}{\tau_{\text{int}}}} = \frac{\pi}{2} \cdot \frac{1}{\frac{V_{hyst}}{V_s} + \frac{K_{fb} \cdot t_d}{\tau_{\text{int}}}}$$

$$f_{sw,AIM}(D) = \frac{D(1-D)}{2\frac{V_{hyst}\tau_{\text{int}}}{2V_s K_{fb}} + t_d}$$

For D = 0.5:

$$f_{sw,AIM}(0.5) = \frac{0.25}{2\frac{V_{hyst}\tau_{\text{int}}}{2V_s K_{fb}} + t_d} = \frac{1}{4\left[\frac{V_{hyst}\tau_{\text{int}}}{V_s K_{fb}} + t_d\right]}$$

For finding the complete small-signal transfer function of the hysteretic comparator, the system is assumed to be 1st-order. This means that the gains at DC and f_{sw} define a single possible solution, depending on which gain is the highest or lowest.

If $A_{v,hyst,DC} > A_{v,hyst,fsw}$ then the small-signal transfer function must contain a pole:

$$G_{hyst}(s) \equiv \frac{V_{PWM}(s)}{V_{carrier}(s)} = \frac{A_{v,hyst,DC}}{1 + \tau_p s}$$

The problem is then to choose τ_p so that:

$$\left|G_{hyst}(j2\pi f_{sw})\right| = A_{v,hyst,fsw}$$

This can be expressed as:

$$A_{v,hyst,fsw} = \left|\frac{A_{v,hyst,DC}}{1 + \tau_p \cdot j2\pi f_{sw}}\right|$$

Leading to:

$$\tau_p = \frac{\sqrt{\left(\frac{A_{v,hyst,DC}}{A_{v,hyst,fsw}}\right)^2 - 1}}{2\pi f_{sw}}$$

Likewise, if $A_{v,hyst,DC} < A_{v,hyst,fsw}$ then the small-signal transfer function is assumed to contain a zero, very similarly leading to:

$$G_{hyst}(s) \equiv \frac{V_{PWM}(s)}{V_{carrier}(s)} = A_{v,hyst,DC}(1 + \tau_z s)$$

With

$$\tau_z = \frac{\sqrt{\left(\frac{A_{v,hyst,fsw}}{A_{v,hyst,DC}}\right)^2 - 1}}{2\pi f_{sw}}$$

AN EXPERIMENT - EXTENDED MODEL FOR D≠0.5

The gain of the hysteretic comparator at the switching frequency will still by definition be given by the ratio of the PWM signal fundamental amplitude to the carrier fundamental amplitude for values of *D* different from *0.5*. For the variable-*D* carrier signal, the fundamental frequency complex Fourier coefficient is found to be:

$$c_{1,carrier}(D) = \frac{1}{4} \frac{2V_{hyst} + \Delta V_h + \Delta V_l}{\pi^2 D(1-D)} \left[\cos(2\pi D) - 1 - j \cdot \sin(2\pi D)\right]$$

More usefully, this means that the fundamental amplitude is:

$$V_{carrier,fsw}(D) \equiv 2 \cdot \left|c_{1,carrier}(D)\right|$$

$$V_{carrier,fsw}(D) = \frac{1}{2} \frac{2V_{hyst} + \Delta V_h + \Delta V_l}{\pi^2 D(1-D)} \sqrt{(\cos(2\pi D) - 1)^2 + (\sin(2\pi D))^2}$$

Similarly the following applies for the output PWM signal (with single-supply):

$$c_{1,PWM}(D) = \frac{V_s}{j2\pi}\left[1 - e^{(-j2\pi D)}\right]$$

This again is used to find the fundamental amplitude:

$$V_{PWM,fsw}(D) \equiv 2 \cdot \left|c_{1,PWM}(D)\right|$$

$$V_{PWM,fsw}(D) = \frac{V_s}{\pi} \sqrt{\sin^2(2\pi D) + (1 - \cos(2\pi D))^2}$$

The found fundamental amplitudes are again used to express the small-signal gain of the comparator at the switching frequency:

$$A_{V,hyst,fsw}(D) \equiv \frac{V_{PWM,fsw}(D)}{V_{carrier,fsw}(D)}$$

This leads to:

$$A_{V,hyst,fsw}(D) = \frac{\frac{V_s}{\pi}\sqrt{\sin^2(2\pi D)+(1-\cos(2\pi D))^2}}{\frac{1}{2}\frac{2V_{hyst}+\Delta V_h+\Delta V_l}{\pi^2 D(1-D)}\sqrt{(\cos(2\pi D)-1)^2+(\sin(2\pi D))^2}}$$

The idea is then to use this expression can be used together with the already developed model to get a complete model for any *D*. It will turn out, however, that the model accuracy is reduced with the any-*D* extension at the extremes of the *D* range.

VERIFICATION TOOLS

The proposed model was tested both against data from a simulated AIM loop and 3 different switching control loops. To obtain each point in the simulated magnitude response of the hysteretic comparator, the simulation model was perturbed with the frequency of interest, and carrier and PWM FFTs provide data on the input/output magnitudes at the perturbation frequency, much like a real gain/phase analyzer operates.

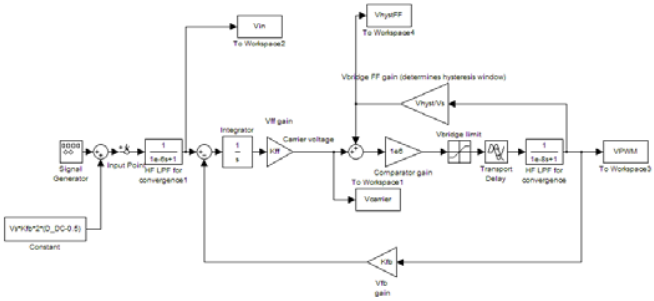

Figure 7. Switching model of an AIM control loop, as implemented in Simulink, used for providing simulated gain/phase data and the plots in Figure 3 and Figure 4.

An AP Instruments Model 200 gain/phase analyzer provided the experimental data from a linear-carrier BPCM class-D amplifier (Figure 8), a non-linear-carrier 4th-order-filtered buck converter (Figure 9) and a dedicated AIM loop test board (Figure 10.)

All controllers were perturbed via their reference inputs, and the gain/phase characteristics measured directly across the hysteretic comparator/driver/power stage. The perturbation amplitude in all cases was chosen low enough to cause less than 10% duty cycle variation in the various controllers.

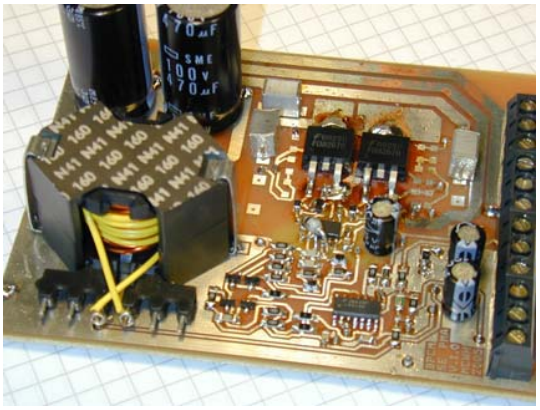

Figure 8. Hysteretically-controlled 200W class-D power amplifier prototype with linear carrier used for providing experimental gain-phase data.

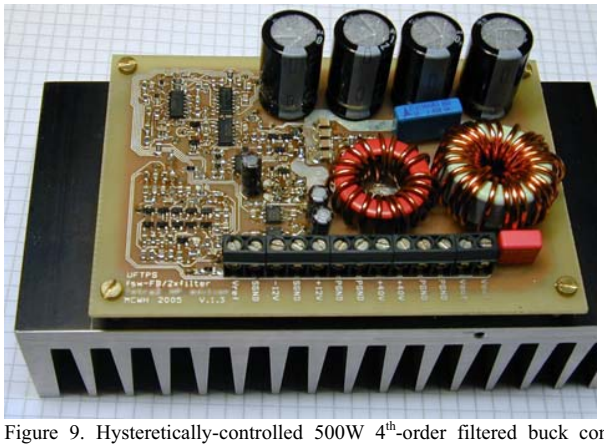

Figure 9. Hysteretically-controlled 500W 4th-order filtered buck converter prototype with non-linear carrier used for providing experimental gain-phase data.

Figure 10. AIM loop experimentation PCB used for providing experimental gain-phase data with well-defined model parameters.

MODEL VERIFICATION BY SIMULATION AND EXPERIMENT

The proposed model was initially checked against the switching simulation model, which takes the exact same parameters as the model. Magnitude responses obtained from the model and the simulation with different AIM loop parameters are plotted together for comparison in Figure 11 and Figure 12. The agreement between model and simulation

is very good, as long as the comparator delay is significantly larger that the simulation time step size (10ns in all simulations.)

The performance of the extended model is illustrated in the plots shown in Figure 13. It is apparent that the model accuracy is good when D is in the 0.2 to 0.8 range (symmetry is assumed), while the simulated gain is up to 6-8dB higher than the modeled gain for *D=0.9*. The gains at DC and the switching frequency are accurately predicted at all *D* values, however. This strongly indicates that the simple idea of connecting the calculated DC and switching frequency gains with a simple 1st order transfer function is not entirely representative of the true nature of the system – a different (and probably much more complex) approach will be needed for providing the full picture. A relatively firm link between the simulated and measured magnitude responses is established through the *D=0.5* measurement data on the AIM board, so no experimental data for *D≠0.5* has been included.

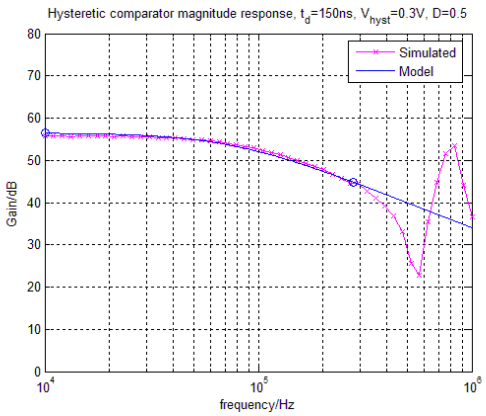

Figure 11. Typical example of modeled and simulated hysteretic comparator behavior. The finite comparator gain at LF is apparent. The model fits the simulated data nicely.

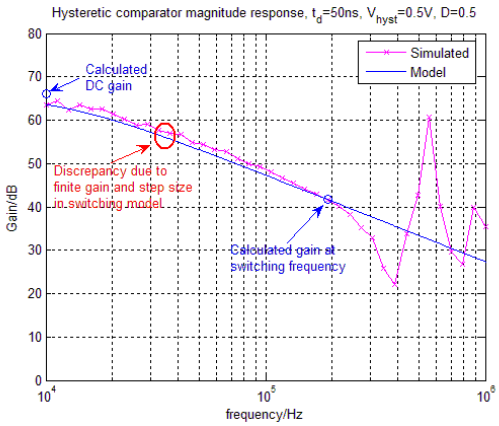

Figure 12. Modeled and simulated hysteretic comparator behavior with low propagation delay. The comparator approaches integrator behavior.

The derived model was also tested against the different experimental hysteretic control loops, results are shown in Figure 14, Figure 16 and Figure 17. It is generally evident that the model can describe the hysteretic comparator very well below the switching frequency, although deviation form the perfectly-linear carrier due to output filter dynamics in the BPCM loop and the dual-filter loop produce unmodeled effects. More detailed carrier signal descriptions would be necessary in these cases, but this would also produce DC gain expressions of much higher complexity, shrouding the basic message that time delay limits DC gain.

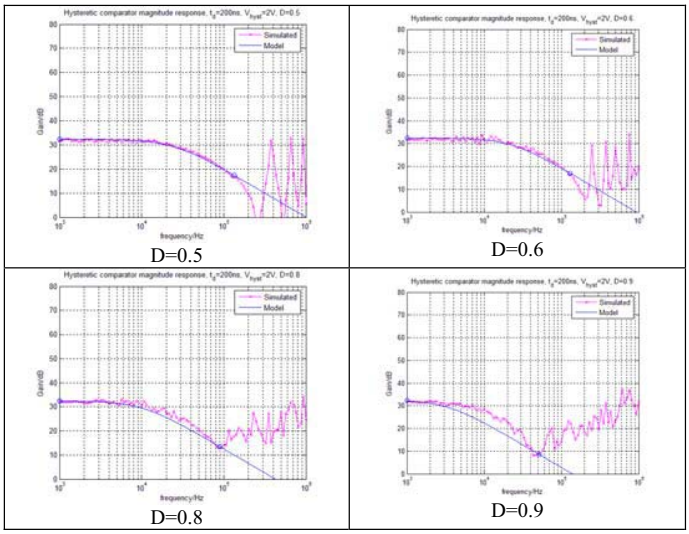

Figure 13 Modeled and simulated hysteretic comparator magnitude responses with varying duty cycle. The shortfall of the 1st order approximation model at high *D* is apparent.

The difference between the gain of a standard PWM modulator and that of the hysteretic comparator can be quite high; in the BPCM amplifier the DC gain is about 55dB, with a carrier amplitude of around 100mVpp and +/-20V supply, in the standard PWM modulator this would imply 46dBs of gain (given by the supply to carrier voltage ratio [6].) In other words the small-signal behavior of the hysteretic comparator cannot be described using a carrier signal analogy to the standard PWM modulator, as could otherwise be a tempting assumption.

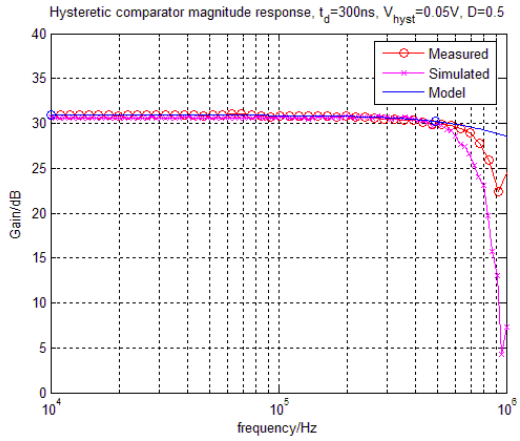

Figure 14. Gain-plot from AIM test board vs. modeled and simulated results. All curves are in good agreement below the switching frequency.

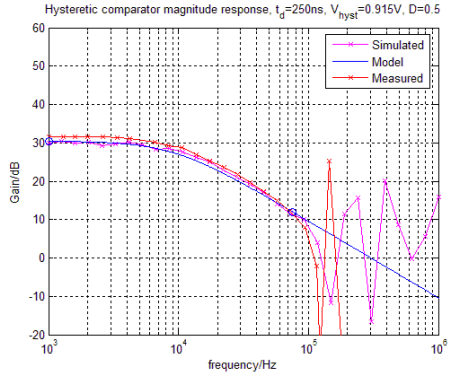

Figure 15. Gain-plot from AIM test board vs. modeled and simulated results with a different parameter set. All curves are still in very good agreement below the switching frequency.

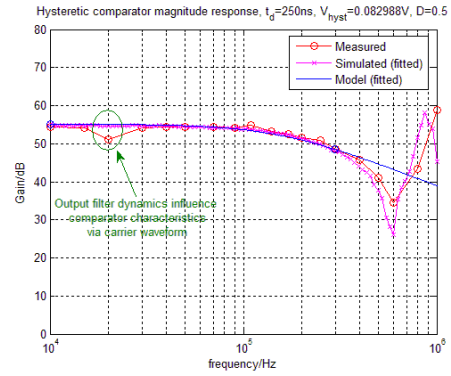

Figure 16. Gain-plot from BPCM amplifier board vs. fitted modeled and simulated results. Agreement is good, except around the output filter corner frequency of the prototype.

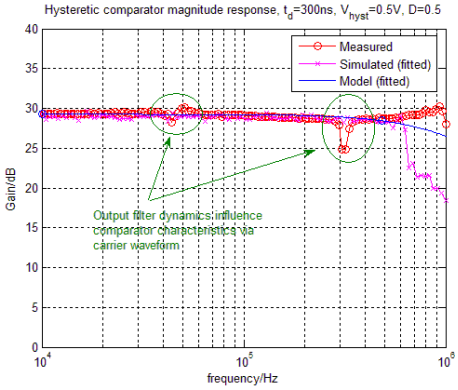

Figure 17. Gain-plot from 500W dual-filter buck converter vs. fitted modeled and simulated results. Agreement is good, except around the output filter corner frequencies of the prototype.

A practical remark to the results obtained from the BPCM amplifier is that its THD+N performance would benefit from reduced comparator/power stage delay through the increase in loop gain below 10kHz, where the gain flattens out. If the delay was reduced by a factor of 2, close to maximum gain would be available at the most critical frequency of 6.67kHz, allowing a better "full audio range" THD+N specification. Any further decrease in delay would simply reduce THD+N at lower frequencies, a welcome, but not nearly as necessary improvement.

CONCLUSION

The world's (probably) first, accurate linear continuous-time model of the hysteretic comparator when operating in an AIM control loop has been presented. The model allows for the co-existence of the "infinite-gain" hysteretic comparator model used for easy control system dynamics prediction and actual measurement data showing far from infinite gain. It has been explained that time delay inherent to all comparators and power stages causes the effective hysteresis window to move with the output duty cycle, reducing the hysteretic comparator small signal gain to less that infinity. The model has been verified against both simulated and measured data with good agreement as long at duty cycle extremities are avoided.

The utility of the model is obvious; by allowing accurate calculation of the loop gain in an important group of self-oscillating control systems, estimation of output impedance and, especially for audio applications, harmonic distortion, becomes possible. Future work will concentrate on demonstrating such utilization of the model as well as theoretically cementing the benefits of self-oscillating controllers over clocked controllers in high-performance applications, certainly a long-overdue task.

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Envelope Tracking Power Supply with fully controlled 4th order Output Filter

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Abstract – This paper describes the derivation of a practical solution to designing a medium-power non-isolated DC/DC power converter with very low output ripple voltage and very high output voltage slew-rate capability. The converter is intended for powering and efficiency-optimizing an RFPA (Radio Frequency Power Amplifier) in a communications system base station. A simple and effective analog control scheme for the converter (buck with 4th order output filter) is developed, along with an accurate linear model. The proposed approach is verified experimentally by a 500W output prototype, capable of greater than 1V/µs slew rate with 40mVpp of output ripple and efficiency above 90%.

I. INTRODUCTION

The use of envelope tracking power supplies for RFPAs (Radio Frequency Power Amplifiers) is an emerging application for high-bandwidth power converters. By intelligently adjusting the RFPA supply voltage in accordance with the RFPA output voltage envelope, substantial efficiency improvements are possible for linear RFPAs operating in class-A. Prior art [1], [2] has demonstrated the approach in low-power systems.

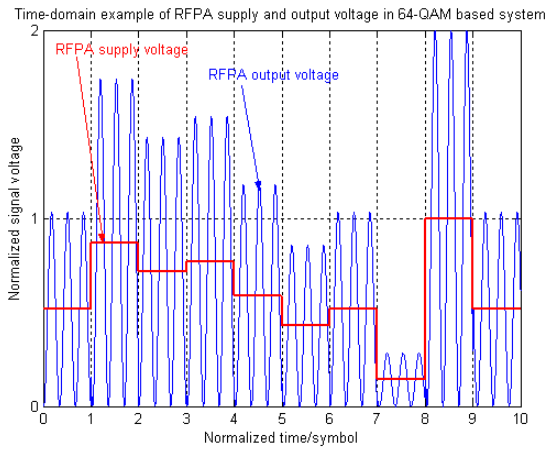

Figure 1 Idealized RFPA output signal and envelope tracking supply voltage for a single-ended class-A RFPA.

Many newer-generation RF communications systems rely on modulation techniques where the transmitted signal amplitude contains information, thus producing fast variations on the output signal envelope. One such modulation technique is QAM[3] (Quadrature Amplitude Modulation), where data bits are represented by a set of combinations of carrier phase and amplitude. The work presented in this paper focuses on how to implement a tracking power supply that is both fast enough for the considered QAM-based system and has minimal output ripple voltage.

II. SYSTEM SPECIFICATIONS

The system considered in this work is a communications network base station, where the RFPA amplifies 64-QAM modulated data with 50kHz bandwidth and at 360W of maximum output power. This leads to a requirement for at least 50kHz of large-signal control bandwidth from the tracking power supply.

The RFPA supply voltage is up to 30VDC, with the bias current at a constant 18A.

The ripple tolerance of the RFPA is unknown – but ripple is known[4] to cause sideband frequency components which are limited by tight specifications.

Therefore low ripple is cautiously specified, initially aiming for the 10-100mVpp range.

Assuming that a 64-QAM transmission system transmits random data, each symbol will be used with equal probability, and the output amplitude distribution will appear as shown in Figure 2.

This simple model yields the output amplitude distribution shown in Figure 2. It is apparent that 9 different amplitude levels exist, and that the signal amplitude on average is 61.5% of the maximum amplitude. It is this less-than-1 peak-to-average ratio that is exploited by using an envelope tracking power supply. The model only describes operation at full RFPA output power– a more complete model would take into account that the average RFPA output power level is adjusted dynamically, according to operating conditions.

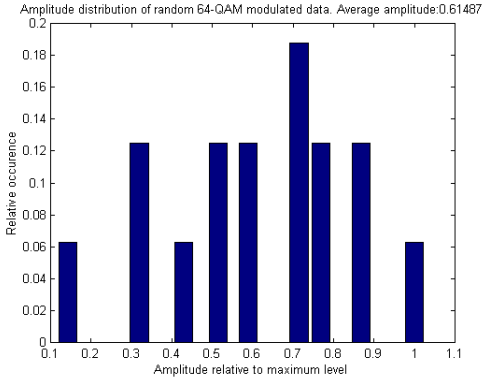

Figure 2 Calculated amplitude distribution of random 64-QAM modulated data at full RFPA output power.

III. TRACKING CONVERTER TOPOLOGY

The synchronous buck topology is selected due to its simple dynamics and symmetrical slew-rate capability. The requirement for >50kHz control bandwidth suggests the use of a switching frequency in excess of 5*50kHz=250kHz [5].

The output filter cut-off frequency should be 50kHz or more to allow 50kHz of large-signal control bandwidth.
Disregarding higher harmonics in a D=0.5 PWM signal, the output ripple voltage from the 2nd order output filter can be approximated as:

$$\Delta V_{out,pp} \approx \frac{4}{\pi} \frac{V_{PWM,pp} \cdot f_{filter}^2}{f_{sw}^2}$$

Where $V_{PWM,pp}$ is the peak-peak amplitude of the PWM signal, f_{sw} is the switching frequency and f_{filter} is the output filter cutoff frequency.
Solving for f_{sw} yields:

$$f_{sw} \approx f_{filter} \sqrt{\frac{4}{\pi} \frac{V_{PWM,pp}}{\Delta V_{out,pp}}}$$

It follows that 40mVpp of ripple requires a switching frequency of around 1.8MHz, given a 50kHz filter and an input voltage of 40V. This is clearly way beyond what is required for adequate dynamic performance and certainly what is optimal for efficiency.
One solution for reducing the switching frequency while maintaining low ripple is higher-order filtering, implemented by a second LC filter on the buck converter.

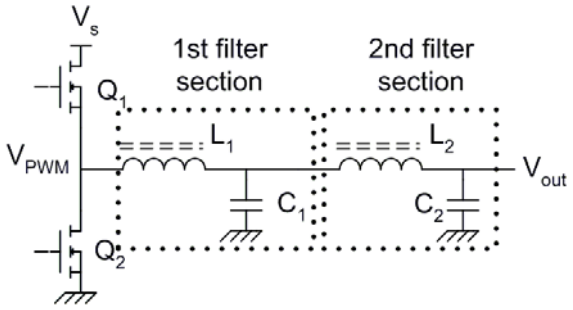

Figure 3 Buck converter with 4th order output filter.

Finding and implementing a practical, low-cost design solution to controlling the buck converter with 4th order output filter is the focus of the work presented here.

VI. LINEAR MODEL OF POWER CONVERTER

In order to understand the dynamics of the buck converter with 4th order filtering, a linear model of the system has been developed, for numerical use in MATLAB. The use of hysteretic control is assumed, whereby the transfer function from hysteretic comparator input to PWM output can simply be modelled as an infinite gain[6]. Very low-ESR output capacitors (such as ceramic or polypropylene caps) are assumed, which moves ESR-capacitance zeros outside the frequency range of interest.
The 4th order output filter is described in SIMULINK as shown in Figure 4, this model forms the basis of the control system design procedure used.

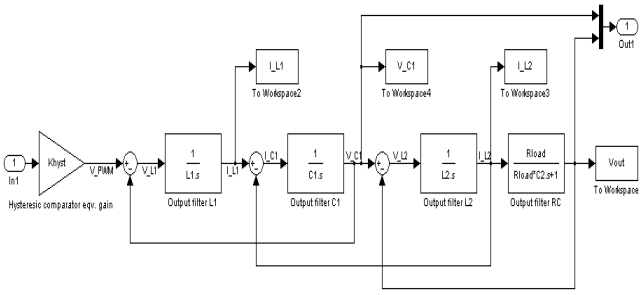

Figure 4 SIMULINK model of hysteretic comparator, buck switching stage and 4th order LC output filter.

V. CONTROL SYSTEM IMPLEMENTATION

In order to provide a flexible control solution, compatible with existing integrated control circuits, only a single operational amplifier is allowed in the control circuit. For a standard buck converter, this is no problem, with excellent implementations possible, such as the PID[7],[8] control implementation shown in Figure 5, which forms the basis for further discussion presented here.
The controller shown in Figure 5 has poles and zeros at the following frequencies:

$$f_{pole,PI} = 0$$

$$f_{zero,PI} = \frac{1}{2\pi R_{PI} C_{PI}}$$

$$f_{zero,D} = \frac{1}{2\pi R_D C_D}$$

In this implementation, the 2 controller zeros can be used to partially cancel the output filter poles while the integral term provides the necessary loop gain and HF roll-off.

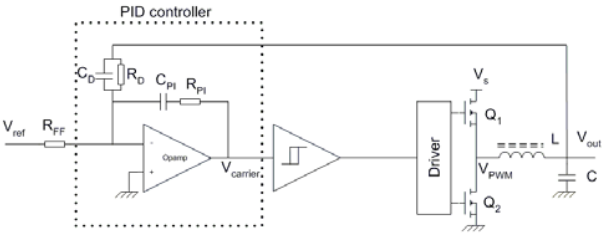

Figure 5 PID voltage mode hysteretic controller for a buck converter[8].

When adding an extra output filter section, attention must be paid to the damping of the second filter section, which varies with load impedance. In the case considered, the RFPA can be modelled as a current sink, with near-infinite impedance. Thus, the second output filter will ideally have an infinite Q with the intended load impedance, which will ruin the converter transient response if not taken care of. Two fundamental approaches to controlling the output filter Q exist:

- Passive damping via a dissipative device
- Active damping via the control system

In the application considered, the inductor currents are nearly constant, so during an output voltage step, it is mainly the filter

capacitor energy that is changed. If a dissipative damping device is used, the energy removed from the capacitor during a negative voltage step will be lost in the damping device, an equal amount of energy will also be lost during a positive step:

$$P_{damp} = f_{step} \cdot C_2 \left(V_{top}^2 - V_{bot}^2 \right)$$

Assuming a 50kHz square output stepping between 20V and 30V and C_2=470nF, the power dissipated will be nearly 12W, which would have to be dissipated in a sizeable power resistor. This power dissipation directly reduces the converter efficiency by more than 2 percentage points, and this would be even more pronounced in a lower-current application. Therefore, for the sake of efficiency and versatility, an inexpensive active damping solution is sought.

Since the one opamp allowed for the design is already assigned, the only solution available is to add a feedback path from the second output filter. By using a parallel RC network as shown in Figure 6, an open-loop zero is added, which can be used to reduce open-loop phase lag and thereby improve closed-loop stability. The zero introduced effectively makes the outer control loop a PD (proportional-differential) loop.
Demonstrating the effectiveness of this particular approach is one of the key aims of this paper.

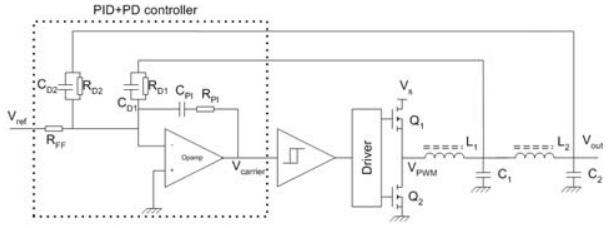

Figure 6 Inner PID + outer PD voltage mode hysteretic controller for a buck converter with 4th order output filter.

A disadvantage with the controller implementations shown in Figure 5 and Figure 6 is that both have inverting inputs, so that the reference voltage is inverted on the output. This is presumed to be amendable by moving the reference signal injection point to the opamp non-inverting input. This will be shown to affect the closed loop transfer function, but not more than can be corrected using a simple RC input filter as shown in Figure 7. Additionally, resistor R_{FB} is added to provide control over the controller closed-loop gain.

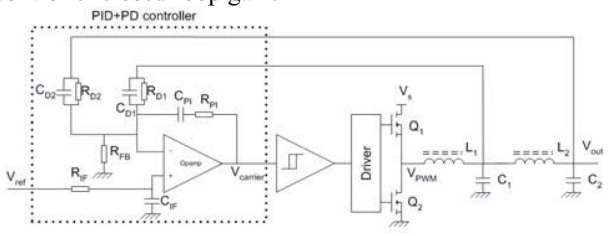

Figure 7 Proposed PID+PD controller implementation with non-inverting reference input.

An additional issue that needs to be considered is the effect of the switching frequency variation inherent to most hysteretic controllers on output voltage ripple. Since the 4th order output filter has a stopband attenuation of 24dB/octave, any reduction of the switching frequency will seriously increase the ripple voltage. To defeat this mechanism, a switching frequency control loop is implemented around the hysteretic comparator, as shown in Figure 8. The basic idea is that an MMV (Monostable MultiVibrator or one-shot) provides frequency-to-voltage conversion, which forms the basis for a simple integrating control loop, where the error output from the integrator is phase-split into a hysteresis window.
The small-signal analysis and design details of this control loop are unfortunately beyond the scope of this paper.
The effect of delay on the switching frequency control loop, however, needs to be considered for the presented experimental data to make sense.

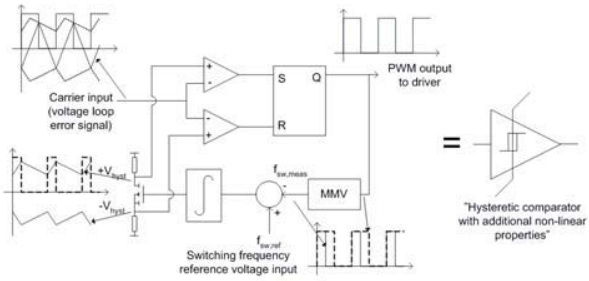

Figure 8 Principal illustration of the constant-switching-frequency hysteretic comparator used in the prototype.

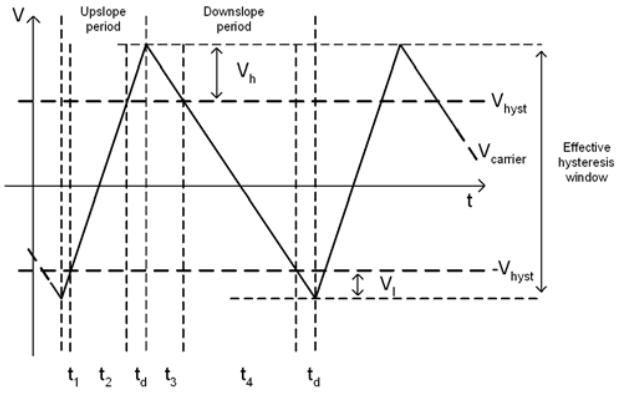

Figure 9 Carrier signal and effective hysteresis window in a system with delay. The propagation delay (t_d) increases the hysteresis window and adds a displacement from the intended symmetry point.

By dividing a period of the carrier waveform into segments as shown in Figure 9, the following expression for the switching frequency of the hysteretic controller is found:

$$f_{sw} = \frac{D(1-D)}{2\left[\frac{V_{hyst}}{K} + t_d\left(1 + \frac{(1-D)^2}{2} + \frac{D^2}{2}\right)\right]}$$

where K wraps up a number of constants and D is the converter duty cycle. The key point to note here is that even if the hysteresis window can be controlled, the time delay will always contribute to reducing the switching frequency, and it ultimately sets the limit for the maximum switching frequency of the control loop.

VI. CONTROL SYSTEM DESIGN

The control system design is initially performed on a model of the system shown in Figure 6 due to the simplicity of calculating controller transfer functions.

The inner control loop presumably has to be significantly faster than the second filter stage dynamics if proper damping is to be achieved. In the design shown, the 2nd filter stage has a cutoff frequency equal to the required bandwidth (50kHz) to make small-signal bandwidth equal to power bandwidth at minimum output ripple. The 1st filter stage is made significantly faster (cutoff at 275kHz), providing sufficient power bandwidth from the inner control loop to allow effective control of the 2nd filter stage.

The zeros of the PID controller are as the only significant compensator parameters placed right near the output filter cut-off frequency. The proportional gain of the compensator is irrelevant to system dynamics since the hysteretic comparator that follows has high gain.

Using this technique, the closed-loop step response of the converter will appear as shown in Figure 10.

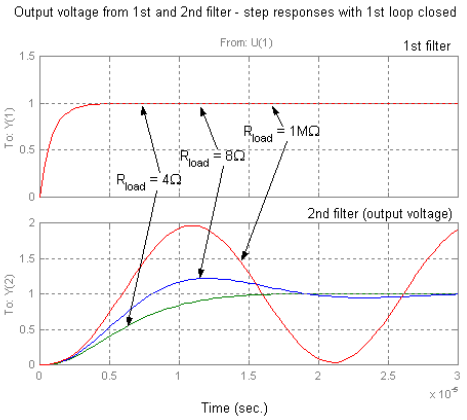

Figure 10 Calculated step responses with 1st control loop (PID) closed. Fast and well-damped response of inner loop is evident.

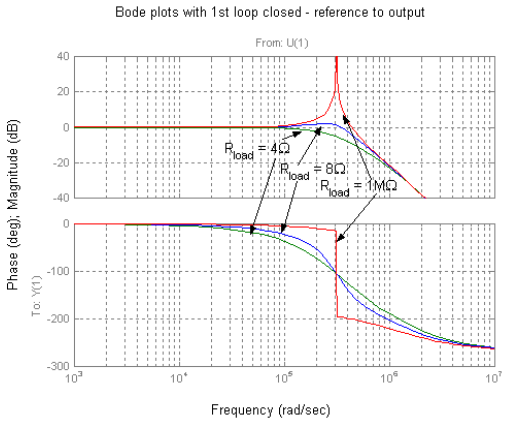

Figure 11 Bode plot from reference to output - 1st loop (PID) closed. Extremely poor stability margins for uncompensated 2nd loop are evident.

It is apparent that the inner loop is very well-behaved at all loads and that the 2nd filter needs damping. Looking at this problem from a frequency-domain perspective (Figure 11) it is apparent that a positive phase boost is required to stabilize the 2nd loop with a meaningful loop gain.

Positive phase boost is neatly achieved with the proposed implementation by placing the zero of the PD compensator close to the 2nd output filter section cut-off frequency, leading to the open-loop bode plot in Figure 12 and the closed-loop step response shown in Figure 13. The LF loop gain is unity, but the resonant action of the undamped filter as well as the introduced zero provides the HF loop gain required for effective damping.

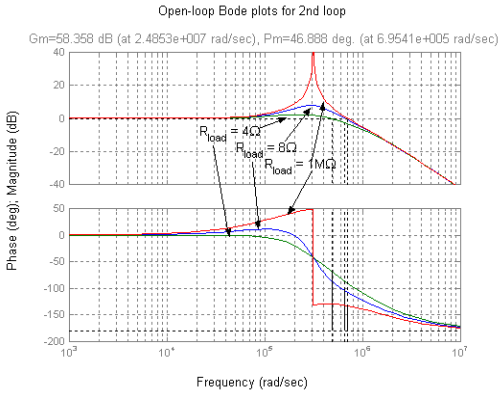

Figure 12 Open-loop bode plot for outer (PD) loop. Compensation zero provides good stability margins (Phase margin is 46.9°.)

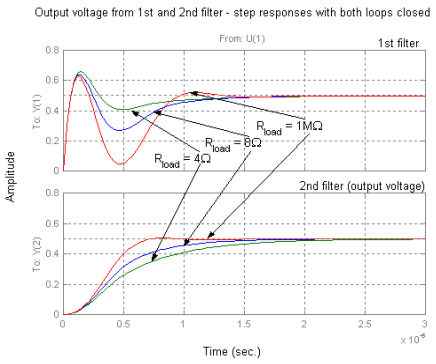

Figure 13 Step responses with both loops closed. Effective damping of 2nd filter section is evident.

When moving the reference injection point, the controller open-loop transfer functions will still be the same, while the closed-loop transfer function may change. Therefore, the closed-loop transfer function of the designed controller must be calculated from scratch when migrating to the proposed solution shown in Figure 7.

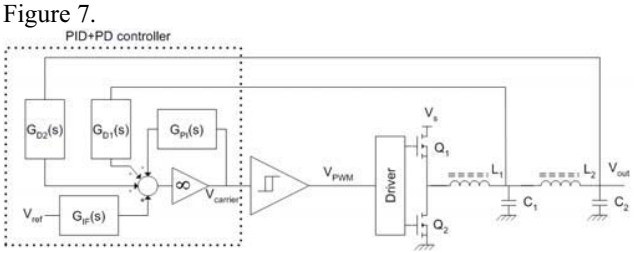

Figure 14 Definition of critical blocks when finding closed-loop transfer function for the proposed controller

The following expressions are found:

$$G_{PI}(s) = \frac{s(R_{FB} \parallel R_{D1} \parallel R_{D2})C_{PI}}{1 + s \cdot k_{PI,Den1} + s^2 \cdot k_{PI,Den2}}$$

$$G_{D1}(s) = \frac{R_{D1} \parallel R_{D2}}{(R_{D1} \parallel R_{D2}) + R_{PI}} \cdot \frac{1 + s(R_{PI}C_{PI} + R_{D1}C_{D1}) + s^2(R_{PI}R_{D1}C_{PI}C_{D1})}{1 + s \cdot k_{D1,Den1} + s^2 \cdot k_{D1,Den2}}$$

$$G_{D2}(s) = \frac{R_{D1} \parallel R_{D2}}{(R_{D1} \parallel R_{D2}) + R_{PI}} \cdot \frac{1 + s(R_{PI}C_{PI} + R_{D2}C_{D2}) + s^2(R_{PI}R_{D2}C_{PI}C_{D2})}{1 + s \cdot k_{D2,Den1} + s^2 \cdot k_{D2,Den2}}$$

$$G_{IF}(s) = \frac{1}{1 + sR_{IF}C_{IF}}$$

Where

$$k_{PI,Den1} = \left((R_{FB} \parallel R_{D1} \parallel R_{D2})(C_{D1} + C_{D2} + C_{PI}) + R_{PI}C_{PI}\right)$$

$$k_{PI,Den2} = R_{PI}(R_{FB} \parallel R_{D1} \parallel R_{D2})C_{PI}(C_{D1} + C_{D2})$$

$$k_{D1,Den1} = \frac{(R_{D2} \parallel R_{FB})R_{PI}C_{PI} + (R_{D2} \parallel R_{FB})R_{D1}(C_{D1} + C_{PI}) + R_{D1}R_{PI}C_{PI}}{(R_{D2} \parallel R_{FB}) + R_{D1}}$$

$$k_{D1,Den2} = \frac{(R_{D2} \parallel R_{FB})R_{PI}R_{D1}\left(C_{PI}C_{D1} + C_{PI}C_{D2}\right)}{(R_{D2} \parallel R_{FB}) + R_{D1}}$$

$$k_{D2,Den1} = \frac{(R_{D1} \parallel R_{FB})R_{PI}C_{PI} + (R_{D1} \parallel R_{FB})R_{D2}(C_{D2} + C_{PI}) + R_{D2}R_{PI}C_{PI}}{(R_{D1} \parallel R_{FB}) + R_{D2}}$$

$$k_{D2,Den2} = \frac{(R_{D1} \parallel R_{FB})R_{PI}R_{D2}\left(C_{PI}C_{D2} + C_{PI}C_{D1}\right)}{(R_{D1} \parallel R_{FB}) + R_{D2}}$$

Which is used together with the power stage and output filter model. Feeding the already found component values and a suitably placed input filter pole into the total model results in the step responses shown in Figure 15.

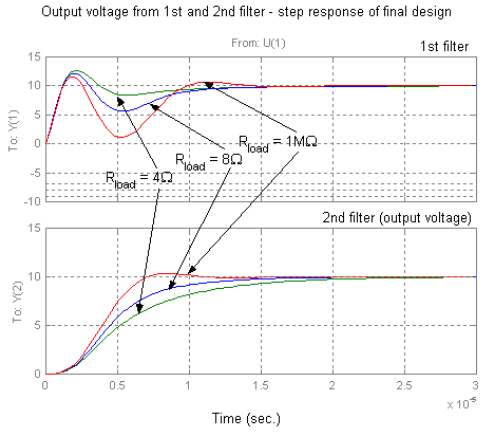

Figure 15 Step responses with proposed control solution. Desired closed-loop response is obtained from the non-inverting reference input.

Table 1 Key prototype design data and suggestions

Parameter description	Parameter name	Parameter value	Suggested design rule
Targeted control bandwidth	BW	50kHz	Choose
Targeted closed-loop gain	A_V	10V/V	Choose
Switching frequency	f_{sw}	700kHz	$f_{sw} > 12 \cdot BW$
1st filter cutoff	f_{c1}	275kHz	$f_{c1} = 5.5 \cdot BW$
2nd filter cutoff	f_{c2}	50kHz	$f_{c2} = BW$
PID lower corner frequency	$f_{zero1,PID}$	159kHz	$f_{zero1,PID} = 3 \cdot BW$
PID upper corner frequency	$f_{zero2,PID}$	188kHz	$f_{zero2,PID} = 3.5 \cdot BW$
PD corner frequency	$f_{zero,PD}$	23kHz	$f_{zero,PD} = 0.45 \cdot BW$
Input filter corner frequency	$f_{pole,IF}$	100kHz	$f_{pole,IF} = 2 \cdot BW$

The design parameters and the values used in the prototype are listed in Table 1 along with a corresponding set of suggested design rules for the considered application.

VII. RESULTS FROM SIMULATION AND EXPERIMENT

The results from the closed-loop model have been verified in a switching simulation, as shown in Figure 16 (top). Good agreement with waveforms found with the linear model is evident. For the sake of comparison, the corresponding measured step response is also shown. Waveforms are still seen to be in good agreement with results from the linear model.

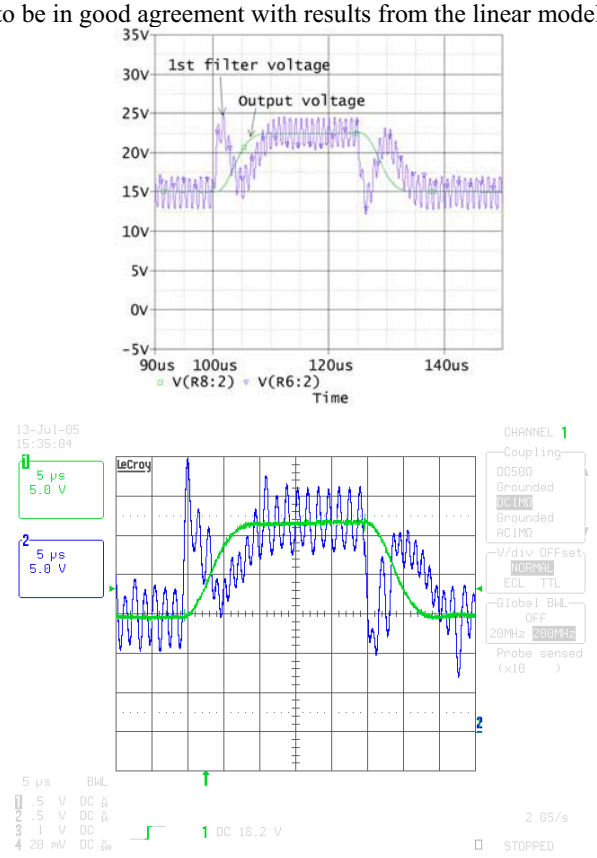

Figure 16 Simulated (top) and measured(bottom) step response (1st filter and 2nd filter output voltages) of prototype with intended (infinite) load impedance.

A prototype envelope tracking power supply has been constructed, using the proposed control scheme and the controller design shown. A picture of the prototype is shown in Figure 17, and key specifications are summed up in Table 2. The prototype uses ground planes extensively, but a modified "hair pin" configuration with less-than-ideal inductance was necessary to make the 4 input-side electrolytics share the considerable input ripple current. A fast 80V half-bridge driver IC provides the gates signals, additional low-inductive pull-down capability has been added using discrete bipolar transistors. A low-permeability iron-powder core has been used for the 1st filter inductor, because the ripple current otherwise results in excessive core loss. Due to the almost-zero ripple current in the 2nd filter inductor, a similarly sized, higher-permeability core is useable. For continuous operation at 500W

output, moderate fan cooling of inductors and input electrolytics was found necessary to stay within temperature ratings.

Table 2 Key prototype specifications

Input voltage	20 – 45V
Output voltage @ 40V input	12 – 28V
Output ripple voltage (p-p)	40mV
Output current	0 – 20A
Efficiency @ 18A output current	80 – 92%
Small-signal control bandwidth	90kHz
Large-signal control bandwidth	50kHz

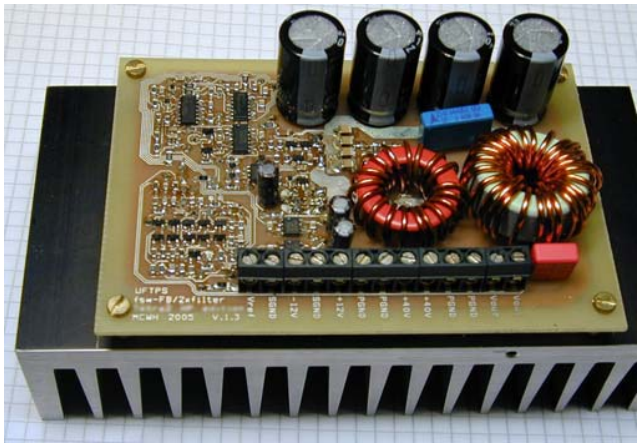

Figure 17 Prototype tracking power supply as implemented on 2-layer PCB. The TO-220 power devices are mounted on the PCB bottom side.

Table 3 Gain-phase measurements on prototype. Blue=gain, red=phase, frequency range 1kHz to 1MHz. Gain range –20 to 60dB, 8dB/div, phase range –180° to 180°, 36°/div.

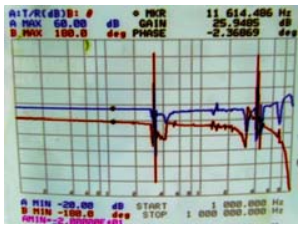

Figure 18 Hysteretic comparator and power stage. Equivalent small-signal gain ≈ 26dB.

Figure 19 Open-loop measurement on inner (PID) control loop. Oscillating frequency ≈ 730kHz.

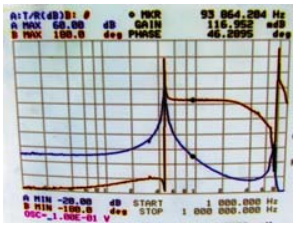

Figure 20 Open-loop measurement on outer (PD) control loop. Phase margin = 46.3°.

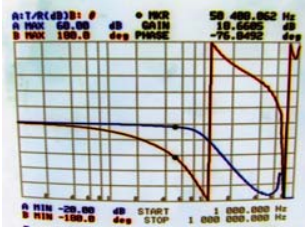

Figure 21 Closed-loop measurement from reference input to output. Bandwidth is well above 50kHz.

The implemented control system has been checked using a gain-phase analyzer, results are shown in Table 3. Open-loop and closed-loop measurements in the outer (PD) control loop correspond well with the linear design model. The measurements made on the inner loop reveals that the hysteretic comparator and power stage in fact has finite (rather than infinite, as assumed) small-signal gain. The model used for the hysteretic comparator is thus principally not very accurate, but it still provides good enough prediction of the loop behavior.

The frequency domain output characteristics of the converter were examined used a spectrum analyzer, results are shown in Table 4. The spectrum of the output from the 1st filter stage indicates the degree of linearity/distortion performance that can be expected from the converter; 3rd harmonic distortion is about 30dB below the fundamental. Depending on the way the RFPA in envelope tracking system is implemented, the inevitable harmonic distortion generated by the tracking power supply may compromise the purity of the RF output spectrum due to unwanted intermodulation products. When the 2nd filter is added, a reduction of harmonics above 50kHz can be expected, as seen in Figure 23. Harmonics below 50kHz will not be attenuated by the 2nd filter; however the loop gain is higher at lower frequencies, and therefore distortion will be lower. The switching process mainly contributes with a single "spur" at 720kHz, higher harmonics are effectively attenuated due to the 24dB/octave slope of the 4th-order filter.
Using a purpose-built 500W variable constant-current load, the converter functionality was verified at 18A of output current. The constant-current load was designed to act as such over a wide frequency range (this is not guaranteed for an off-the-shelf variable electronic load), to avoid adding undesired dynamics to the control system.

Table 4 Spectrum analyzer measurements (1kHz to 10MHz.) on prototype; 50kHz/20Vpp sine + 20VDC output. Magnitude range –90dBm to 10dBm, 10dB/div.

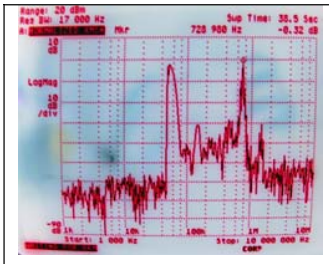

Figure 22 1st filter output voltage; ripple voltage nearly has same magnitude as desired output signal.

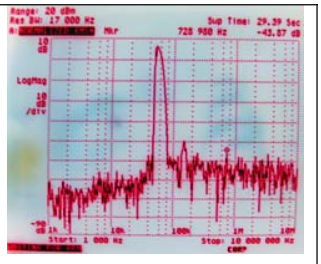

Figure 23 Output voltage; very little ripple remains; a little 3rd harmonic distortion is seen.

The measurement shown in Figure 24 reveals that the converter provides the desired functionality of 20dB gain, less than 10µs total large-signal response time and minimal under/overshoot at 18A output. Changes in the inductor values due to the non-constant permeability of the iron power cores used account for the slight change in the step response compared to the ones shown in Figure 16. The output current is seen to respond slightly to changes in the output voltage, which is due to the

finite small-signal drain-source impedance of the power MOSFETs used to provide the constant-current functionality.

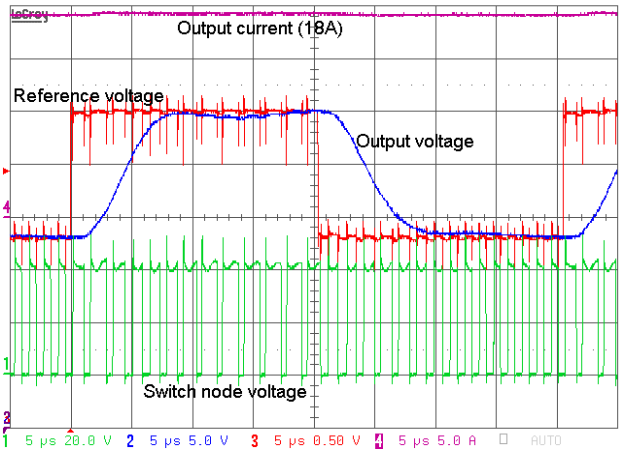

Figure 24 Measured output voltage at 18A output current, stepping between 18V and 30V at 25kHz from a 40V supply. The desired output voltage is reached within 10µs following a reference step.

The efficiency of the prototype is indicated by Figure 25. At high output voltage and low output currents, up to 94% efficiency is achieved. However, efficiency drops to around 80% at low output voltages and 18A output, a direct consequence of having fixed switching and conduction losses (total losses are about 50W at 18A output) for a given output current. The slopes of the efficiency curves indicate that the design is conduction loss dominated at high currents, and there is definitely room for optimization. However, it should

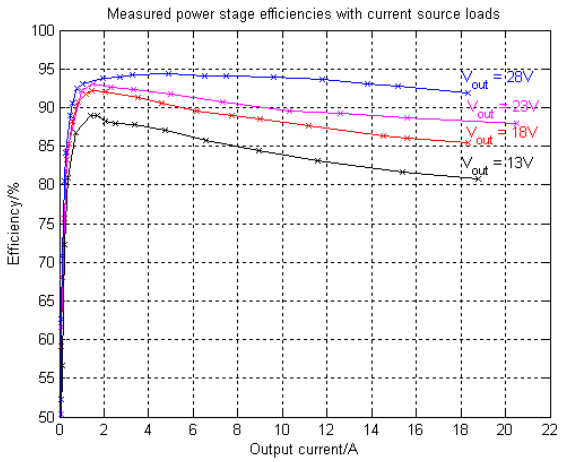

Figure 25 Power stage efficiency figures measured on prototype with constant-current loads at 13, 18, 23 and 28VDC output at 40VDC input.

come as no surprise that the use of 700kHz switching in a 500W converter implemented using a standard power stage costs efficiency.

The effect of using feedback to stabilize the switching frequency can be assessed from Figure 26 and Figure 27. Compared to a standard hysteretic controller (with triangular carrier/error signal), the prototype controller provides constant switching frequency in the area of interest (output between 25% to 75%of input), which is reflected in the ripple performance, which is very good (40mVpp) over a similar range. The reason why the control system fails to keep the switching frequency constant over the entire range is the presence of delay (about 150ns in total), and the switching frequency controller simply saturates at zero hysteresis window leaving the switching frequency to be determined by the time delay alone.

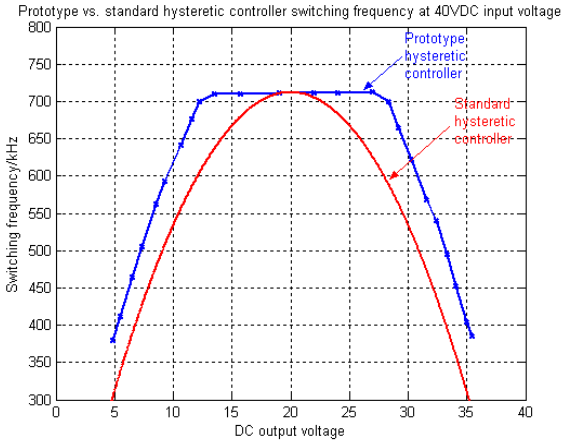

Figure 26 Steady-state switching frequency measured on prototype and with an equivalent standard hysteretic controller.

The adverse effect of reduced switching frequency on ripple is apparent; at 410kHz switching frequency the ripple is increased more than tenfold to about 420mVpp. Stabilizing the switching frequency is, in other words, crucial when higher-order filtering is used to attenuate the switching fundamental. The tested-and-tried fixed-frequency PWM solution does indeed have constant switching frequency, but this comes at the cost of available control bandwidth, which would be unacceptable in this application.

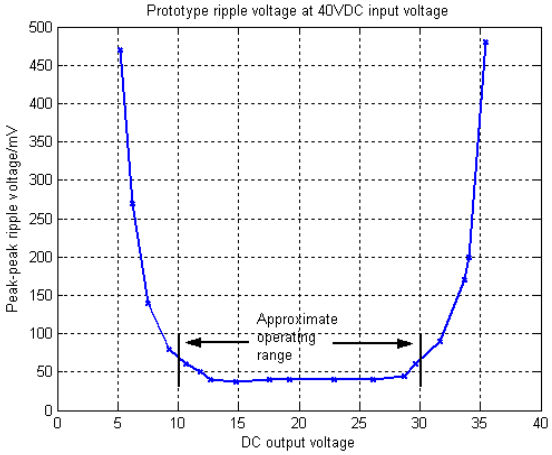

Figure 27 Steady-state ripple voltage (peak-peak) measured on prototype. 40mVpp is achieved over most of the intended operating range.

Finally, the dynamics of the switching frequency control loop are demonstrated in Figure 28. The output voltage is stepped so that the hysteresis window must be changed to maintain the

switching frequency setpoint. This occurs within 20µs, if the output voltage varies faster than this, the control loop will simply try to maintain the correct *average* switching frequency. It is also very evident that the hysteretic controller is close to operating in pure delay-mode since the carrier amplitude exceeds the hysteresis window substantially. When inspecting the carrier signal envelope during the transition, a high similarity is found to shape of the 1st filter stage output voltage (e.g. as in Figure 16). This observation fits well together with the measured finite comparator/power stage gain (Figure 18). Elaborating on this claim, the argument is that since the carrier envelope contains a scaled-down form of the demodulated PWM voltage, the comparator/power stage gain has to be finite since a finite input produces an equally shaped, finite output. In a system without delay (as assumed in [6]) the carrier envelope cannot exceed the hysteresis window, which means that a linear-sloped carrier cannot contain any LF information, again meaning that the hysteresis/power stage gain must be infinite.

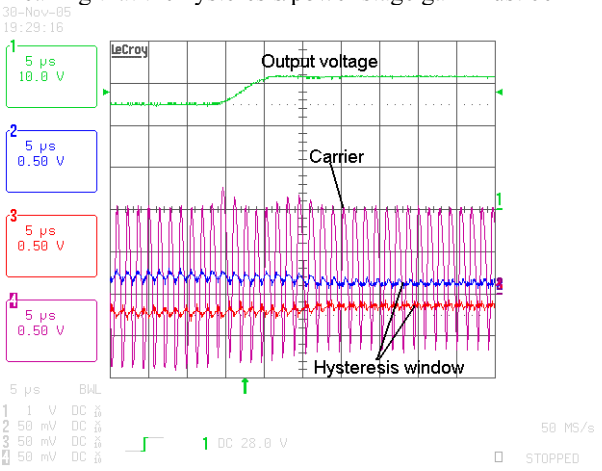

Figure 28 Measured example of carrier and hysteresis window dynamics in prototype. Switching frequency is re-locked in about 20µs following a duty cycle step.

As a final comment, extrapolating from the achieved results by assuming that the product of switching frequency and output power is constant, a 5W-converter switching at 70MHz and achieving 4mVpp ripple and 5MHz control bandwidth from a 4V-supply should be implementable (as an ASIC) at reasonable efficiency. Switching frequencies of 100MHz have actually been reported[9] in this power area, where the target is mobile telephones and other handheld/mobile communications equipment.

IIV. CONCLUSION

A viable solution for providing high slew-rate and low ripple voltage at high efficiency using DC-DC converter techniques has been proposed and experimentally demonstrated. In particular, the effectiveness of the combined usage of constant-frequency hysteretic control and 4th order output filtering has been demonstrated, while keeping controller implantation at a simple level. The constant-frequency hysteretic controller does increase the controller implementation complexity substantially, but this contribution can be largely eliminated in a dedicated control ASIC. An implementation using a standard fixed-frequency PWM IC (if one exists) should be possible due to the simple compensation scheme, albeit at reduced control bandwidth.

The adverse effects on efficiency of using a high switching frequency have been demonstrated, and maintaining high efficiency is an important area for continuing research in high-bandwidth, high-power DC/DC converters. Likewise, reducing the delay of the hysteretic controller and power stage is of major importance for increasing the bandwidth/ripple performance significantly beyond the level presented here. This again points towards an ASIC-based solution, especially in a situation where no commercial hysteretic control ICs cater for the specific demands imposed by ultra-fast power converters at the voltage levels in the 20-50V range.

The proposed control solution effectively gives tracking power supply designers more freedom in the tradeoff between ripple voltage and large-signal bandwidth by extending the available solution space in the direction of lower ripple and moderate control bandwidths for a given switching frequency.

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DERIVATION AND ANALYSIS OF A LOW-COST, HIGH-PERFORMANCE ANALOGUE BPCM CONTROL SCHEME FOR CLASS-D AUDIO POWER AMPLIFIERS

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This paper presents a low-cost analogue control scheme for class-D audio power amplifiers. The scheme is based around bandpass current-mode (BPCM) control, and provides ample stability margins and low distortion over a wide range of operating conditions. Implementation is very simple and does not require the use of operational amplifiers. Small-signal behavior of the controller is accurately predicted, and design is carried out using standard transfer function based linear control methodology. Effectiveness of the approach is demonstrated via a 60W/8Ω single-ended switching amplifier with THD+N of typically 0.02%.

I. INTRODUCTION

Class-D audio power amplifier technology is presently under continuous development, and improved techniques and products appear frequently. Advantage is taken of the very high efficiency (in comparison with linear amplifiers) while inherent problems with distortion and EMI are brought under control through the application of specialist knowledge.

Within the field of self-oscillating analogue control of class-D audio power amplifiers, a lot of high-performance schemes have been demonstrated [1], [2], [3], [4] each with different levels of complexity, distortion, and control loop stability. In comparison with all-digital solutions, the self-oscillating analogue controllers still provide the highest performance since amplifier power stage and output filter non-linearities can be relatively easily compensated for. All-digital solutions, on the other hand, presently need to rely on very accurate PCM-to-PWM converters and power stages, as well as low-distortion output filters, to achieve low distortion.

This paper presents an analogue control scheme that emphasizes simplicity, low cost, and unconditional stability. The approach is based on hysteresis control [5] and bandpass current-mode control [6] and is analyzed and explained from a small-signal point-of-view. The paper furthermore attempts to provide a transparent example of class-D amplifier controller design.

II. BASIC APPROACH

In order to minimize cost of the amplifier, the zobel network normally used to control output filter Q has to be removed. This leaves a potentially undamped output filter, which can be perfectly dealt with using a combination of inductor current and output voltage feedback. The drawback in using current feedback is the requirement for current measurement via a resistive device. This is typically lossy, noisy, and expensive and therefore not suitable for this application. An alternative, where the DC component of the measured current is unimportant, is using current estimation via inductor voltage integration [7], [8]. True integration of the inductor voltage is impossible [7] due to the lack of DC feedback, so integration effectively has to mean low-pass-filtering. This can be done with a single RC filter, which is inarguably a low-cost solution. It is assumed that adding a simple extra winding to a machine-wound inductor will not increase cost noticeably.

Using current estimate feedback and output voltage feedback, the closed-loop system is thus potentially well damped without resistive sensing or filter damping. The use of band-limited current feedback is the logical reason behind the use of the "bandpass current-mode" term.

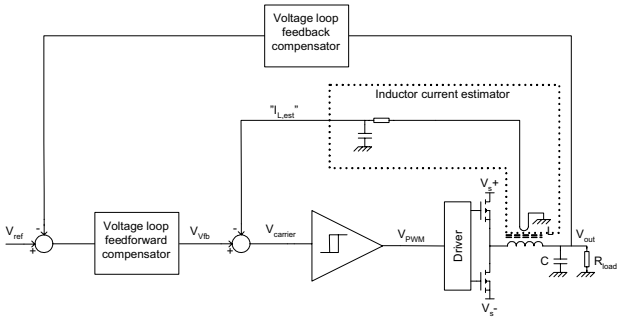

Figure 1 Basic structure of the proposed control scheme

III. DERIVATION OF PROPOSED CONTROL SCHEME

The basic control scheme derived so far is shown in Figure 1, consisting of estimated inductor current feedback and output voltage control via a suitable compensator. The following questions need answers, not in prior art:

- How does the closed BPCM loop behave from a small-signal point-of-view?
- How should the current estimator time constant be chosen?
- What should the voltage loop compensator look like?

The BPCM loop considered is shown in Figure 2.

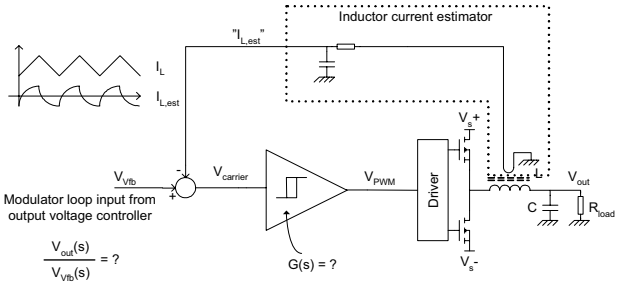

Figure 2 Principal BPCM loop as proposed

The model of the hysteresis comparator/power stage used in [7] has been found to lead to poor matching between expected and measured closed-loop parameters with loop parameters as found in switching amplifiers. The assumption that the hysteresis comparator/power stage behaves as a PWM modulator (as per [9]) thus appears invalid:

$$G(s) = \frac{\langle V_{PWM} \rangle(s)}{\langle V_{carrier} \rangle(s)} \neq \frac{V_s}{V_{carrier,peak}}$$

Being a non-linear component, the hysteresis comparator cannot be straightforwardly converted to a linear model, although methods (such as describing function analysis) do exist. An indirect, argumentative method is used instead to find a suitable small-signal model for the hysteresis comparator, when used in the considered application.

Assuming that a fixed carrier signal is present, offsetting this by an infinitesimal amount will cause the comparator output to go either high or low, since one of the hysteresis limits is no longer reached. It thus appears that the hysteresis comparator small-signal gain is *infinite* while a carrier signal is present (at least at DC) This argumentation is illustrated in Figure 3.

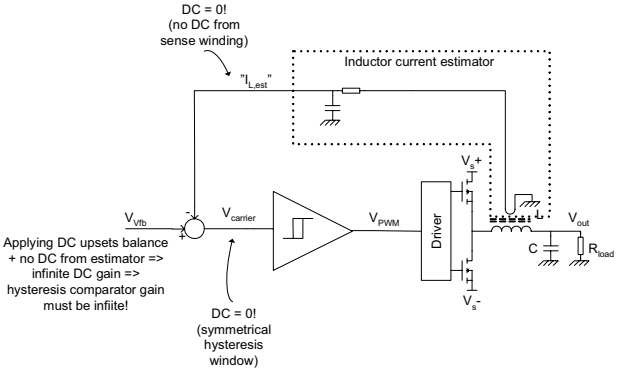

Figure 3 Derivation of hysteresis comparator/power stage small signal model.

Using this knowledge, the BPCM controlled power stage and output filter can be modelled as shown in Figure 4.

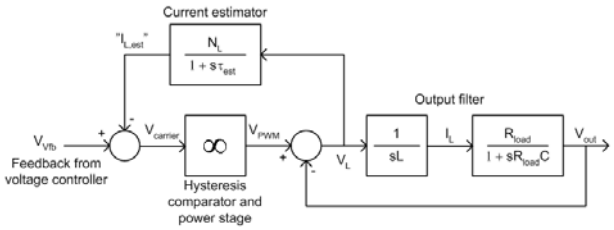

Figure 4 Derived small-signal model of comparator, power stage and output filter with hysteretic BPCM control.

The model shown has the following parameters:

Inductor voltage sense winding ratio	N_L
Current estimator time constant	τ_{est}
Output filter inductance	L
Output filter capacitance	C
Load resistance	R_{load}

The closed-loop transfer function of the BPCM loop can, for any hysteresis comparator small-signal transfer function, *G(s)*, be written as:

$$G_{BPCM,cl}(s) = \frac{V_{out}(s)}{V_{Vfb}(s)}$$

$$G_{BPCM,cl}(s) = \frac{G(s)\cdot(1+s\tau_{est})\cdot R_{load}}{\left(1+s\frac{L}{R_{load}}+s^2CL\right)(1+s\tau_{est})\cdot R_{load} + G(s)\cdot N_L \cdot sL\cdot(1+sR_{load}C)}$$

Assuming that $G(s)=\infty$ (as argued), this reduces to:

$$G_{BPCM,cl}(s) \cong \frac{(1+s\tau_{est})\cdot R_{load}}{N_L \cdot sL\cdot(1+sR_{load}C)}$$

A number of useful observations can be made:

- $G_{BPCM,cl}(s)$ only has real poles/zeros (i.e. output filter Q is a non-issue)
- $G_{BPCM,cl}(s)$ can be turned into an integrator by choosing $\tau_{est}=R_{load}C_{out}$ (pole-zero cancellation)
- Switching frequency has no impact on closed-loop behaviour of the BPCM loop.

By choosing components so that $\tau_{est}=R_{load}C_{out}$, voltage loop compensation can be minimal, relying only on gain blocks.
By providing enough raw gain from the closed BPCM loop, these gain blocks can implemented as resistive attenuators, with associated low cost and simplicity, as shown in Figure 5.
Well-behaved closed loop amplifier response is also ensured in this way, since the system effectively only contains a single pole. The impact of load (R_{load}) variation on closed-loop behaviour is assumed to be manageable.
Figure 6 shows the small-signal model of the proposed

controller, while shows a low-cost implementation.

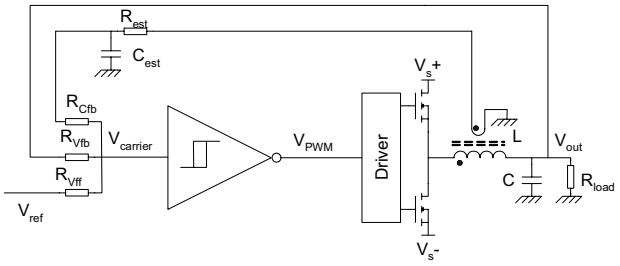

Figure 5 Low-cost implementation of proposed controller

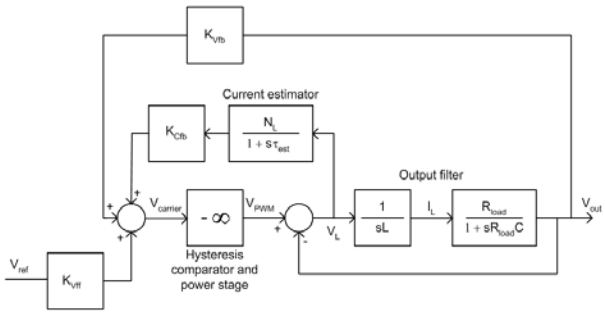

Figure 6 Small-signal model of proposed controller

The BPCM loop transfer function is affected by the introduction of K_{Cfb}:

$$G_{BPCMcl}(s) \cong \frac{(1+s\tau_{est})\cdot R_{load}}{K_{Cfb}\cdot N_L \cdot sL\cdot(1+sR_{load}C)}$$

This model forms the basis for all further linear modelling work presented in this paper.

Assuming that source impedance, amplifier output impedance and current estimator output impedances are small, the following expressions for controller gains K_{Cfb} K_{Vfb}, K_{Vff} will apply:

$$K_{Cfb} = \frac{R_{Vfb} \parallel R_{Vff}}{(R_{Vfb} \parallel R_{Vff}) + R_{Cfb}}$$

$$K_{Vfb} = \frac{R_{Cfb} \parallel R_{Vff}}{(R_{Cfb} \parallel R_{Vff}) + R_{Vfb}}$$

$$K_{Vfb} = \frac{R_{Vfb} \parallel R_{Cfb}}{(R_{Vfb} \parallel R_{Cfb}) + R_{Vff}}$$

The amplifier closed-loop gain A_V, assuming the above as well as sufficient open-loop voltage-loop gain, is simply:

$$A_V \cong -\frac{R_{Vfb}}{R_{Vff}}$$

As would also apply for a standard inverting opamp-based amplifier. The current estimator time constant τ_{est} is finally, assuming that $R_{Cfb} >> R_{est}$, given by

$$\tau_{est} = R_{est} C_{est}$$

This model forms the basis for all further linear modelling work presented in this paper.

Selection of gains and estimator time constant is constrained by non-linear phenomena in addition to standard bandwidth/gain requirements, as will be discussed in the following.

IV. PROTOTYPE DESIGN

The effectiveness of the proposed control scheme is best illustrated in a design with a relatively low (by class-D amplifier standards) output filter cutoff frequency. The output filter cutoff frequency is set at 35.3kHz, which coincides with convenient filter component values. These values, along with other relevant design parameters, are listed in the following table.

Output filter inductance	L	20.25µH
Inductor voltage sense winding ratio	N_L	2:9 ≈ 0.22
Output filter capacitance	C	1µF
Nominal load resistance	$R_{load,nom}$	4.7Ω
Closed-loop gain	A_v	20dB
Supply voltage	+/-V_s	+/-40V
Idle switching frequency	$f_{sw,idle}$	300kHz

The nominal load resistance is set to allow convenient selection of current estimator components in order to achieve $\tau_{est}=R_{load}C_{out}$, leading to $R_{est}=100\Omega$, $C_{est}=47nF$. These values also ensure a relatively low output impedance of the estimator, as required with this realization.

The modelled BPCM closed-loop transfer function with these values is shown in Figure 7. The closed loop clearly behaves as an integrator at a load resistance slightly above 4Ω, as it should. It can also be noted that, provided that enough voltage loop open-loop gain is provided, voltage loop stability margins will be excellent at all loads within the considered range.

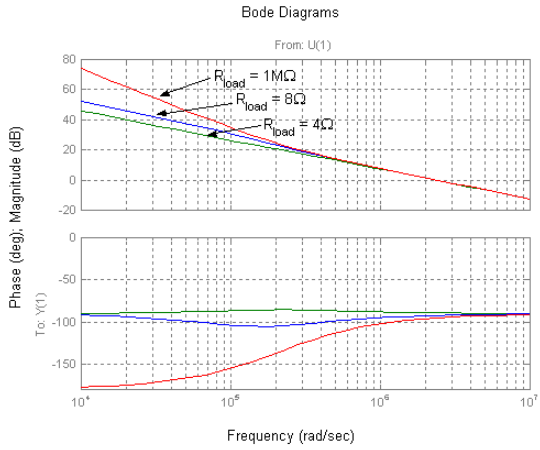

Figure 7 BPCM loop closed-loop frequency responses for varying load resistances

Determining the actual voltage loop gain constants is a matter that requires attention to *carrier distortion* [1], [2]. The idea presented in [1] is that the modulation process achieves maximum linearity when the produced carrier is perfectly triangular. In this system, the carrier composed of components from the inner (BPCM) control loop and the outer (voltage) control loop.

Balancing of current estimator and voltage loop feedback gains, while achieving the desired switching frequency can be straightforwardly achieved through iterative simulation work.

For the considered design example, relevant simulation waveforms are shown in Figure 8.

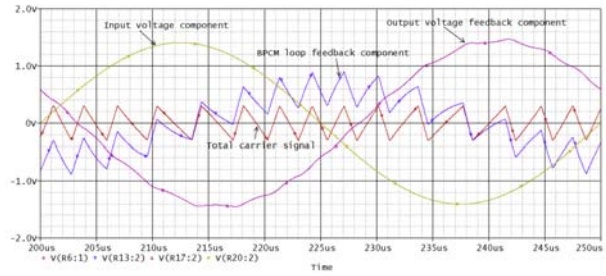

Figure 8 Simulated, optimized carrier signal and its subcomponents in prototype amplifier design. Amplifier producing 20kHz sinewave output at M=0.75 with 8Ω load.

The complete set of component values found for the design is shown in the following table:

R_{est}	100Ω
C_{est}	47nF
R_{cfb}	2kΩ
R_{Vfb}	10kΩ
R_{Vff}	1kΩ

The resulting open-loop and closed-loop frequency characteristics are shown in Figure 9 and Figure 10. With the controller gains as forced by carrier linearity considerations, closed-loop –3dB cutoff is around 20kHz with 4Ω load, while the worst-case phase margin is close to 45° when the amplifier is unloaded. Amplifier bandwidth is thus adequate for audio, while stability is unconditional.

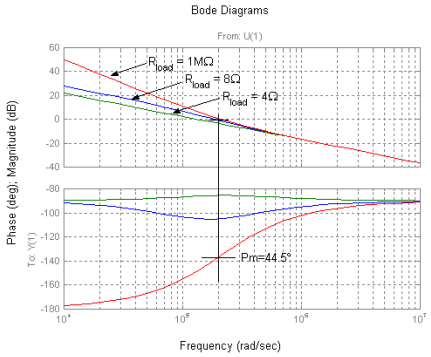

Figure 9 Open-loop Bode plots for prototype amplifier design, showing worst-case phase margin

The step response of the closed-loop linear model with all its assumptions is shown in Figure 11. This can be directly

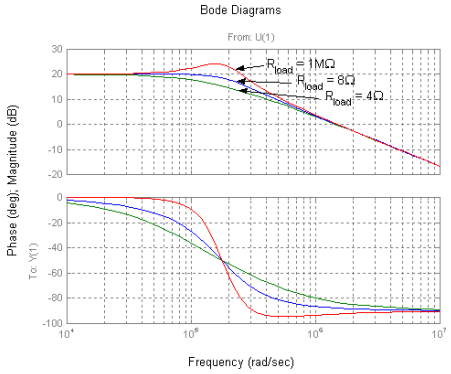

Figure 10 Closed-loop Bode plots of prototype amplifier design

compared to the simulated step responses where the simulation model corresponds to Figure 5. Results are in good agreement indicating that the small-signal model used has sufficient accuracy for dynamic behaviour prediction. An entirely different matter is BPCM loop error suppression capability (i.e. as found by calculating the loop sensitivity function), which realistically cannot be infinite, which logically results from having an infinite gain inside the loop. BPCM loop oscillation can likewise not be explained using the presented model.

Linear modelling of the hysteresis comparator is in other words *not* an outdebated (if at all debated?) topic.

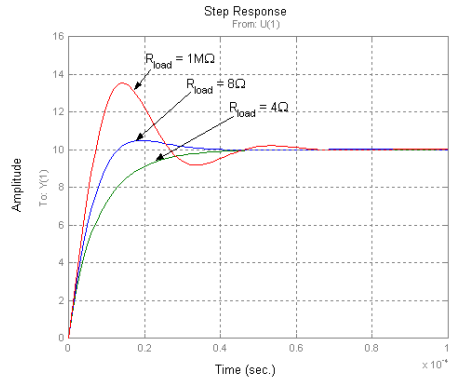

Figure 11 Step-responses of prototype amplifier design as predicted by linear modeling

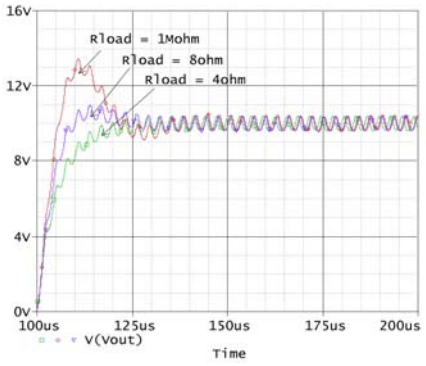

Figure 12 Simulated step responses of prototype amplifier design

VI. ACHIEVED PRACTICAL RESULTS

A prototype amplifier has been constructed on a 2-layer PCB with single-side component placement, as shown in Figure 13. The relatively large number of components is due to the fact that the PCB has provisions for the implementation of more complex control schemes.

Figure 13 The prototype amplifier in its test bench

To conclude the investigation of dynamic response modeling, the measured step response corresponding to the modeled and simulated step responses is shown in Figure 14. This result is in good agreement with the already predicted responses. The easiest comparison to make is between no-load overshoot, which is measured to about 32%, simulated to about 29%, and modeled to about 35%. The deviation between simulated and measured switching frequency (and thus, ripple voltage) is due to the absence of comparator/power stage delays in the simulation model.

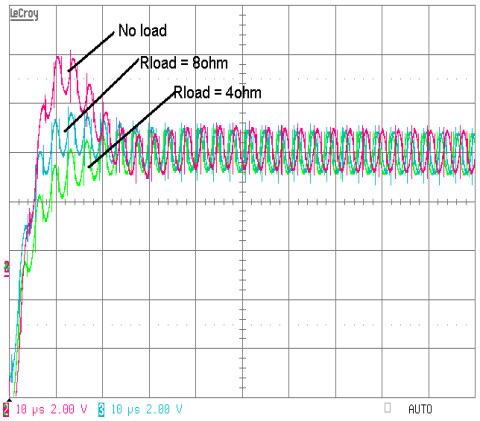

Figure 14 Measured step response of prototype – 2V/div and 10µs/div

Distortion performance is indicated by the THD+N measurements shown in Figure 15 and Figure 16. Although not state-of-the-art [1], [3], the results are very reasonable, and THD+N stays around 0.02% within the area of operation. Signal frequencies are chosen to allow direct comparison with other published results, e.g. [1]. Worth noting is the fact that THD+N is not worse at 6.67kHz than at 1kHz which is the case for certain other control schemes. Additionally, low distortion is achieved with modest voltage loop gain, as indicated by the relatively low closed-loop bandwidth.

Clipping with 4Ω load occurs at lower power than otherwise expected, this is due to current limiting in the power supplies used.

Since power stage/comparator chain implementation generally contributes significantly to the overall THD+N performance of a class-D amplifier, details are given in the following table as a reference:

Total delay (approx.)	160ns
Dead time (approx.)	50ns
Driver	HIP2100 (Intersil)
MOSFETs	FDD3672 (Fairchild)
Gate resistance	Minimal (only parasitics)

The results presented have in other words been achieved using a standard, average-performance power stage/comparator chain (relative to integrated power stages, such as those provided by TI). THD+N performance of the prototype shows significant sensitivity to variation in negative power stage supply

decoupling, indicating that higher performance is possible by circuitry improvements.

The relatively long dead time used results in little power stage shoot-through and low idle losses. The case temperature of the TO-252 packaged MOSFETs settles at around 30°C above ambient during idle operation, corresponding to total idle losses in the MOSFETs of around 1W.

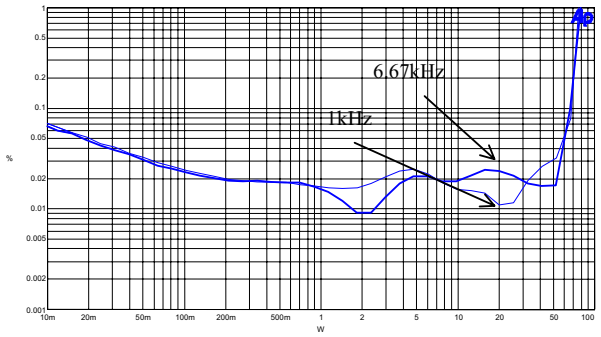

Figure 15 THD+N ratio of prototype amplifier with 8Ω load at 1kHz and 6.67kHz, 80kHz measurement bandwidth

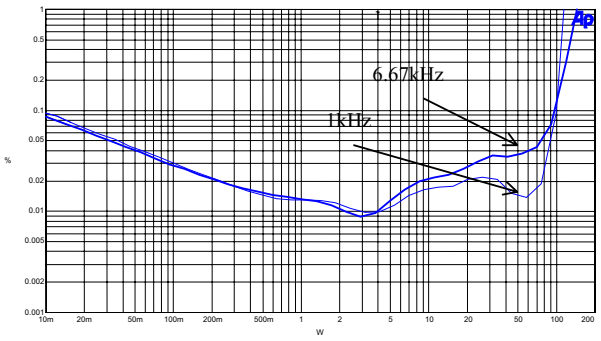

Figure 16 THD+N ratio of prototype amplifier with 4Ω load at 1kHz and 6.67kHz, 80kHz measurement bandwidth

The measured frequency response of the amplifier is shown in Figure 17, and a zoom of the predicted response is shown in Figure 18 for easy comparison. For 4Ω and 8Ω, results are in good agreement with the linear model whereas peaking is less than expected with open load. Output capacitor losses and/or modelling inaccuracies are probable causes. Output capacitor losses will especially cause increased removal of energy from the output filter LC circuit, thereby decreasing its Q.

The deviation of mid-band gain of about –0.7dB is partially due to generator output impedance and input buffering (accounts for –0.26dB), the remaining –0.44dB are almost within limits set by 1% resistor tolerance (+/-0.35dB).

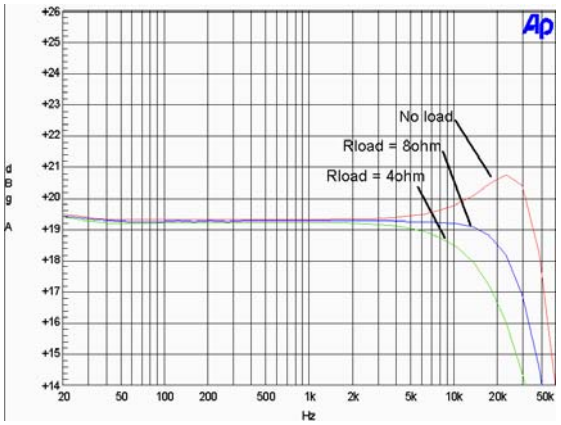

Figure 17 Frequency response of prototype amplifier at V_{out}=10V_{peak} into 4Ω, 8Ω and open load, >500kHz measurement bandwidth.

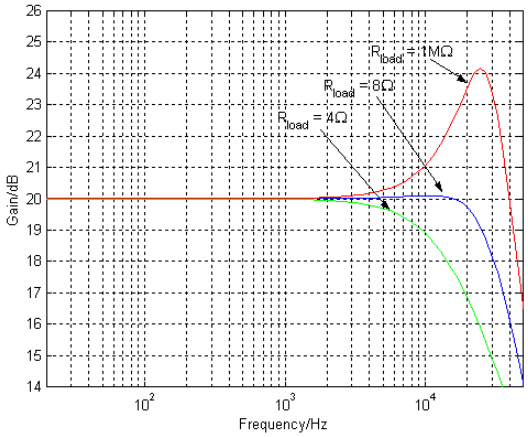

Figure 18 Predicted frequency response of prototype amplifier (zoom of Figure 10, top)

VII. CONCLUSION

This paper has presented a small-signal model of a self-oscillating control loop, which allows accurate prediction of the dynamic behaviour of the complete amplifier. This tool can be used as a supplement to simulation, especially for troubleshooting during the control system design process. The small-signal model also allows overall design rules to be firmly established.

Used in combination with prior art, the small-signal model based method has been demonstrated capability to lead to well functioning, predictable amplifier designs.

The proposed BPCM based control scheme places itself in the low-cost, high-performance category among amongst analogue, self-oscillating control systems for buck-type converters.

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High-Bandwidth, High-Efficiency Envelope Tracking Power Supply for 40W RF Power Amplifier Using Paralleled Bandpass Current Sources

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Abstract - This paper presents a high-performance power conversion scheme for power supply applications that require very high output voltage slew rates (dV/dt). The concept is to parallel 2 switching bandpass current sources, each optimized for its passband frequency space and the expected load current. The principle is demonstrated with a power supply, designed for supplying a 40W linear RF power amplifier for efficient amplification of a 16-QAM modulated data stream.

I. INTRODUCTION

Power conversion through paralleled converters is useful when an application calls for higher performance than can be achieved with a single converter. Examples are the combination of a buck converter and a linear power stage where improved load step performance is required in a DC-DC converter [1] and the combination of a class-D and a linear power stage for audio amplification with both high efficiency and low distortion [2]. In both these applications, the linear power stage supplies very little average power.

The combination of 2 or more identical switching converters is frequently seen in form of the multi-phase buck converters used for microprocessor power supplies.

In applications where both significant DC and high-frequency AC currents must be supplied, exchanging the fast, linear converter used in [1] with a high-bandwidth switching converter offers an opportunity for increasing efficiency, since a switching converter is substantially more efficient than a linear converter at high load currents.

An emerging application for DC+AC supplies is envelope tracking power supplies for RFPAs (Radio Frequency Power Amplifiers), where QAM (Quadrature Amplitude Modulation) is used.

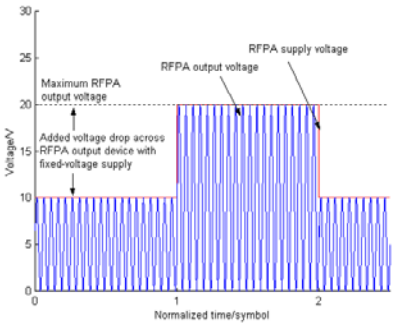

Figure 1 Idealized example of envelope tracking supply voltage for an RFPA for 16-QAM signal amplification.

The concept of using an envelope tracking power supply for an RFPA has been well known for a number of decades [3]. The basic idea is to maximize the efficiency of a linear RFPA by supplying only the minimum necessary supply voltage an any given time, as illustrated in Figure 1. Recently, the use of switch-mode techniques [4], [5] has resulted in small and efficient envelope tracking power supplies for low-power QPSK (Quadrature Phase Shift Keying) cellular mobile telephony applications.

The increasing use of QAM over QPSK, to increase bandwidth efficiency potentially imposes higher demands on power supply output voltage slew-rate (dV/dt) due to fundamental differences between these modulation schemes. The UMTS (Universal Mobile Telecommunications System) standard for next-generation mobile telephony systems incorporates QAM in some of its higher-speed data transmission modes.

This paper examines a possible solution to designing high-efficiency envelope tracking power supplies, based on using paralleled switching power converters. The 3 main issues discussed in this paper are:

- Comparison between a single converter and the parallel configuration.
- Derivation of a suitable control method.
- Experimental verification.

II. DESIGN SPECIFICATIONS

The practical design problem considered concerns the design of an envelope tracking power supply for an X-band 40W RFPA for a satellite telephony system. The RFPA amplifies a 16-QAM modulated data stream with 150kHz symbol rate, thus requiring the power supply to effectively track a 75kHz square envelope. The following design parameters are obtained:

Table 1 Considered design specifications.

Input voltage (V_{in})	30V
Output voltage (V_{out})	Between $1/3 \cdot V_{in}$ and $2/3 \cdot V_{in}$
Output current	Up to 2A
Equivalent load resistance	≈ 10Ω
Output transition time	Less than 2µs
Output ripple voltage	As low as possible

Where the requirement for a 2µs transition time is set as a compromise between maximizing RFPA efficiency and minimizing the required power supply bandwidth.

III. PROPOSED POWER CONVERSION SCHEME

In high dV/dt applications, high control bandwidth is required. In the considered example, around 300kHz of closed-loop bandwidth is required, leading to a minimal switching frequency of around 1.5MHz if a single buck converter is used. In the voltage range considered, switching losses will be the dominant source of power loss, so by minimizing the current delivered by the fast switching buck converter, its efficiency can be maximized. This can be accomplished by diverting the DC load current to a slower, more efficient buck converter (see Figure 4). However, the slow converter must have a non-zero bandwidth, since the average (past to future) output current, logically enough, is unknown. It must therefore adapt to the current load current, which it should do as quickly as possible to minimize loading of the fast converter. In a proper design, the slow converter output voltage large-signal control bandwidth will be limited by inductor current slew rate, which thus provides a suitable 'adaptation' time constant. The impact of having non-zero control bandwidth, limited by slew-rate is shown in Figure 4.

Note that the inductor currents shown are averaged over one switch cycle (no ripple) and that output capacitor charging/discharging currents are disregarded.

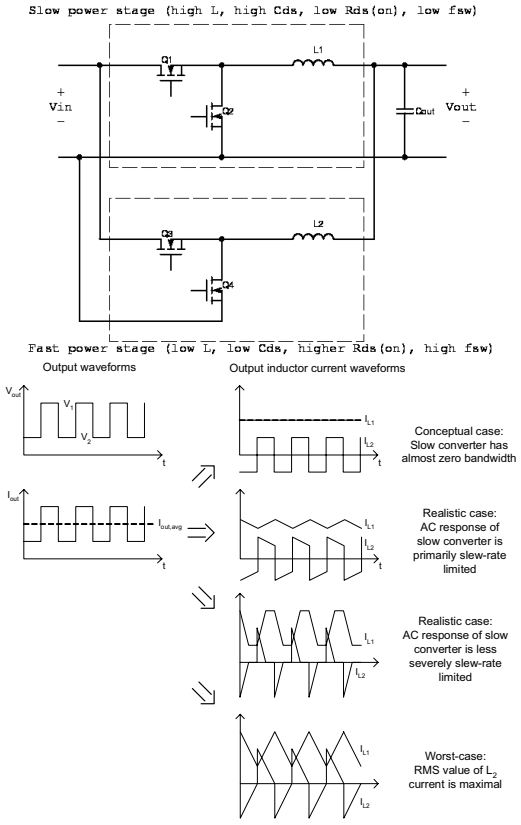

Figure 2 Principal illustration of the proposed power conversion scheme.

Comparison between a single-converter and a dual-converter solution is made based on the conceptual function of the paralleled converters, since RMS inductor currents are otherwise dependent on both inductor values (slew-rate) and square-signal frequency. The worst-case L_2 RMS current is a factor of $2(\sqrt{3})^{-1}\approx 1.15$ times higher than in the conceptual case, so the error made cannot seriously affect the outcome of the comparison.

The following expressions apply for the RMS values of the shown (averaged) conceptual inductor currents:

$$I_{L1,RMS} = \frac{V_1 + V_2}{2R_{load}} \qquad I_{out,RMS} = \sqrt{\left(\frac{V_1 + V_2}{2R_{load}}\right)^2 + \left(\frac{V_1 - V_2}{2R_{load}}\right)^2}$$

$$I_{L2,RMS} = \frac{V_1 - V_2}{2R_{load}}$$

If V_1=20V and V_2=10V (worst-case condition in the considered application), L_1 carries 3 times the RMS current of L_2, and the RMS current in L_2 is thus reduced by a factor of $\sqrt{10}$, when comparing to a single buck converter. This reduction in RMS current is reflected directly to the MOSFETs, allowing the $R_{ds(on)}$ of Q_3, Q_4 to be 10 times higher for a fixed conduction loss. This leads to approximately 10 times lower gate charge, and thus, switching losses. The decrease in switching losses in the fast converter should then be able to accommodate the extra losses associated with adding the slow buck converter.

Reducing the RMS switch current in the fast converter also causes reduced switching (peak) currents, directly contributing to further reduction of switching losses.

In a comparable 2-phase interleaved buck solution, each converter will deliver half the output current. This enables the use of MOSFETs with 2 times higher $R_{ds(on)}$ and thus 2 times lower Q_g for fixed conduction losses, compared to a single buck solution. The FETs in the 2-phase buck will thus switch twice as fast and at half the current, reducing switching losses by a factor of 4. So, provided that efficiency of the slow converter in the proposed scheme is high enough, efficiency will be superior to that of a 2-phase interleaved buck solution.

IV. PROPOSED CONTROL SCHEME

The initial idea for controlling the paralleled converters is to operate the 2 output inductors as current sources, since current sources can be paralleled without problems. This requires each inductor current to be controlled individually. The Laplace-domain block diagram model of the paralleled, current-controlled buck converters is shown in Figure 3. This model is an extension of the single buck converter model utilized in [6].

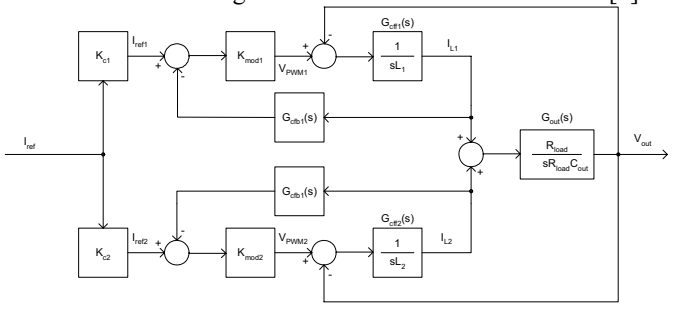

Figure 3 Block diagram of paralleled, current controlled buck converters.

The following transfer function expressions are found:

$$G_{c1}(s)=\frac{V_{out}(s)}{I_{ref1}(s)}=K_{\mathrm{mod}1}G_{out}(s)\frac{G_{cff1}(s)}{1+G_{cff1}(s)(K_{\mathrm{mod}1}G_{cfb1}(s)+G_{out}(s))}$$

$$G_{c2}(s)=\frac{V_{out}(s)}{I_{ref2}(s)}=K_{\mathrm{mod}2}G_{out}(s)\frac{G_{cff2}(s)}{1+G_{cff2}(s)(K_{\mathrm{mod}2}G_{cfb2}(s)+G_{out}(s))}$$

$$G_{c}(s)=\frac{V_{out}(s)}{I_{ref}(s)}=K_{c1}G_{c1}(s)+K_{c2}G_{c2}(s)$$

$G_c(s)$ can be computed numerically using these expressions.

In order to minimize measurement problems, current estimation via inductor voltage integration is utilized. As discussed in [6], this method causes the current loop to transit to voltage mode when the inevitable estimator low-frequency cut-off is reached. The transition into voltage mode has the benefit of lowering output impedance [7], and is the logical reason behind calling the closed current loop around L_1 a 'bandpass' current source. It is obvious that at least *one* of the inductor current loops has to operate down to DC, since paralleling voltage sources would be disastrous. Therefore, current estimation is only used on L_1, which carries the highest RMS current. In order to ensure that the DC current in L_2 is exactly 0, proportional-integral (PI) feedback is used in the current loop around L_2. Thus the closed current loop around L_2 is also a bandpass current source, with zero DC gain.

The derived current control scheme shown in Figure 4.

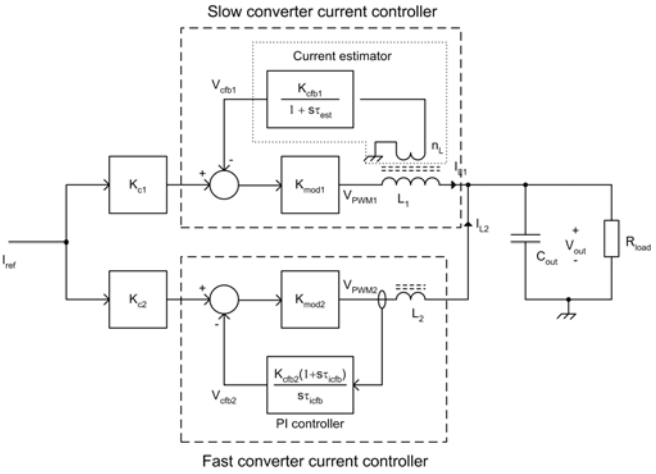

Figure 4 Principal illustration of the proposed current control scheme.

Table 2 Parameters used in current control loop design.

Output filter capacitor	C_{out}	200nF
Slow buck inductor	L_1	50µH
Fast buck inductor	L_2	2.2µH
Current estimator time constant	τ_{est}	300µs
Current estimator gain	K_{cfb1}	1
Inductor sense winding ratio	n_L	1:1
PI current compensator time constant	τ_{icfb}	300µs
Slow PWM modulator gain	K_{mod1}	100
Fast PWM modulator gain	K_{mod2}	100
Slow current loop gain	K_{c1}	1
Fast current loop gain	K_{c2}	1

The transfer function from current reference to output voltage, $G_c(s)$ is plotted for various values of R_{load} in Figure 5, using the parameters shown in Table 2.

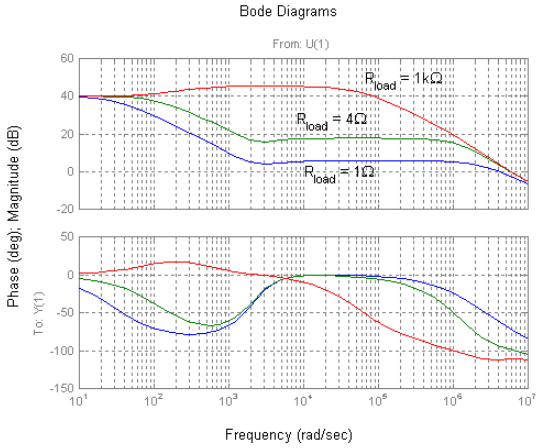

Figure 5 Combined closed-loop current controller transfer functions ($G_c(s)$) with different loads.

Using the selected parameters, the current controller transfer function is well behaved, and all transfer function complex pole/zero pairs have a damping factor > 1 for loads above 1Ω. Voltage control loop design is thus relatively straightforward. In order to increase mid-band loop gain (which is low at 1Ω), lag compensation is used, although this has the effect of decreasing phase margin at higher load resistances. No acceptable design is found suitable for the entire load range above 1Ω but fortunately, the converter aims for applications with load resistances above the 4-8Ω range. The problem observed is general for current controlled designs.

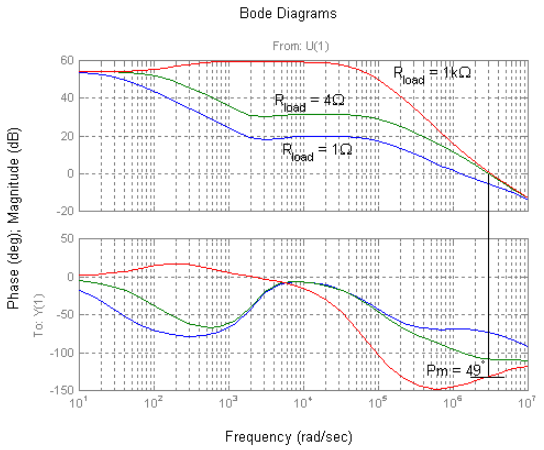

Figure 6 Open-loop voltage control loop transfer functions with different loads, demonstrating worst-case phase margin.

Table 3 Parameters used in voltage control loop design

Lag compensator pole time constant	τ_p	10µs
Lag compensator zero time constant	τ_z	0.82µs
Controller proportional gain	K_P	5

Using the voltage loop compensator parameters given in Table 3 results in the open- and closed-loop Bode plots shown in Figure 6 and Figure 7. The corresponding closed-loop step response is shown in Figure 8.

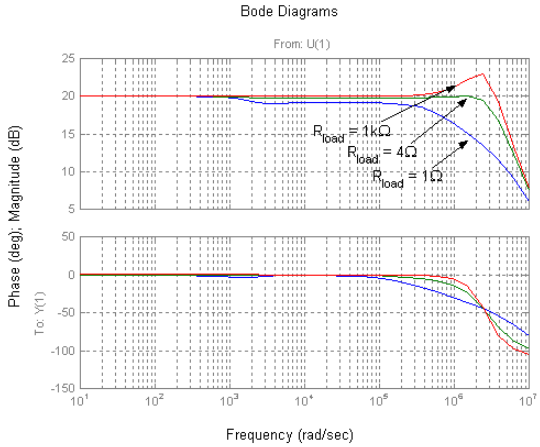

Figure 7 Closed-loop Bode plots of voltage control loop.

Adequate phase margin is obtained at all loads, while the output voltage settles at the correct value within 2µs for load resistances above 4Ω.

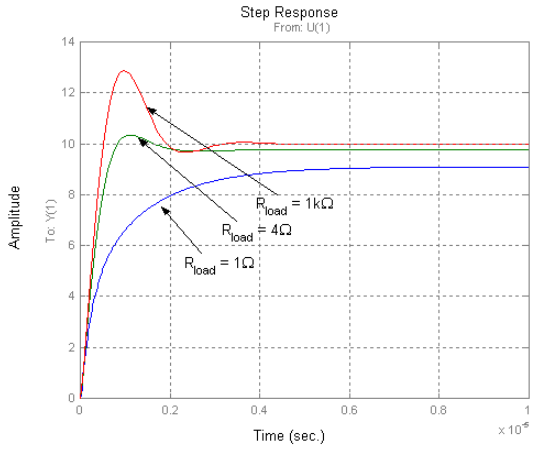

Figure 8 Step responses of closed voltage control loop showing that fast and well damped responses are achievable using the proposed control scheme.

The results obtained with the linear model are mainly useful for confirming that the paralleled converters can be controlled in a stable and fast manner. In the actual system, inductor current slew rates will limit the response speed of the power supply, regardless of the voltage loop gain provided. As will be shown, however, the calculated response times are well within range provided that output filter components are selected correctly.

V. PROTOTYPE DESIGN

Hysteresis control is used in both converters to maximize the control bandwidth per switching frequency ratio [6], [8]. The switching frequency of the fast converter is set to 1.5MHz, reflecting the control bandwidth requirement. The fast converter output filter cut-off frequency is chosen to allow sufficient output voltage slew rate. The L_2 filter inductor value is chosen as a compromise between minimizing ripple current and minimizing inductor size. MOSFETs for the fast converter are chosen with emphasis on low Q_g and C_{DS} to minimize the penalty for operating at high switching frequency, leading to use of the Fairchild FDD5612. This device has the lowest Q_g among considered 60V D-PAK MOSFETs (7.5nC), but still leads to switching losses being dominant.

The slow converter switching frequency is chosen for maximal efficiency. The L_1 filter inductor is finally chosen so that the slow converter contributes with acceptable output ripple voltage.

Closed-loop control bandwidth	B_{-3dB}	300kHz
Fast converter switching frequency	f_{sw2}	1.5MHz
Fast converter output filter cut-off frequency	$\frac{1}{2\pi\sqrt{L_2 C_{out}}}$	240kHz
Fast buck inductor	L_2	2.2µH
Output filter capacitor	C_{out}	200nF
Slow converter switching frequency	f_{sw1}	250kHz
Slow buck inductor	L_1	50µH

VI. SIMULATED RESULTS

A PSpice simulation model is used to verify the power supply design. As shown in Figure 9 and Figure 10, the designed control system leads to absence of DC current in L_2 while maintaining stability and fast response time (≈1.5µs) over the intended load range.

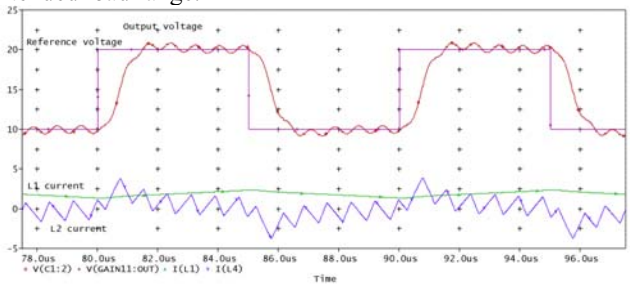

Figure 9 Simulated output (red) and reference voltages (magenta), L_2 (blue) and L_1 (green) buck inductor current. Converter driving 100kHz 10Vpp+15VDC square wave response into 8Ω.

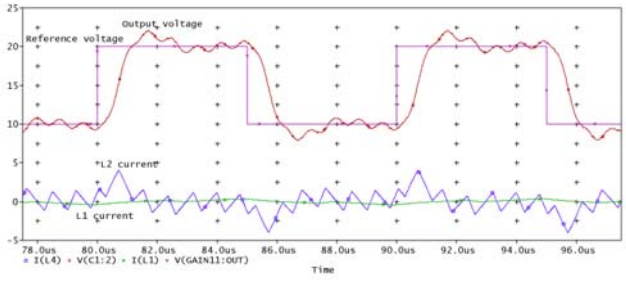

Figure 10 Simulated output (red) and reference voltages (magenta), L_2 (blue) and L_1 (green) buck inductor current. Converter driving 100kHz 10Vpp+15VDC square wave response into open load.

VI. ACHIEVED PRACTICAL RESULTS

A prototype power supply has been implemented, as shown in Figure 11, using a simple 2-layer PCB and low-cost components. Some precautions are necessary to prevent the 2 hysteresis controllers from synchronizing with each other through coupled switching noise. The problem is defeated through filtering at all hysteresis comparator input pins.

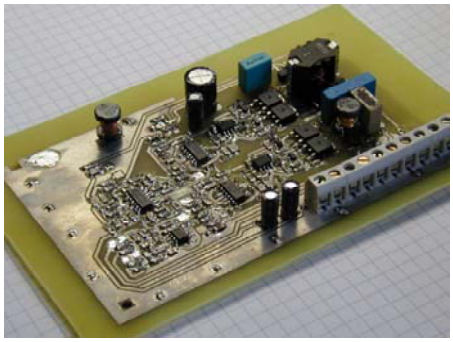

Figure 11 The constructed prototype power supply.

The 100kHz step response into 8Ω is shown along with PWM signal waveforms and inductor currents in Figure 13 and Figure 12. The response+settling time is 2µs, in accordance with specifications. The output voltage response is very similar to the simulated result (in Figure 9) apart from a small overshoot. This is probably due to unmodeled implementation dynamics in the simulation. The current responses are in good agreement, both regarding peak transient currents and ripple currents. It is especially evident that the fast converter supplies only the AC output current, while the slow converter handles the DC current, and as much AC current as allowed by L_1 current slew rate. The latter leads to the slow converter 'locking' onto the reference signal frequency, which is a feature of the hysteresis controller.

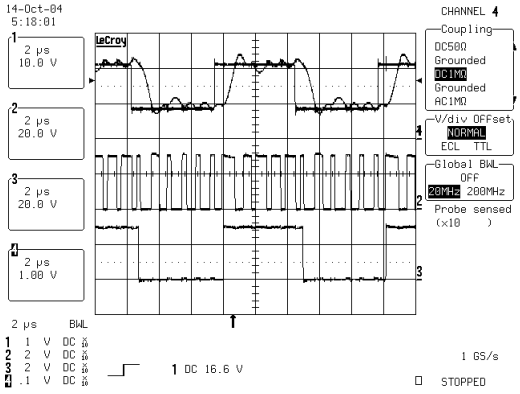

Figure 12 Output and reference voltages (top), HF (middle) and LF (bottom) buck PWM output voltages. Converter driving 100kHz 12Vpp+15VDC square into 8Ω.

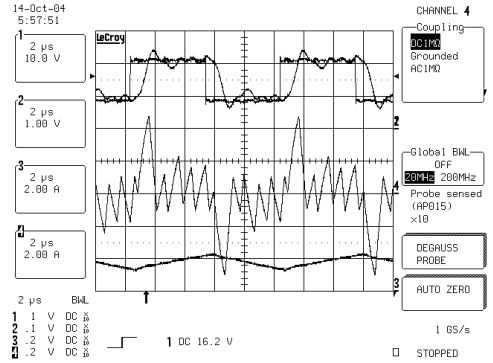

Figure 13 Output and reference voltages (top), HF (middle) and LF (bottom) buck inductor current, conditions as in Figure 12.

The unloaded step response is shown in Figure 14. A small overshoot occurs as predicted by simulation.

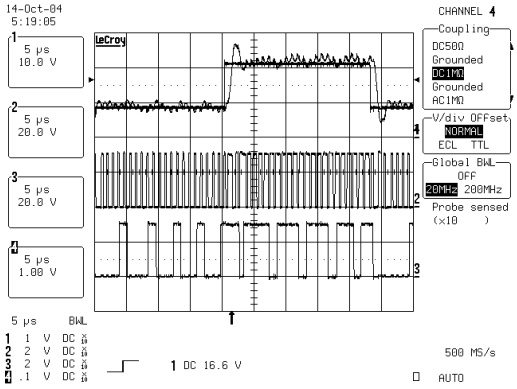

Figure 14 Output and reference voltages (top), HF (middle) and LF (bottom) buck PWM output voltages. Converter driving 20kHz 12Vpp+15VDC square into open load.

The long-term response of the inductor currents to an output voltage step is shown in Figure 15. This measurement clearly illustrates that the slow converter operates to its maximum capability during transients, and thus that the fast converter delivers an absolute minimum fraction of the load current. The absence of DC current in L_2 is also apparent.

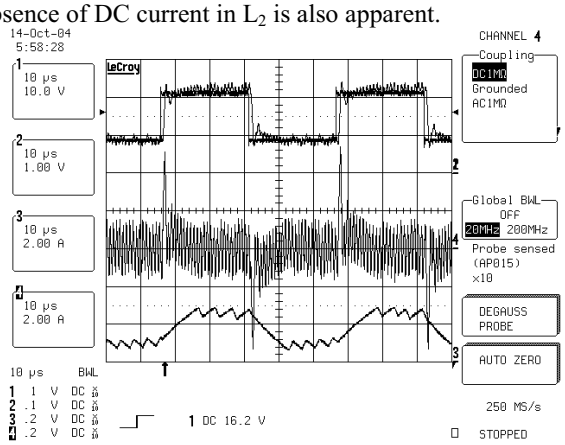

Figure 15 Output and reference voltages (top), HF (middle) and LF (bottom) buck inductor current. Converter driving 20kHz 12Vpp+15VDC square into 8Ω.

A power loss estimation model for the paralleled buck converters has been implemented in MATLAB. Figure 16 shows a comparison between estimated and measured efficiency for a constant output voltage. A high-speed oscilloscope with current probes is used for input/output power measurement since there is significant ripple, especially on output voltage. Oscilloscope measurement errors (measurement resolution is 8 bits) should account for some of the deviation between calculated and measured efficiency.

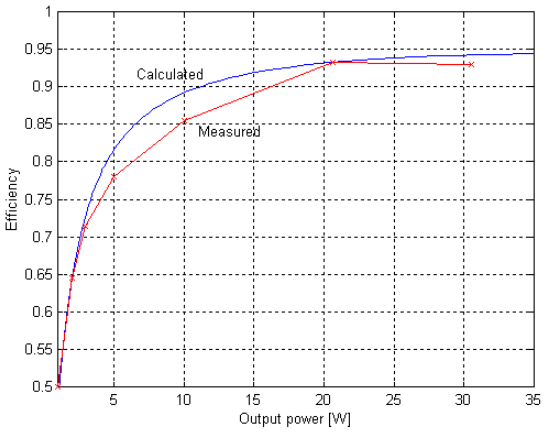

Figure 16 Calculated and measured efficiency figures for stationary 15VDC output voltage.

VII. CONCLUSION

A power conversion and control scheme for power supplies requiring high slew-rate and high efficiency has been presented. The power conversion scheme has been compared to a simpler solution, thereby justifying the proposed, more complex, solution. Comparison with a 2-phase buck solution has proven a complicated task, at least requiring complete loss calculation models for both topologies. However, simple initial considerations show that the proposed topology probably can perform at least as well as the more common 2-phase buck topology.

A fully operational prototype has demonstrated high efficiency, considering the bandwidth and slew-rate provided. The high efficiency naturally results from the use of a highly efficient low-bandwidth converter unloading the high-bandwidth converter in parallel, allowing reduced switching losses in the high-bandwidth converter.

For the control part, operation has been explained by linear modeling, and verified both through simulation and experimental work.

The results presented in this paper are currently state-of-the-art within the field of high-bandwidth power supplies with paralleled switching power conversion.

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(19) United States

(12) Patent Application Publication

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(43) Pub. Date: Feb. 4, 2010

HOYERBY

(54) **BAND-PASS CURRENT MODE CONTROL SCHEME FOR SWITCHING POWER CONVERTERS WITH HIGHER-ORDER OUTPUT FILTERS**

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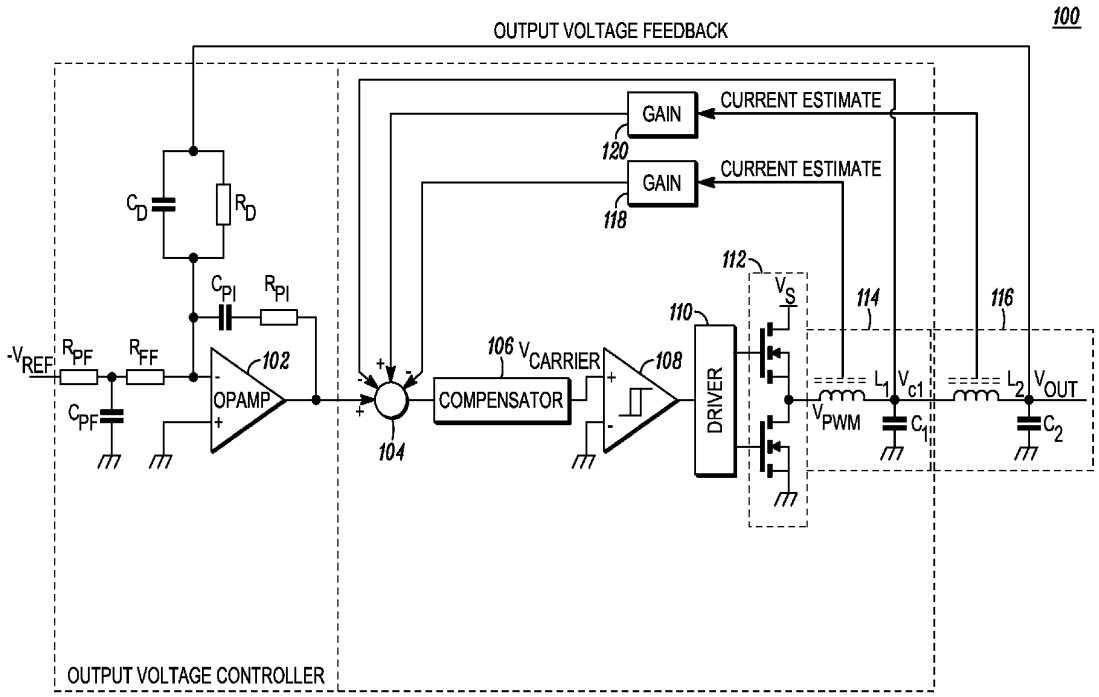
H02M 1/14 (2006.01)

(52) **U.S. Cl.** **363/39**

(57) **ABSTRACT**

A DC-DC converter is described that contains multiple estimators and is self-oscillation. The converter also contains at least a fourth order output filter. The converter contains both feedback and feed-forward paths. The estimators estimate the current through inductors in the filter by sensing the voltage across the inductors.

The forward feed path contains a comparator. The self-oscillation is provided by hysteresis in the comparator or by a phase-shift network connected to the comparator. The estimators comprise extra windings coupled to each inductor or a series combination of a resistor and a capacitor connected in parallel with the inductor.



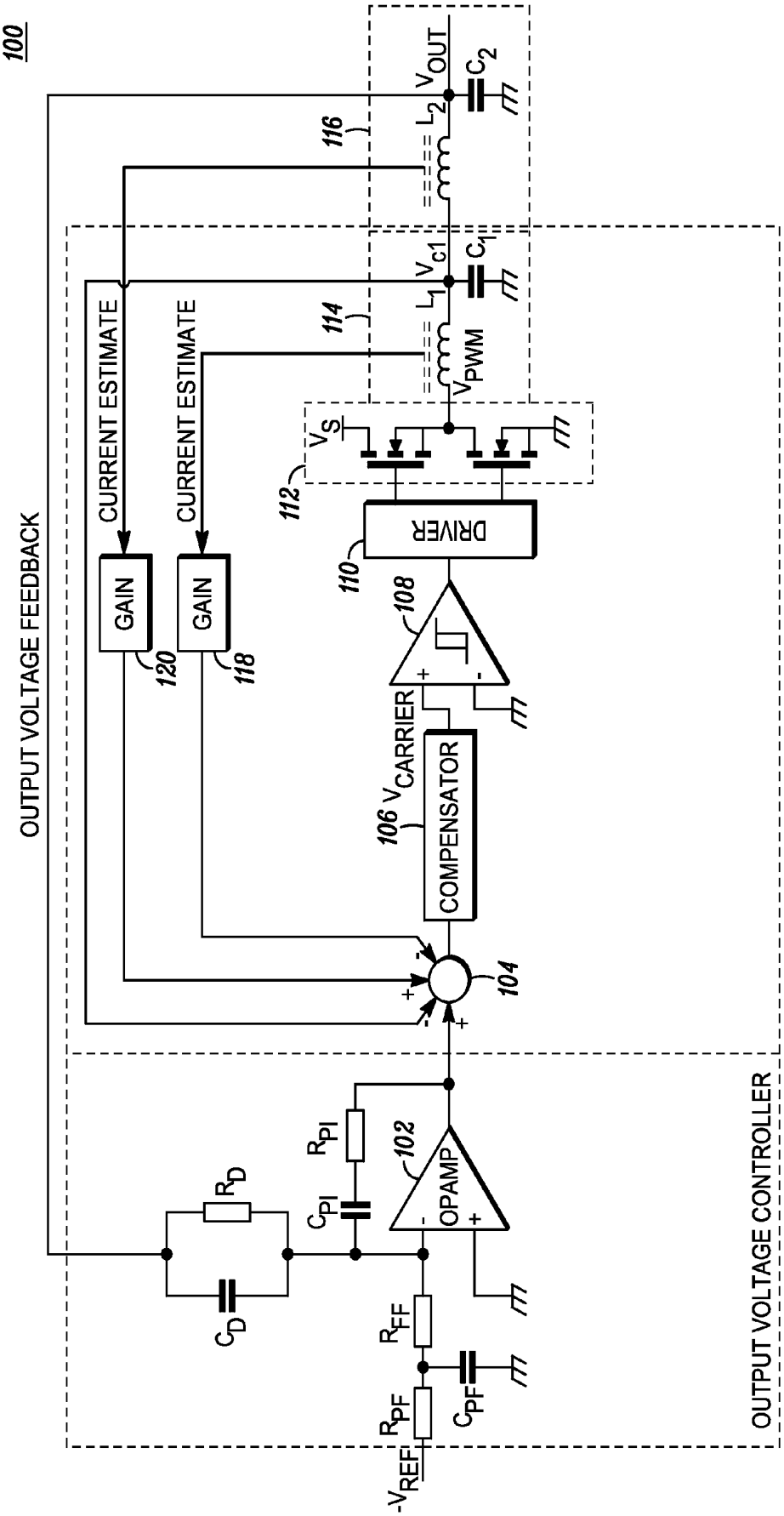

100
OUTPUT VOLTAGE FEEDBACK
CURRENT ESTIMATE
CURRENT ESTIMATE
GAIN
GAIN
120
118
116
114
112
110
108
106
104
102
V_{OUT}
C_2
L_2
V_{c1}
C_1
L_1
V_{PWM}
V_S
DRIVER
$V_{CARRIER}$
COMPENSATOR
OPAMP
R_{PI}
C_{PI}
R_D
C_D
R_{FF}
C_{PF}
R_{PF}
$-V_{REF}$
OUTPUT VOLTAGE CONTROLLER

FIG. 1

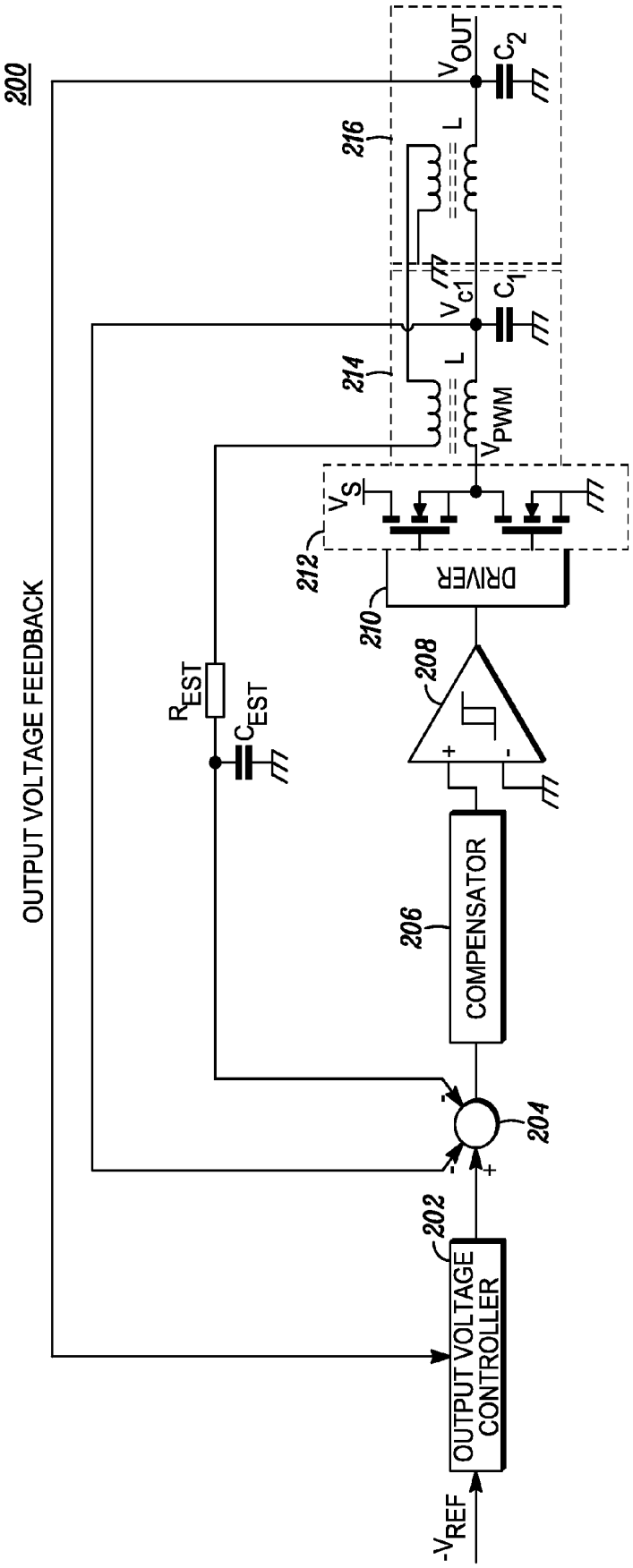

200
OUTPUT VOLTAGE FEEDBACK
V_{OUT}
C_2
216
L
V_{C1}
C_1
214
L
V_{PWM}
V_S
212
DRIVER
210
208
R_{EST}
C_{EST}
206
COMPENSATOR
204
202
OUTPUT VOLTAGE CONTROLLER
$-V_{REF}$

FIG. 2

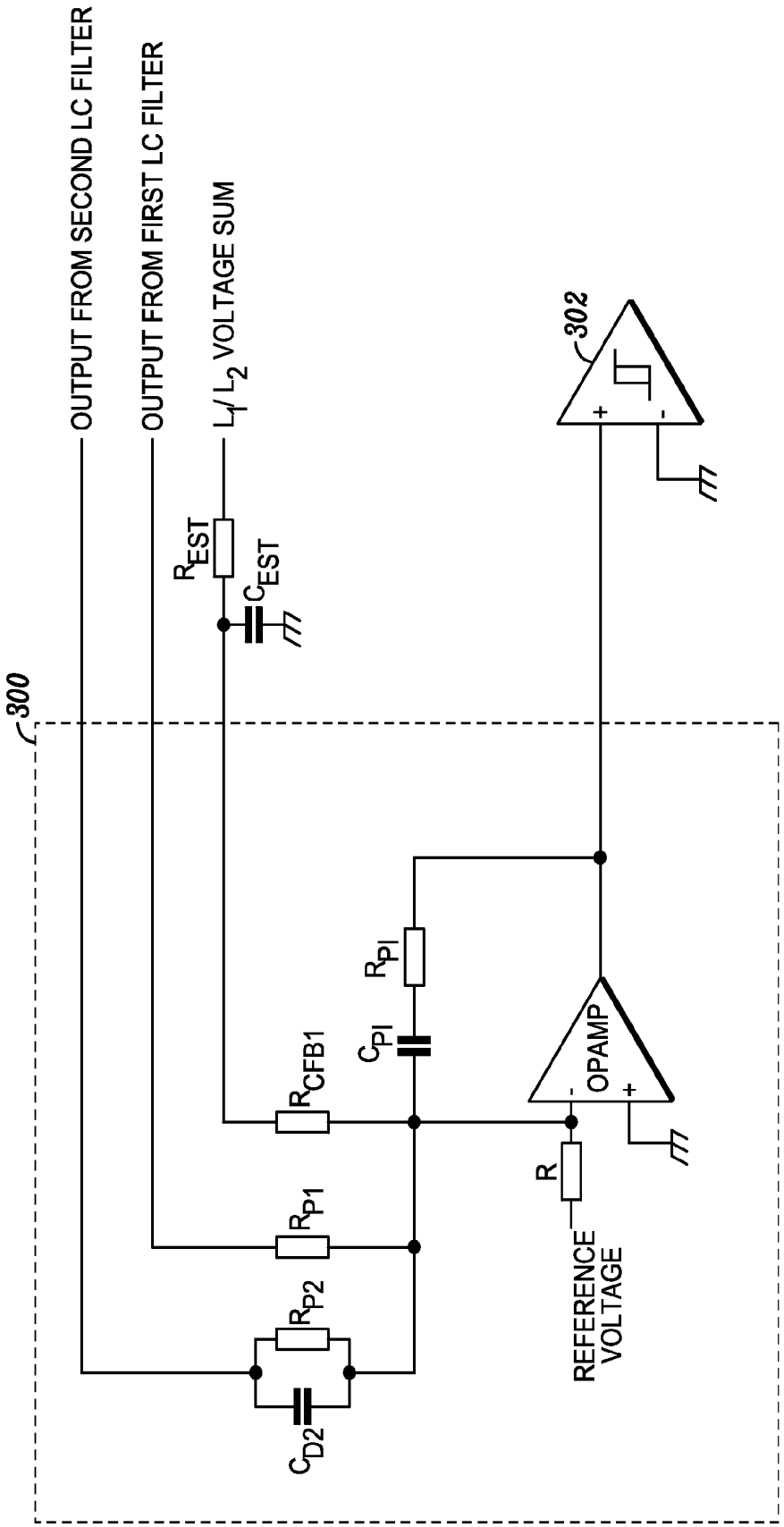

OUTPUT FROM SECOND LC FILTER
OUTPUT FROM FIRST LC FILTER
L1/L2 VOLTAGE SUM
300
302
REST
CEST
RPI
CPI
RCFB1
RP1
RP2
CD2
OPAMP
R
REFERENCE VOLTAGE

FIG. 3

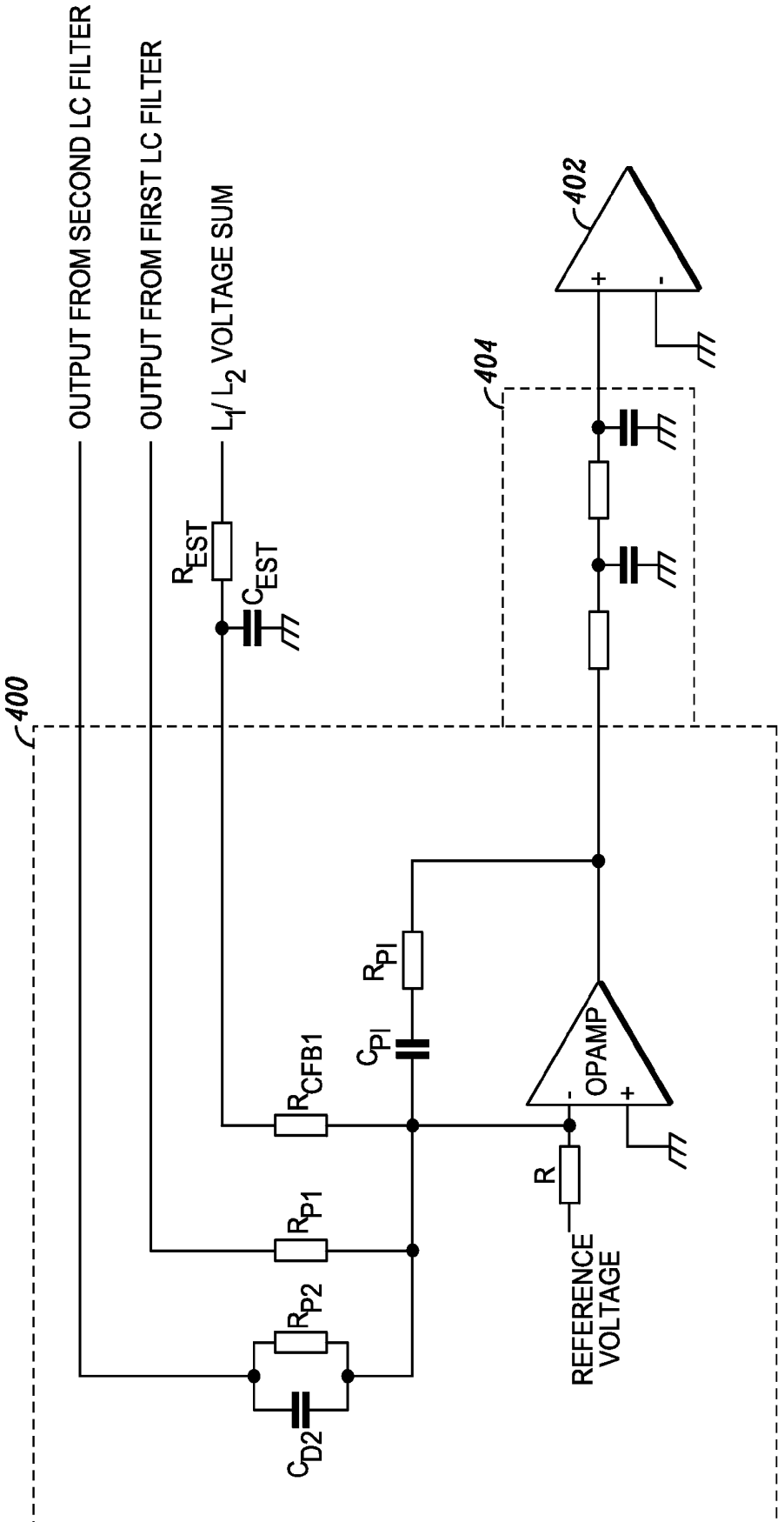

OUTPUT FROM SECOND LC FILTER
OUTPUT FROM FIRST LC FILTER
L1/L2 VOLTAGE SUM
400
402
404
REST
CEST
RPI
CPI
RCFB1
RP1
RP2
CD2
OPAMP
R
REFERENCE VOLTAGE

FIG. 4

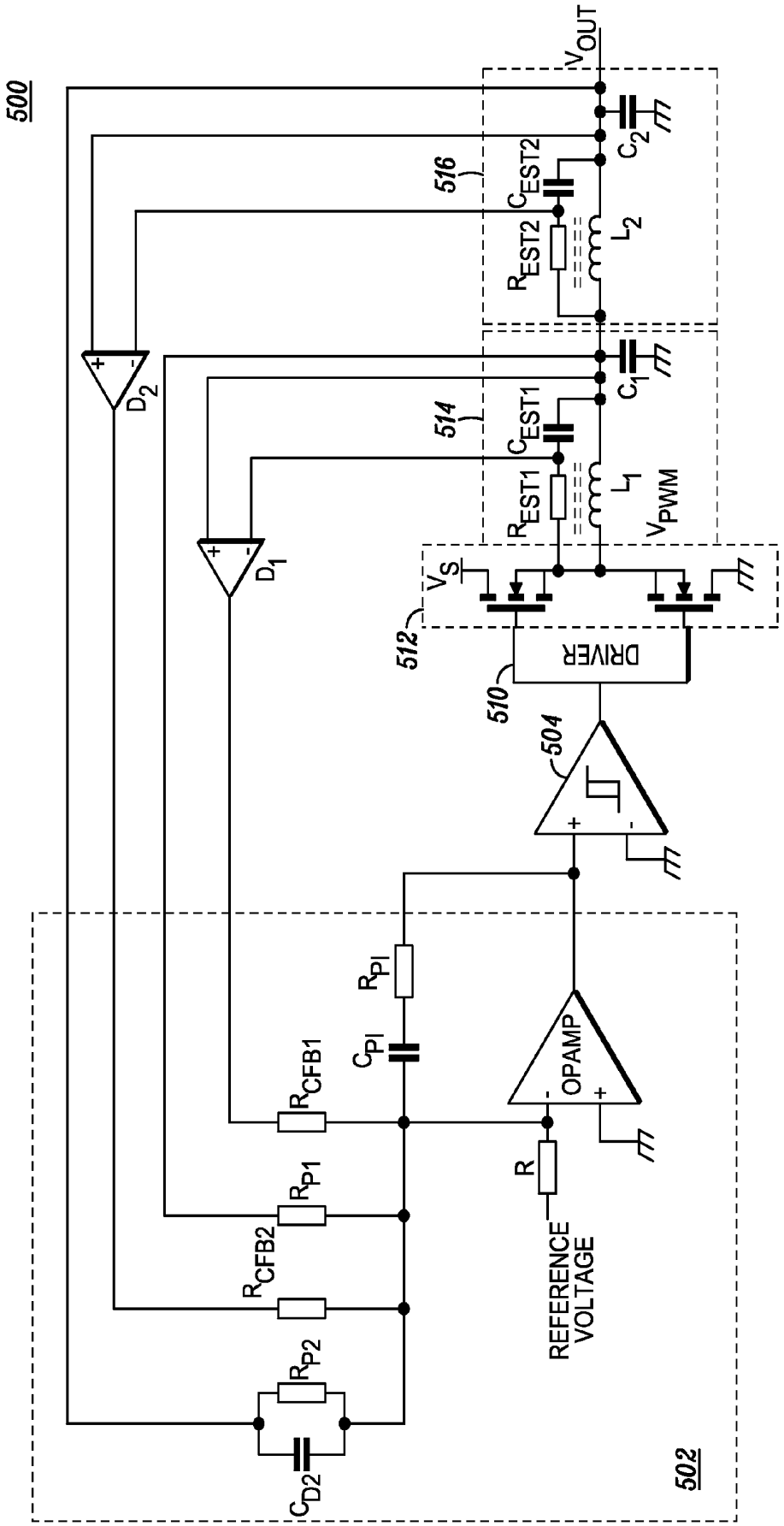

500
V_{OUT}
C_2
516
C_{EST2}
R_{EST2}
L_2
C_1
514
C_{EST1}
R_{EST1}
L_1
V_{PWM}
D_2
D_1
V_S
512
DRIVER
510
504
R_{PI}
C_{PI}
R_{CFB1}
R_{P1}
R_{CFB2}
R_{P2}
C_{D2}
OPAMP
R
REFERENCE VOLTAGE
502

FIG. 5

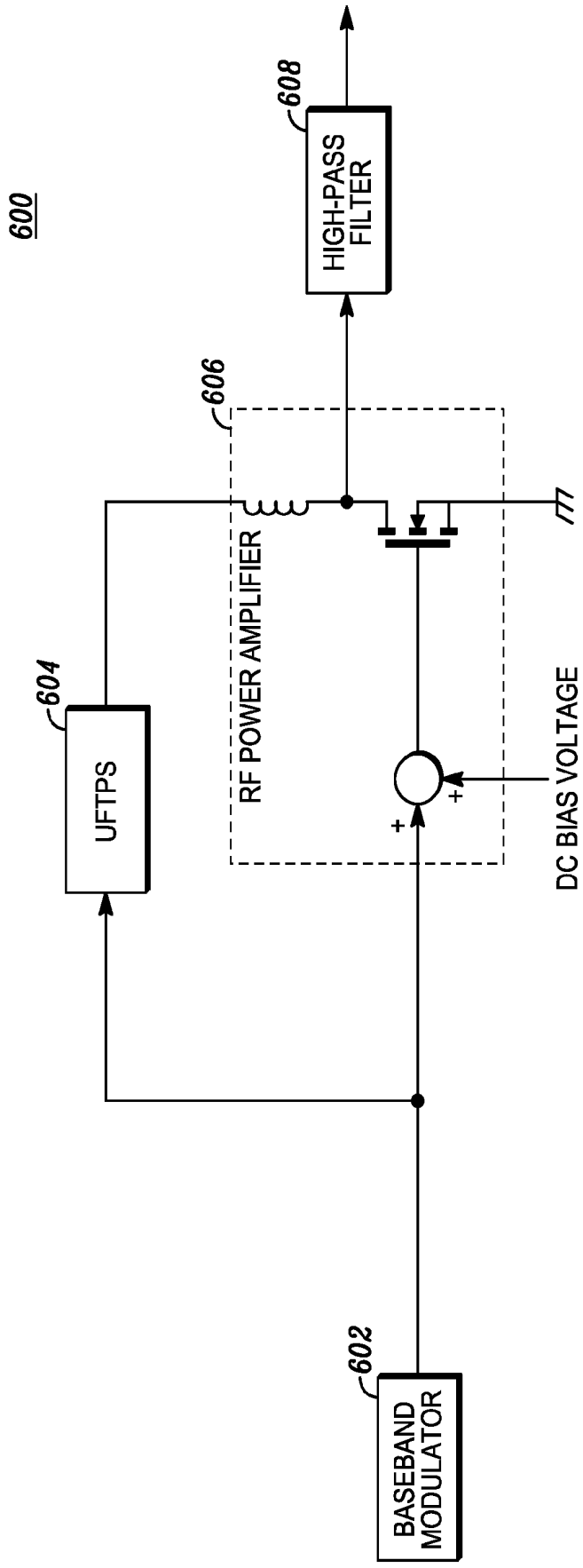

600
608
HIGH-PASS FILTER
606
RF POWER AMPLIFIER
604
UFTPS
DC BIAS VOLTAGE
602
BASEBAND MODULATOR

FIG. 6

BAND-PASS CURRENT MODE CONTROL SCHEME FOR SWITCHING POWER CONVERTERS WITH HIGHER-ORDER OUTPUT FILTERS

TECHNICAL FIELD

[0001] The present application relates to power amplifiers. In particular, the application relates to the power amplifiers having output inductors and feedback loops containing estimates of the current through the inductors.

BACKGROUND

[0002] Power amplifiers are used in a variety of applications. In communication systems, for example, power amplifiers provide the desired signal strength for radio frequency (RF) wireless transmissions between a base station and a wireless handset. A power supply provides power to the power amplifier. In some communication power amplifier systems, an Ultra-Fast Tracking Power Supply (UFTPS) is employed to better control the power amplifier in the transmitter to provide the desired instantaneous output power level, thereby better maximizing the efficiency of the power amplifier by limiting the wasted power.

[0003] To realize power savings in the system, the UFTPS is to act as a low-dissipation controllable voltage source from DC to the RF bandwidth. It is thus desirable for the UFTPS to have sufficiently low power losses. The UFTPS typically employs a switch-mode power converter to provide such a low power loss. Besides power savings, reducing the response time is also desirable. Accordingly, it is desirable for the output voltage of the UFTPS to respond relatively quickly to changes in the reference voltages—ideally at a rate equivalent to the bandwidth of the transmitted signal (e.g., 25-150 kHz). Further, to avoid interference when intermodulation of the output occurs with the transmitted RF signal, it is desirable for the output ripple voltage of the switch-mode power converters to be relatively small, e.g., 5-50 mVpp. Also, it is desirable for the UFTPS to have a relatively low output impedance (e.g., 10-100 mΩ) from DC to the RF bandwidth.

[0004] One example of a commonly-used power supply is a single-phase buck converter (in which a single DC-DC converter is disposed between the input and the load). A buck converter in a UFTPS application may contain one or more output filters coupled with multiple proportional-derivative (PD) control loops to form a proportional-integral-derivative (PID) controller. However, while a buck converter that contains multiple LC filters and control loops is useful in an UFTPS application, the components used in the control loops are subject to practical implementation problems such as increased power consumption, noise sensitivity, and sensitivity to circuit parasitics. It is accordingly desirable to provide a buck converter that reduces these problems.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Embodiments will now be described by way of example with reference to the accompanying drawings, in which:

[0006] FIG. **1** illustrates a BPCM control buck converter according to one embodiment.

[0007] FIG. **2** illustrates a BPCM control buck converter according to another embodiment.

[0008] FIG. **3** shows a portion of a BPCM control buck converter according to another embodiment.

[0009] FIG. **4** shows a portion of a BPCM control buck converter according to another embodiment.

[0010] FIG. **5** illustrates a BPCM control buck converter according to another embodiment.

[0011] FIG. **6** illustrates one embodiment of a power amplifier system containing a UFTPS.

DETAILED DESCRIPTION

[0012] A power amplifier system containing a buck converter and method of providing DC-DC conversion is described. The power amplifier system contains multiple estimators and self-oscillating control in a multiple order filtered buck converter. The buck converter contains feedback and feed-forward control paths. The feed-forward path contains a comparator. The self-oscillation is provided either by a phase-shift network disposed before the comparator in the feed-forward signal path or by hysteresis in the comparator. The estimators estimate currents through the inductors and capacitors in the output filter by sensing the voltage across the inductors.

[0013] The various individual components are well-known to one of skill in the art and will not be described in detail. Further, other circuitry that is associated with the power amplifier system and is well-known to one of skill in the art will not be described for conciseness.

[0014] FIG. **1** illustrates one embodiment of a switch-mode power converter. The power converter shown is a Band Pass Current Mode (BPCM) controlled buck converter, with Band-Pass Current Mode Feedback arranged as to achieve the dynamics of a Global Loop Integrating Modulator (GLIM). The BPCM buck converter in general contains a switching power converter with an output filter in which multiple loops provide feedback from the output filters. The BPCM buck converter **100** shown uses an estimate of the inductor current rather than using direct voltage measurements as feedback to control the buck converter **100**. The BPCM current feedback signals, along with the feedback of one of the capacitor voltages (V_{cl}) of a capacitor C_1 in the output filter, function together to effectively create feedback control of the voltage and current of this capacitor C_1, thereby realizing proportional-derivative (PD) feedback control of the voltage of the capacitor C_1 without employing a differentiating element for the differentiating portion of the PD loop coupled with the capacitor C_1. Avoiding the use of a differentiator reduces problems due to noise in the physical controller implementation.

[0015] Additionally, the BPCM buck converter **100** contains a proportional-integral-derivative (PID) controller, which is a control loop feedback mechanism that corrects an error between the output voltage and a desired voltage by calculating an error correction and then providing the error correction to adjust the output voltage. The PID controller contains proportional, integral, and derivative paths. The first of these paths determines the reaction to the current error, the second determines the reaction based on the sum of recent errors, and the third determines the reaction to the rate at which the error has been changing. A weighted sum of these paths is used to adjust the output voltage.

[0016] As shown, the buck converter **100** contains an output voltage controller **102** to which a negative reference voltage $-V_{REF}$ is supplied through a low pass filter. The output voltage controller **102** is connected with an adder **104**. The output of the adder **104** is connected with an input of a compensator **106**. The compensator **106** may contain, for

example, a proportional-integral (PI) feed forward in which the derivative path is eliminated, which, combined with the PD emulation of the BPCM feedback, leads to control solution functionally equivalent to that of a PID controller but with added immunity to circuit parasitics and switching noise. The output of the compensator **106** is connected with an input of a comparator **108** with hysteresis, which may be a conventional Schmitt trigger. The hysteresis of the comparator **108** provides a self-oscillation mechanism. The output of the comparator **108** alternates between the positive and negative supply voltages dependent on whether the voltage supplied to the positive terminal is larger than the voltage supplied to the negative voltage (which, as shown, is ground) or vice-versa.

[0017] The output of the comparator **108** is connected to a driver **110** to activate the driver **110**, which in turn drives a pair of power transistors **112** connected in a simple push-pull configuration (although other configurations can be used). The transistors **112** can be field effect devices, such as MOSFETs, or bipolar devices, such as BJTs.

[0018] The outputs of the transistors **112** are connected to a first LC output filter **114**. The first LC output filter **114** is connected in series with a second LC output filter **116**. The first and second LC output filters form a 4^{th} order output filter, which decrease the ripple of the output voltage from the buck converter **100**. The first and second LC output filters **114**, **116** contain an inductor L_1, L_2 and a capacitor C_1, C_2, respectively. The switching frequencies of the transistors **112**, which are much higher than the maximum frequency response of the human ear (about 20 kHz), cause radio-frequency interference. The output filters **114**, **116** reduce this interference and allow the output signal to correspond to the input signal. However, as the output filters **114**, **116** are potentially undamped and the current drawn from the output terminal (node V_{out}) is time-varying, the output voltage V_{out} is controlled via negative feedback. Multiple feedback loop are used because of the difficulty in compensating for the phase lag of the entire fourth order filter in a single control loop. The voltage from the second LC output filter **116** (the output voltage V_{OUT}) is integrated and supplied as feedback through an outer PD control loop to an operational amplifier (OpAmp) in the controller **102**, where the difference between the reference signal V_{REF} and the output voltage V_{OUT} is used to adjust the voltage from the controller **102**. The voltage from the first LC output filter **114** is supplied as feedback through an inner PD control loop to the adder **104** such that this voltage is subtracted from the voltage from the controller **102**.

[0019] Rather than the currents in the output filters being directly supplied to an integrator to thereby provide PD feedback, these currents are estimated. Specifically, the current through the capacitor C_1 (and the current through the inductor L_1) in the first LC output filter **114** is estimated by sensing the voltage across the inductor L_1 in the first LC output filter **114** and then integrating or low-pass filtering the sensed result. The current through the capacitor C_2 (and the current through the inductor L_2) in the second LC output filter **116** is similarly estimated by sensing the voltage through the inductor L_2 in the second LC output filter **116**. As the voltages through the inductors L_1, L_2 are relatively large, they may be sensed relatively easily. The estimate of the current through the capacitor C_1 in the first LC output filter **114** and the estimate of the current through the capacitor C_2 in the second LC output filter **116** are supplied to the adder **104** through first and second gains **118**, **120**, respectively. The first and second gains **118**, **120** may be the same or different and are either preset (i.e., unchangeable once implemented) or controllable as desired. The amplified estimates are subtracted by the adder **104** so that the difference between the amplified estimates is added to the output of the controller **102** and the voltage of the capacitor C_1 of the first LC output filter **114** subtracted therefrom.

[0020] The resulting signals from the output filters **114**, **116** emulate PD current feedback without the use of noise- and parasitic-sensitive differentiation of the capacitor voltages—in FIG. **1**, only a single capacitor voltage is supplied directly as feedback to the output voltage controller **102**. Instead, the inductor voltages in the LC output filters are sensed and the currents through the capacitors estimated and supplied as the PD feedback.

[0021] The manner in which the signals travel through the converter **100** is now described. Specifically, the OpAmp in the controller **102** receives a sine wave input. An integrator connected between the input and output of the controller **102** integrates the difference between input and output voltages of the OpAmp, resulting in the triangular waveform. The comparator **108** receives the triangular waveform, modified by the adder **104** and compensator **106** and generates square voltage pulses. These pulses are then amplified by the transistors **110** and transmitted to the output filters **112**, **114** to reconstruct the desired output signal V_{OUT}. Note that switching of the comparator **108** at high speed results in a square wave whose pulse width and frequency is dependent on the input voltage and frequency and whose average value corresponds to the buck converter input.

[0022] FIG. **2** illustrates another embodiment of a BPCM control buck converter. Similar to the embodiment of FIG. **1**, the BPCM buck converter **200** of FIG. **2** contains an output voltage controller **202** to which a reference voltage is supplied, an adder **204**, a compensator **206**, a comparator **208** with hysteresis, a driver **210**, transistors **212**, and first and second LC output filters **214**, **216**. These elements are connected together in a manner similar to that of FIG. **1**. Further, similar to the embodiment of FIG. **1**, the voltages in the inductors L_1, L_2 in each of the first and second LC output filters **214**, **216** are sensed and estimates are made of the current through the capacitor C_1, C_2. Specifically, in the embodiment of FIG. **2**, the voltages in the inductors L_1, L_2 are sensed by extra windings. The current through the capacitor C_1 in the first LC output filter **214** is estimated using floating sense windings as a difference block. This voltage difference, which corresponds to the derivative of the capacitor C_1 current, is then integrated using a low pass filter R_{est}, C_{est} disposed in the feedback path between the first LC output filter **214** and the adder **204**. Using this inner PD control loop permits a wide variety of outer PD control loops to be added.

[0023] One example of an output voltage controller **300** is illustrated in FIG. **3**. As shown, the output voltage from the capacitor C_2 of the second LC output filter **216** as shown in FIG. **2** is connected to the inverting terminal of the OpAmp in the controller **300** through a parallel resistor/capacitor R_{P2}, C_{D2} combination. The low-pass filtered voltage difference output between the inductors L_1, L_2 is connected to the inverting terminal of the OpAmp through a resistor R_{cfb1}. The capacitor C_1 is also connected to the inverting terminal of the OpAmp through a resistor R_{PI} to convert the current to a voltage. Feedback is supplied between the output and the inverting terminal of the OpAmp through another integrator of a series resistor/capacitor R_{PI}, C_{PI} combination.

[0024] In another example of a controller and circuitry connected thereto is illustrated in FIG. **4**, the voltage controller **400** is similar to that of FIG. **3**. Unlike the embodiment of FIG. **3**, in which a hysteresis-containing comparator is used to provide the self-oscillation, a phase-shift network provides the self oscillation by providing a phase shift to the output triangular wave from the OpAmp. Thus, rather than the output of the OpAmp of the voltage controller being connected directly to the input of a hysteresis-containing comparator, as shown in the embodiment of FIG. **4**, the phase-shift network **404** is disposed between the output of the OpAmp of the voltage controller **400** and the input of a comparator **402**. The comparator **402** of FIG. **4** does not contain hysteresis as the self oscillation is provided by the phase shift network. The phase-shift can either be preset or controllable as desired, with only the preset version being shown. Other implementations of a phase-shift network using different topologies may be used as desired.

[0025] FIG. **5** illustrates another embodiment of a buck converter. This buck converter **500** contains a controller **502**, a compensator **504** with hysteresis, a driver **510**, a pair of push-pull transistors **512**, and first and second LC output filters **514**, **516** again connected in a manner similar to that of the buck converter **100** of FIGS. **1** and **2**. Unlike the embodiment of FIG. **2**, the buck converter **500** of FIG. **5** does not sense the voltage of the inductors using extra coils, which may be relatively large, bulky, and expensive. Instead, a series combination of an RC filter is connected in parallel with the inductor L_1, L_2 in each of the LC output filters **514**, **516**. The voltage across the capacitor C_{est1}, C_{est2} in each of the series LC combinations provides the input to a differential amplifier D_1, D_2. The output of each differential amplifier D_1, D_2 is connected to the inverting terminal of the OpAmp through a respective resistor R_{cfb1}, R_{cfb2}.

[0026] Although only one type of filter is shown in the figures, filters with other characteristics and orders may be used. Each of these filters may contain an inductor of which the voltage thereacross is detected and the current estimated rather than being directly provided in a feedback loop. The components in the forward and reverse portion of the loop may be altered to achieve the desired loop characteristics.

[0027] FIG. **6** illustrates a power amplifier system **600**. The power amplifier system **600** contains a baseband modulator **602** whose output is connected to the inputs of both a UFTPS module **604** and a power amplifier module **606**. The UFTPS module **604** contains a buck converter similar to that of FIGS. **1-5** and provides the power supply for the power amplifier module **606**. As shown, the output voltage of the baseband modulator **602** is combined with a DC bias voltage and then amplified by a power transistor in the power amplifier module **606**. The output of the UFTPS module **604** is provided as a supply voltage to the power transistor through an inductor. The output of the power amplifier module **606** is supplied to a high pass filter **608**, whose output is provided as the output of the power amplifier system **600**.

[0028] Note that although the embodiments shown in the figures contain multiple current estimators, in other embodiments at least one direct connection can be used and at least one current estimator can be used when multiple LC filters are used.

[0029] The buck converters and power amplifier described herein are useful in narrowband RF systems with variable RF amplitude. Such systems include Tetra (TErrestrial Trunked RAdio), Tetra2, iDen (Integrated Digital Enhanced Network) systems. The buck converters can be used in multiple communication applications including individual handsets and other subscriber applications or base stations.

[0030] It will be understood that the terms and expressions used herein have the ordinary meaning as is accorded to such terms and expressions with respect to their corresponding respective areas of inquiry and study except where specific meanings have otherwise been set forth herein. Relational terms such as first and second and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual such relationship or order between such entities or actions. The terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. An element proceeded by "comprises . . . a" does not, without more constraints, preclude the existence of additional identical elements in the process, method, article, or apparatus that comprises the element.

[0031] Those skilled in the art will recognize that a wide variety of modifications, alterations, and combinations can be made with respect to the above described embodiments without departing from the spirit and scope of the invention defined by the claims, and that such modifications, alterations, and combinations are to be viewed as being within the purview of the inventive concept. Thus, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. The invention is defined solely by the appended claims including any amendments made during the pendency of this application and all equivalents of those claims as issued.

1. A switch-mode power converter comprising:

an output filter of at least fourth order containing a plurality of inductors and capacitors; and

a control system comprising a plurality of inductor estimators positioned to sense voltage across the inductors and estimate current through the inductors, a feedback loop providing the estimates to an input of the control system, and a self-oscillation mechanism to provide self-oscillation of the control system, wherein the output filter is connected with an output of the control system and comprises a plurality of low pass filters connected in series.

2. The switch-mode power converter of claim **1**, wherein the control system comprises a forward feed path containing an OpAmp, a proportional-integral (PI) compensator, and a comparator, the PI compensator connected between the OpAmp and the comparator in the forward feed path.

3. The switch-mode power converter of claim **2**, wherein the comparator contains hysteresis and is connected such that the self-oscillation mechanism comprises the comparator.

4. The switch-mode power converter of claim **2**, wherein the control system further comprises a phase-shift network

connected between the OpAmp and comparator, the self-oscillation mechanism comprising the phase-shift network and the comparator.

5. The switch-mode power converter of claim **2**, further comprising second feedback loops each connecting one of the capacitors with an inverting input of the OpAmp, one of the second feedback loops containing a resistor and another of the second feedback loops containing a parallel combination of a capacitor and another resistor.

6. The switch-mode power converter of claim **2**, wherein the feedback loop comprises a gain disposed between each inductor estimator and the input of the control system, each gain being independently controllable.

7. The switch-mode power converter of claim **2**, wherein each inductor estimator comprises extra windings coupled to the respective inductor.

8. The switch-mode power converter of claim **7**, wherein the feedback loop comprises a low pass filter and the extra windings are connected in series between ground and the low pass filter.

9. The switch-mode power converter of claim **2**, wherein each inductor estimator comprises a series combination of a resistor and a capacitor connected in parallel with the respective inductor.

10. The switch-mode power converter of claim **9**, wherein each inductor estimator further comprises a differential amplifier whose inputs are connected to either side of the respective capacitor.

11. The switch-mode power converter of claim **2**, wherein the control system further comprises a driver driving power transistors connected in a push-pull configuration, the driver and power transistors connected between the OpAmp and the output filter.

12. A method of providing power conversion comprising:
providing a feed forward path;
providing self-oscillation along the feed forward path;
low pass filtering a self-oscillated signal using an output filter of at least fourth order;
estimating current through inductors in the output filter by sensing voltages of the inductors; and
feeding back the estimates along a feedback loop to the feed forward path.

13. The method of claim **12**, further comprising providing a differential amplification and proportional-integral (PI) compensation along the forward feed path.

14. The method of claim **12**, wherein providing the self-oscillation comprises providing a comparator containing hysteresis.

15. The method of claim **12**, wherein providing the self-oscillation comprises providing a controllable phase-shift network connected between a differential amplifier and a comparator in the feed forward path.

16. The method of claim **12**, further comprising providing independently controllable gain for each inductor current along the feedback loop.

17. The method of claim **12**, wherein each estimation is provided using extra windings coupled to the respective inductor.

18. The method of claim **12**, wherein each estimation is provided using a series combination of a resistor and a capacitor connected in parallel with the respective inductor.

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(54) **Title**: COMBINED FEEDBACK AND FEED-FORWARD LINEARISATION OF RF POWER AMPLIFIERS

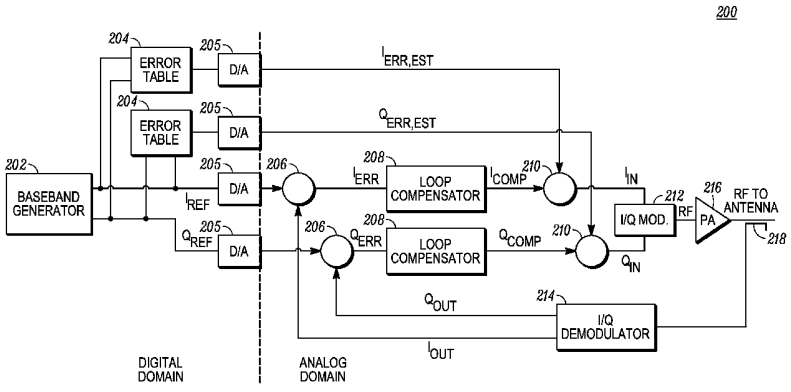

FIG. 2

(57) **Abstract**: A power amplifier module and corresponding system are disclosed for linearising the output from a power amplifier. Both a feedback system, containing a compensator and the power amplifier in a feedback loop, and a pre-distortion compensation system injecting pre-distortion signals into or before the feedback system are used to compensate for non-linearities in the overall system. The pre-distortion signals may be mixed with signals from the compensator or may be filtered to take into account the loop compensator transfer function of the feedback loop, mixed with baseband signals and then converted into analog signals that are provided to the feedback loop. In modules containing a tracking power supply, an envelope calculator calculates an RF envelope of the baseband signals, which the pre-distortion system uses in conjunction with the baseband signals to generate the pre-distortion signals mixed with the signals from the compensator.

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CLAIMS

1. A power amplifier module comprising:

a feedback system containing a compensator and a power amplifier in a feedback loop, wherein the feedback system is an analog system in which signals passing through components in the feedback system are analog signals; and

a pre-distortion compensation system compensating for signals in cooperation with the feedback system, the pre-distortion compensation system injecting pre-distortion signals into the feedback system, the pre-distortion signals compensating for non-linearity of the power amplifier.

2. The power amplifier module of claim 1, wherein the pre-distortion system is a digital system in which all signals passing through components in the pre-distortion system are analog signals, the power amplifier module further comprising a D/A converter for all signals passing between the feedback system and the pre-distortion system.

3. The power amplifier module of claim 2, further comprising a baseband generator generating quadrature reference signals, wherein:

the feedback loop comprises:

first combiners to which demodulated quadrature signals sampled from an antenna are supplied,

loop compensators connected to the first combiners such that signals from the first combiners are supplied to the loop compensators, the loop compensators shaping a loop gain of the feedback loop, and

second combiners; and

the pre-distortion compensation system comprises error tables connected with the baseband generator, the error tables providing estimated error signals based on the quadrature reference signals and that compensate for the power amplifier non-linearity, the error tables connected with the second combiners.

4. The power amplifier module of claim 3, wherein:

the second combiners are connected to the loop compensators such that signals from the loop compensators are supplied to the second combiners, and

analog signals dependent on the digital estimated error signals are supplied to the second combiners.

5. The power amplifier module of claim 4, wherein the baseband generator comprises an envelope calculator that calculates an RF envelope of the quadrature reference signals, the power amplifier module further comprising a tracking power supply connected to the baseband generator to which the RF envelope is supplied, the tracking power supply connected to the power amplifier, the tracking power supply providing a supply voltage that depends on the RF envelope to the power amplifier.

6. The power amplifier module of claim 5, wherein the power amplifier module further comprises a tracking power supply model filtering the RF envelope and supplying the filtered RF envelope to the error tables, the estimated error signals based on the filtered RF envelope in addition to the quadrature reference signals.

7. The power amplifier module of claim 3, the pre-distortion system further comprises a filter disposed between each error table and corresponding second combiner, the filter filtering the estimated error signal to provide an inversion of a loop compensator transfer function of the feedback loop, wherein the second combiners are connected between the baseband generator and the first combiners, the second combiners connected with the filter such that signals from the baseband generator and signals from the filter are supplied to the second combiners.

8. A method of providing linearisation for a power amplifier, the method comprising:

providing feedback using a feedback loop to partially compensate for non-linearity of the power amplifier wherein signals passing through components in the feedback loop are analog signals; and

providing pre-distortion to additionally compensate for the non-linearity of the power amplifier in cooperation with the feedback, the pre-distortion injecting pre-distortion signals into the feedback loop.

9. The method of claim 8, further comprising converting signals from digital signals to analog signals such that the signals provided with the pre-distortion are digital and the signals provided with the feedback are analog.

10. The method of claim 9, wherein providing the pre-distortion comprises providing estimated error signals based on reference signals, analog conversions of the estimated error signals being supplied to combiners in the feedback loop connected to loop compensators in the feedback loop.

11. The method of claim 10, further comprising:

calculating an RF envelope of the reference signals; and

providing a supply voltage to the power amplifier that depends on the RF envelope.

12. The method of claim 11, further comprising filtering the RF envelope and supplying the filtered RF envelope to error tables that provide the estimated error signals such that the estimated error signals are based on the filtered RF envelope in addition to the reference signals.

13. The method of claim 9, further comprising filtering the estimated error signal to provide an inversion of a loop compensator transfer function of the feedback loop, and providing the pre-distortion comprising providing reference signals and the inversion to combiners prior to converting signals from the combiners into analog signals.

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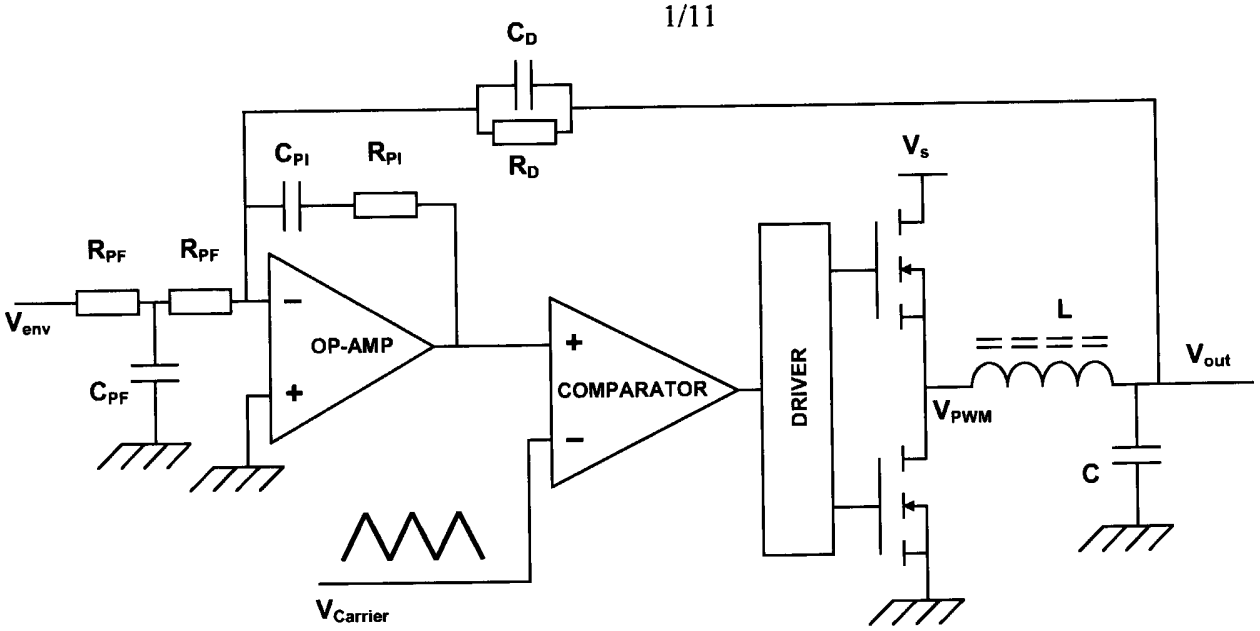

FIG. 1
(Prior Art)

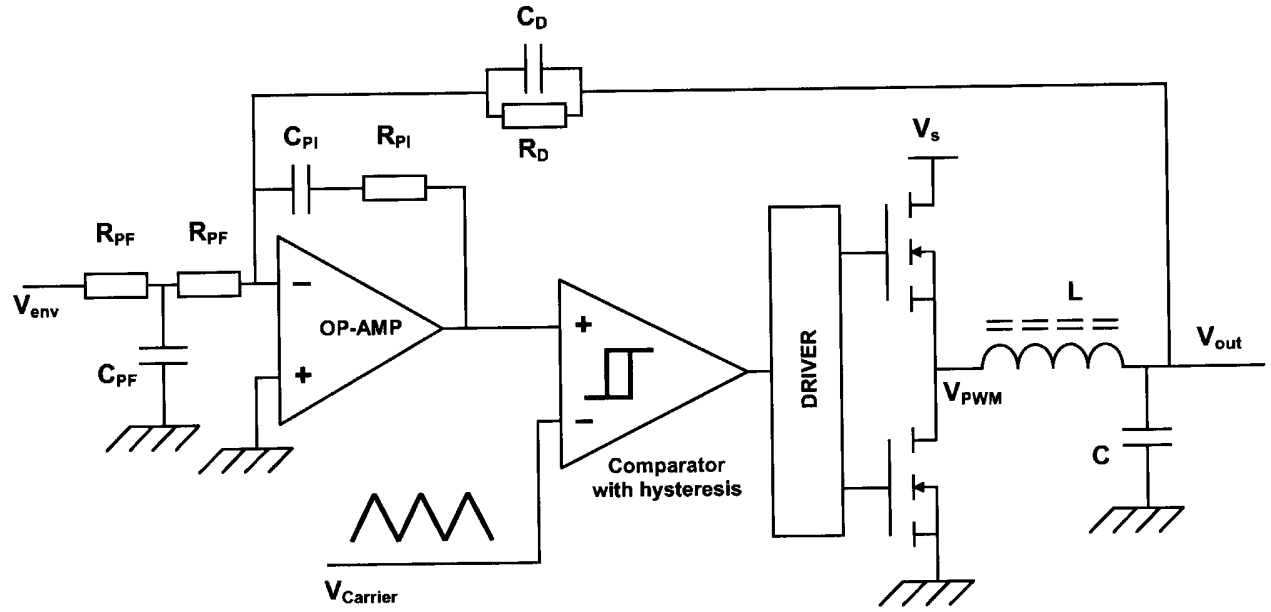

FIG. 2
(Prior Art)

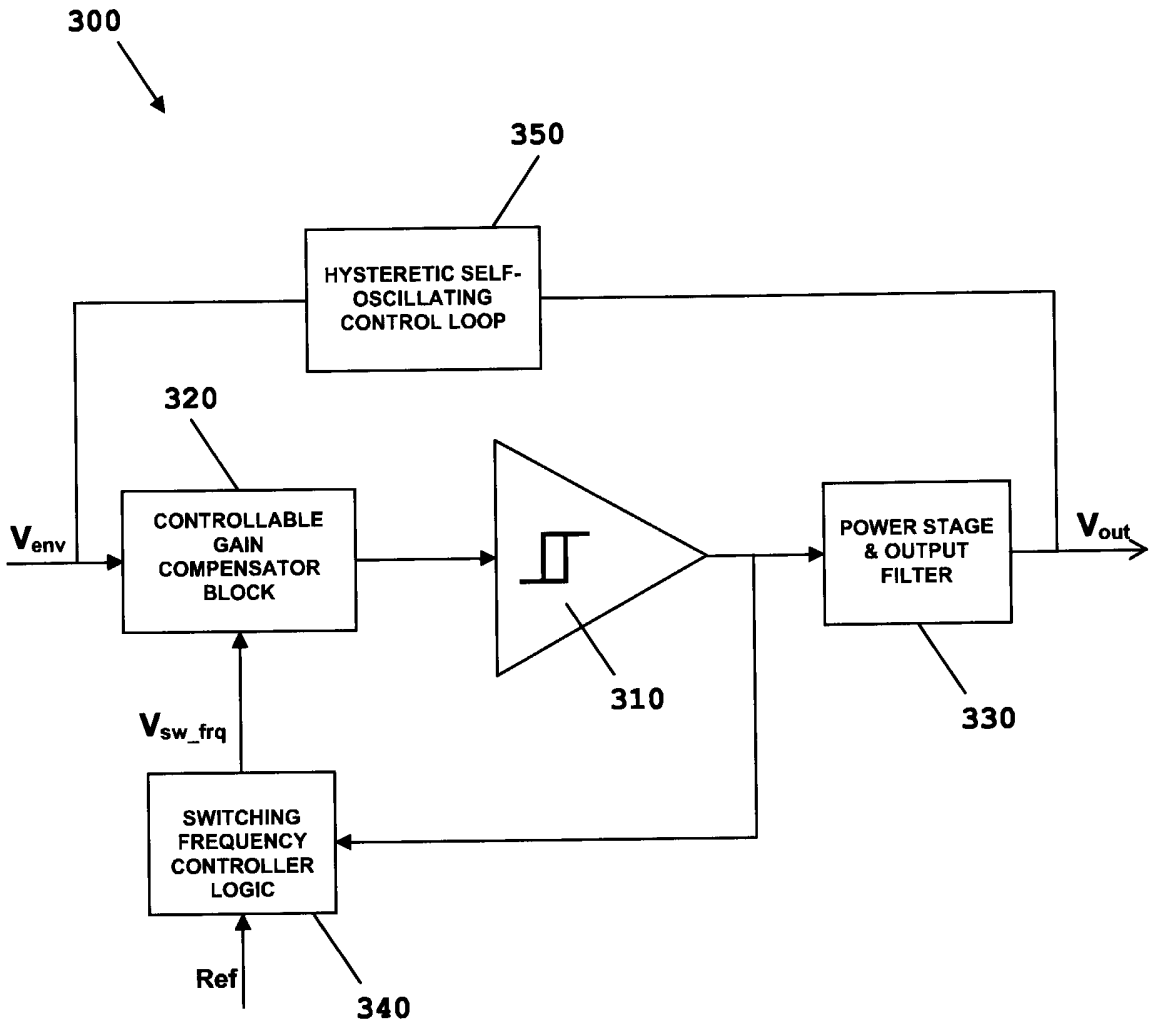
300
350
HYSTERETIC SELF-OSCILLATING CONTROL LOOP
320
CONTROLLABLE GAIN COMPENSATOR BLOCK
V_{env}
310
POWER STAGE & OUTPUT FILTER
V_{out}
330
V_{sw_frq}
SWITCHING FREQUENCY CONTROLLER LOGIC
Ref
340

FIG. 3

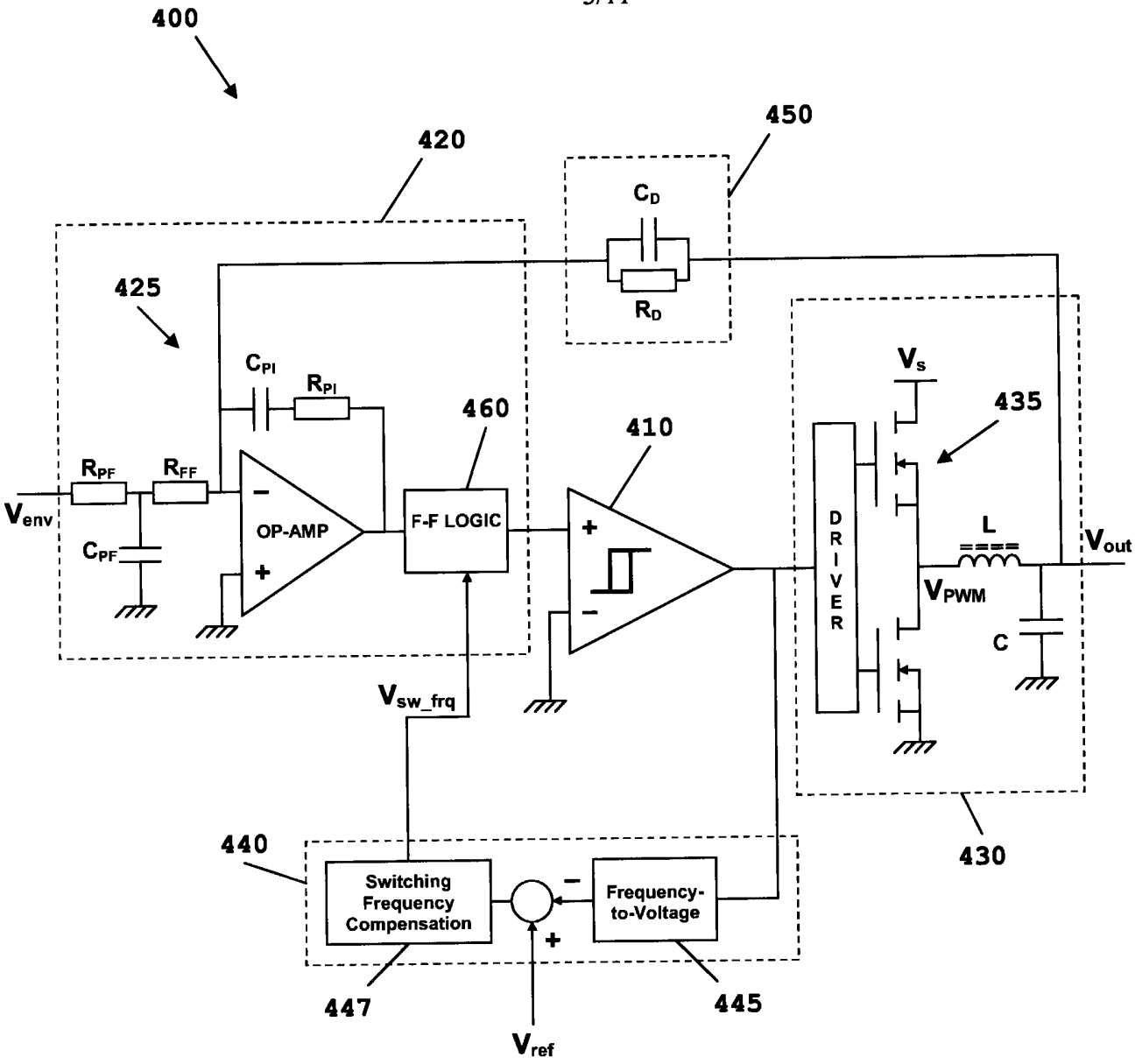
400
420
450
425
C_D
R_D
C_{PI}
R_{PI}
460
410
V_s
435
R_{PF}
R_{FF}
V_{env}
OP-AMP
F-F LOGIC
DRIVER
L
V_{out}
C_{PF}
V_{PWM}
C
V_{sw_frq}
440
Switching Frequency Compensation
Frequency-to-Voltage
430
447
445
V_{ref}

FIG. 4

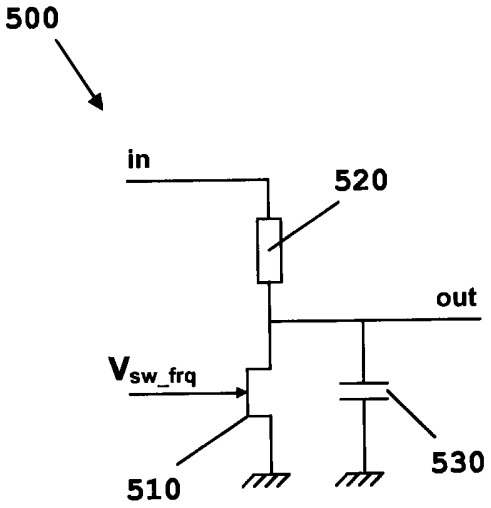

FIG. 5

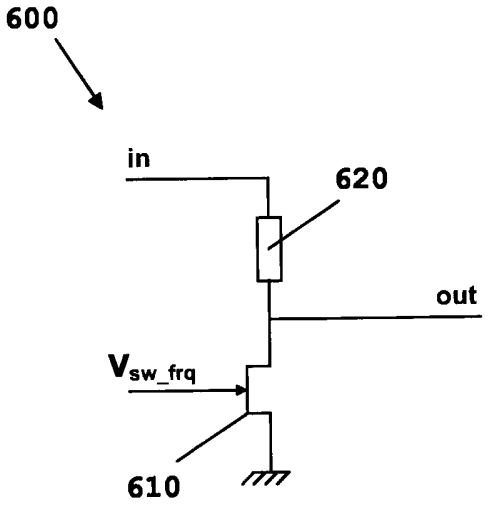

FIG. 6

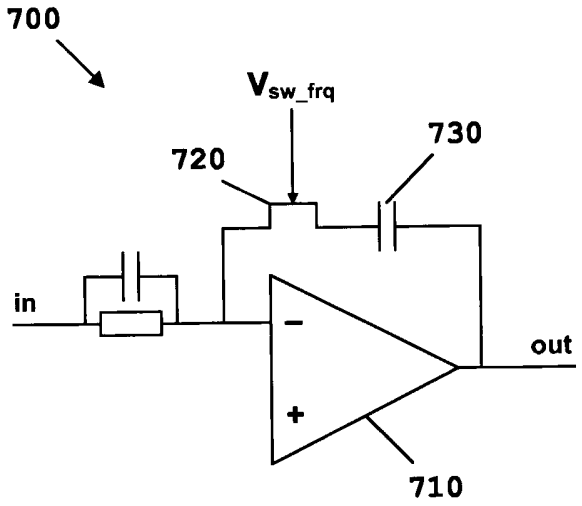

FIG. 7

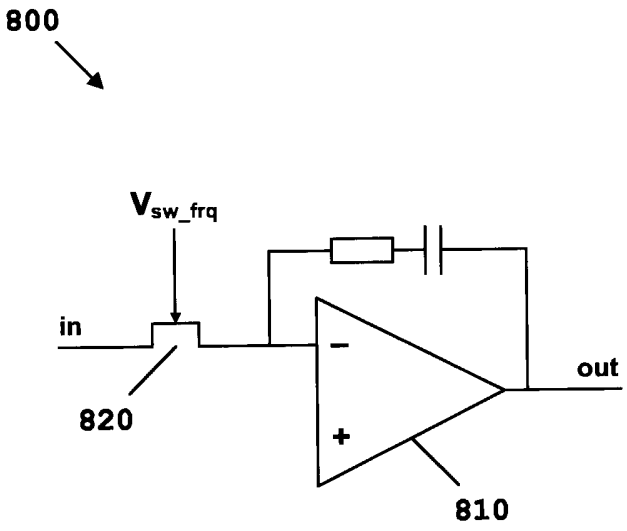

FIG. 8

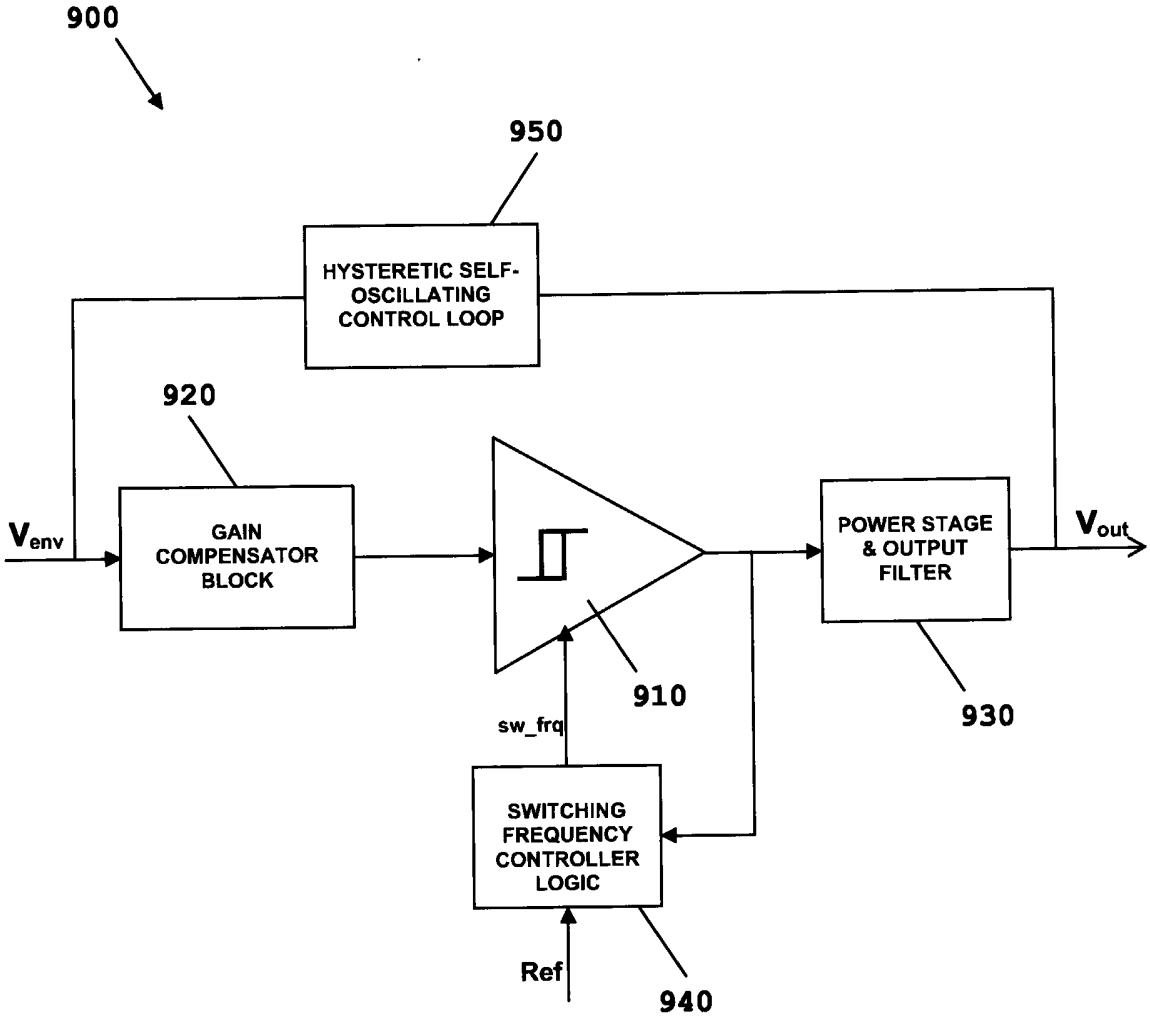
900
950
HYSTERETIC SELF-OSCILLATING CONTROL LOOP
920
V_{env}
GAIN COMPENSATOR BLOCK
910
POWER STAGE & OUTPUT FILTER
V_{out}
930
sw_frq
SWITCHING FREQUENCY CONTROLLER LOGIC
Ref
940

FIG. 9

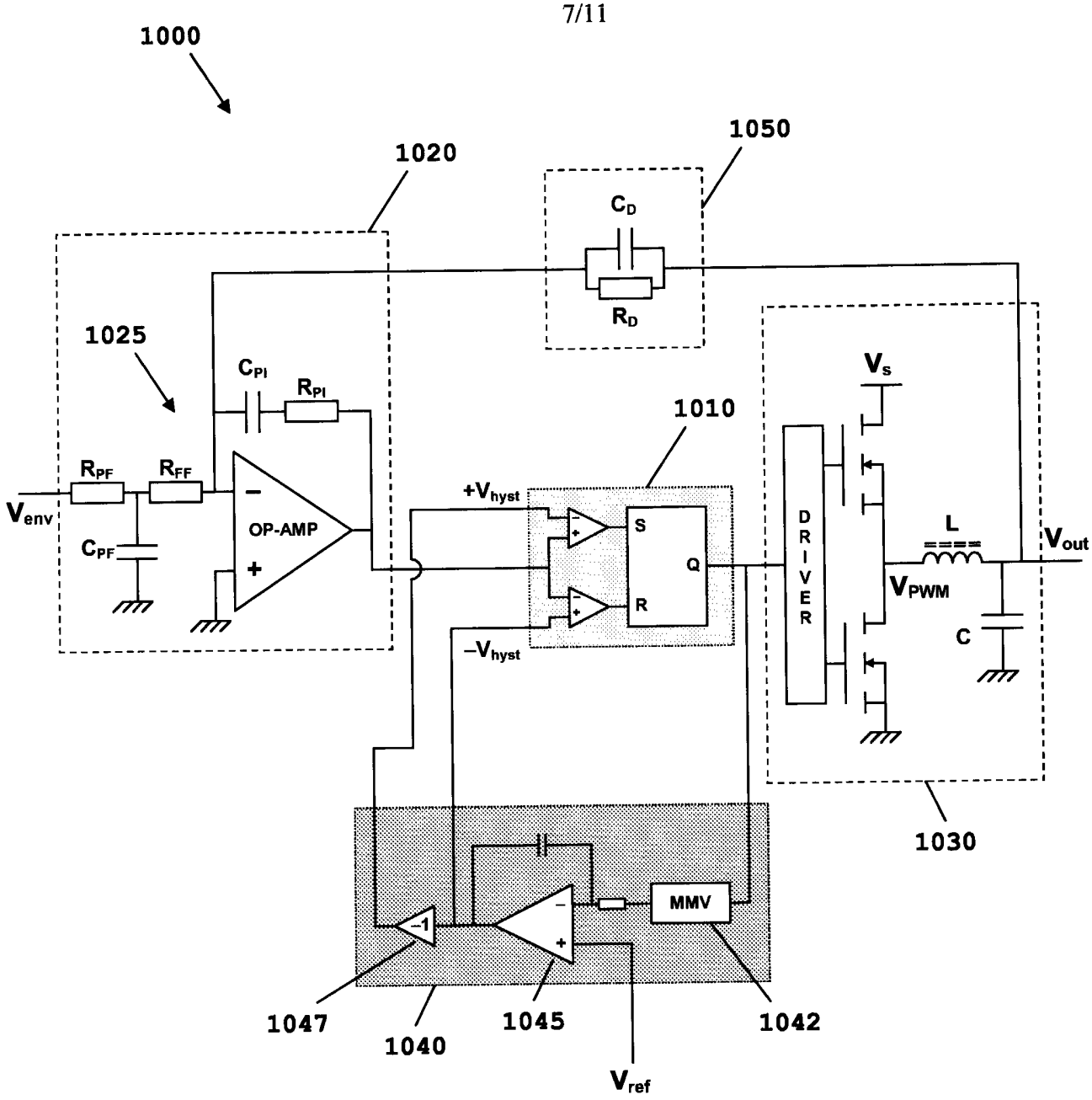
1000
1020
1050
C_D
R_D
1025
C_{PI}
R_{PI}
1010
R_{PF}
R_{FF}
V_{env}
C_{PF}
OP-AMP
$+V_{hyst}$
$-V_{hyst}$
S
Q
R
V_s
DRIVER
L
V_{out}
V_{PWM}
C
1030
MMV
-1
1047
1040
1045
1042
V_{ref}

FIG. 10

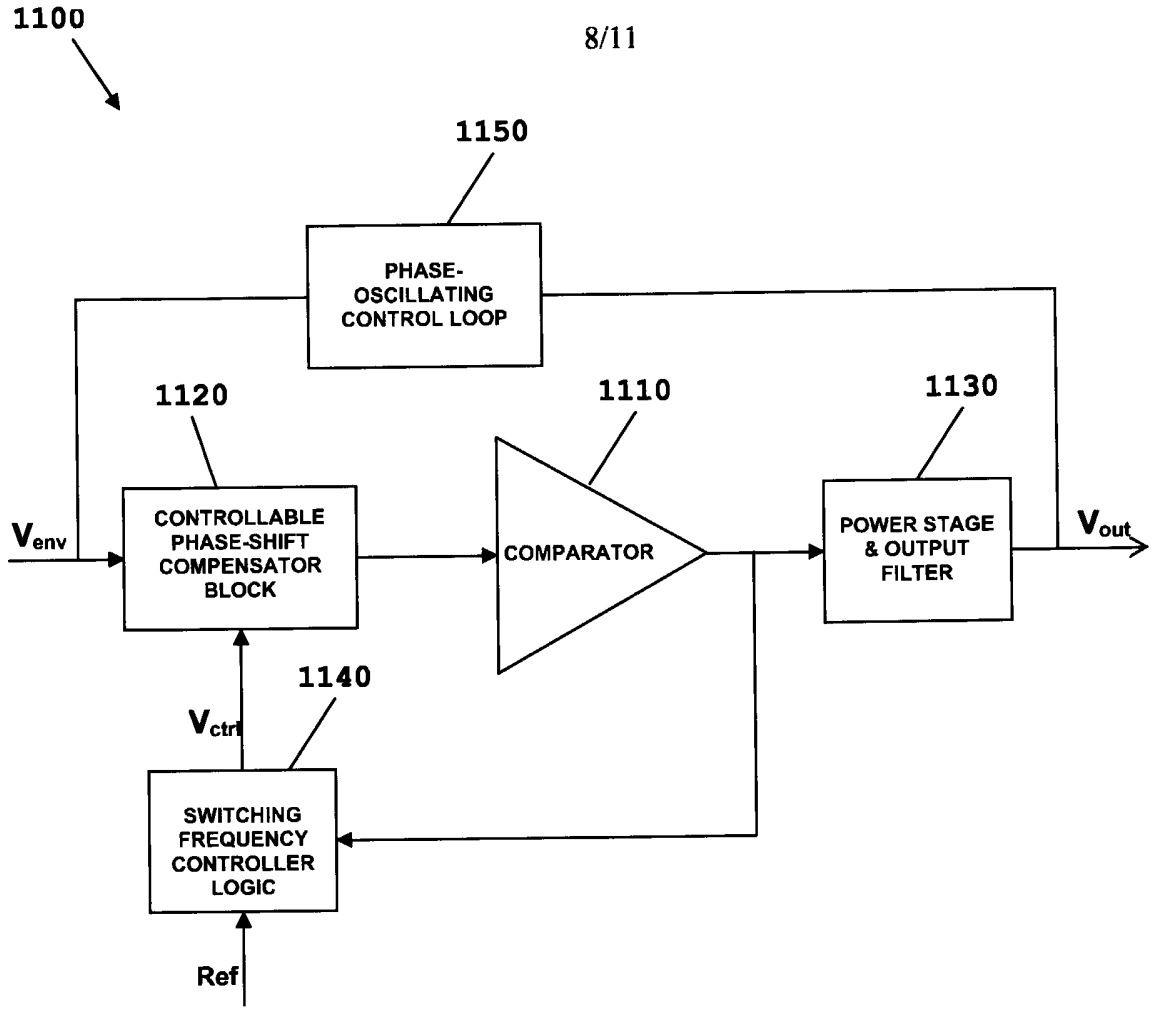
1100
1150
PHASE-OSCILLATING CONTROL LOOP
1120
1110
1130
V_{env}
CONTROLLABLE PHASE-SHIFT COMPENSATOR BLOCK
COMPARATOR
POWER STAGE & OUTPUT FILTER
V_{out}
1140
V_{ctrl}
SWITCHING FREQUENCY CONTROLLER LOGIC
Ref

FIG. 11

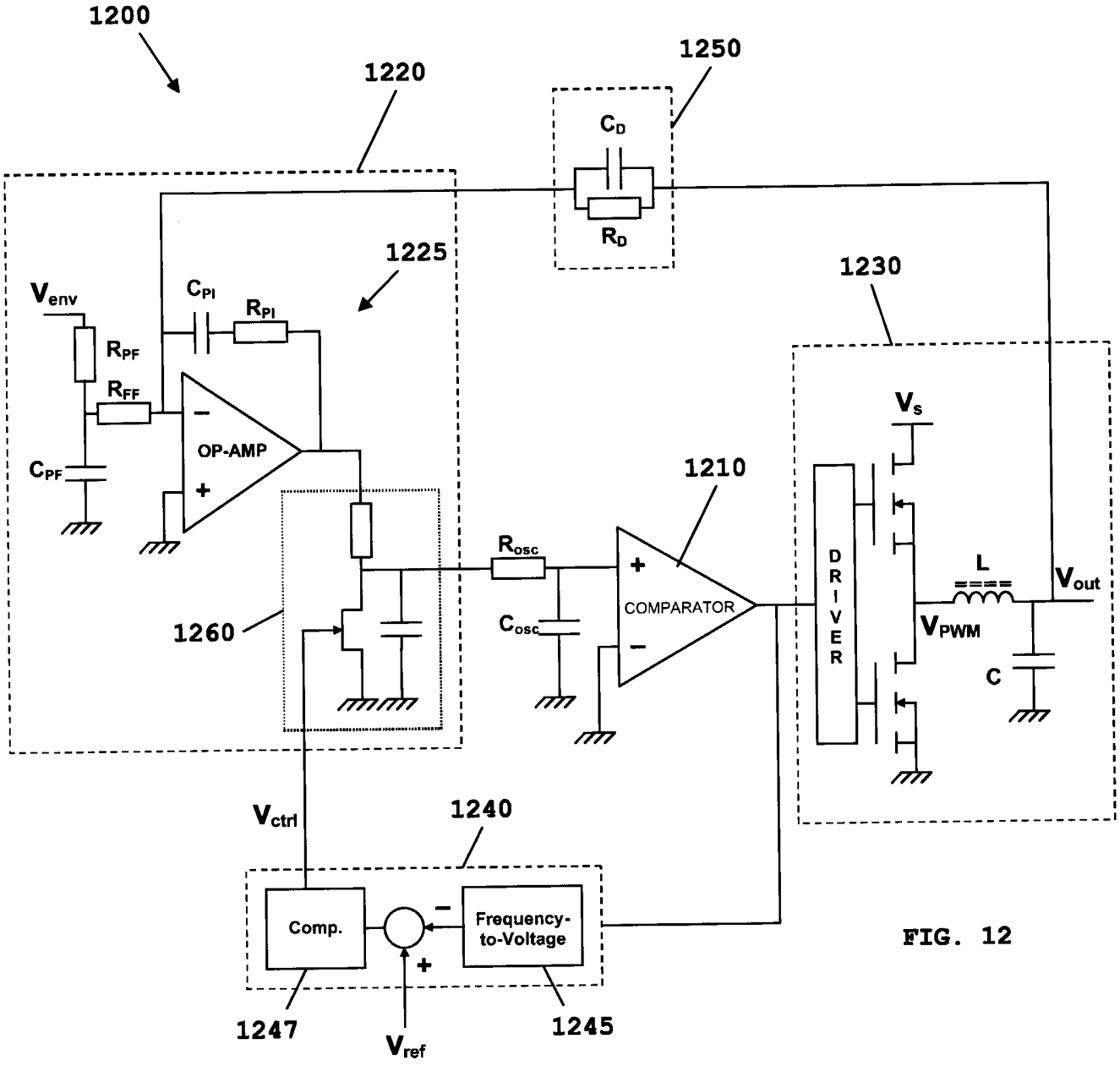
1200
1220
1250
C_D
R_D
1225
1230
V_{env}
C_{PI}
R_{PI}
R_{PF}
R_{FF}
OP-AMP
C_{PF}
V_s
1210
R_{osc}
COMPARATOR
DRIVER
L
V_{out}
V_{PWM}
C
1260
C_{osc}
V_{ctrl}
1240
Comp.
Frequency-to-Voltage
1247
V_{ref}
1245

FIG. 12

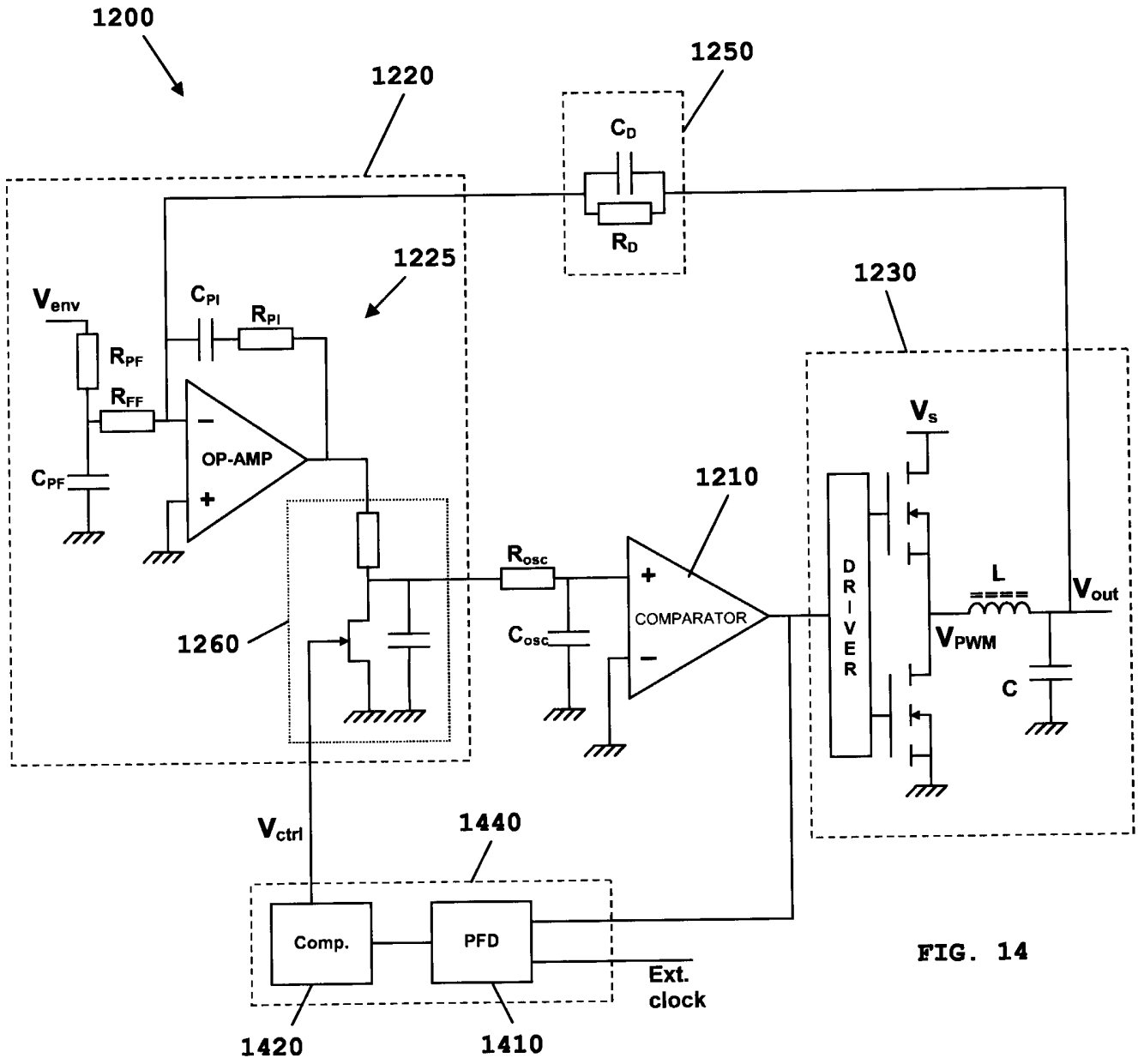
1200
1220
1250
C_D
R_D
1225
1230
V_{env}
C_{PI}
R_{PI}
R_{PF}
R_{FF}
OP-AMP
C_{PF}
V_s
1210
R_{osc}
COMPARATOR
DRIVER
L
V_{out}
V_{PWM}
C
1260
C_{osc}
V_{ctrl}
1440
Comp.
PFD
Ext. clock
1420
1410

FIG. 14

POWER SUPPLY CONTROLLER CIRCUITRY

TECHNICAL FIELD

The technical field relates generally to power supply controller circuitry, and more particularly to power supply controller circuitry for ultra-fast tracking power supplies.

BACKGROUND

In the field of digital radio systems, for example the TErrestrial Trunked Radio (TETRA) system, developed by the European Telecommunications Standards Institute (ETSI), and defined by a plurality of ETSI Standards, including the ETS 300-39x technical specification series, and the more recent TETRA 2 system, defined in the draft for release 2 of the TETRA specifications, it is desirable to control the voltage or current supply to the transmitter power amplifier (PA). In this manner, by use of a controller to dynamically set the applied voltage or current to the PA, the output power level of the PA may be adjusted to correspond more closely to the required instantaneous output power level in order to maximize the PA efficiency.

To this end, an Ultra-Fast Tracking Power Supply (UFTPS) is typically required for generating a rapidly varying PA supply voltage, whilst not wasting power itself. The requirements for such a UFTPS include:

(i) UFTPS power losses should be low enough for an overall system power saving to be realized, and as such must use switch-mode technology;

(ii) the output voltage must respond quickly to reference changes (ideally at a rate equivalent to the transmitted radio frequency (RF) signal bandwidth, for example 25-150kHz according to TETRA 2 specifications);

(iii) the output ripple voltage, which is a feature of switch-mode power converters, must be low enough to avoid RF pollution when it inter-modulates with the transmitted RF signal (for example in a range of 5 – 50mVpp);

(iv) electromagnetic fields emitted from the UFTPS should be configured to not interfere with the PA output spectrum; and

(v) the output impedance of the UFTPS must be sufficiently low, from DC to the RF bandwidth, in order to produce a relatively 'stiff' supply voltage for the PA (for example in a region of 10 – 100mΩ for high power wireless transmission units).

In effect, the UFTPS is required to act as a low-dissipation, low-electromagnetic interference (EMI) controllable voltage source, from DC to the RF bandwidth, and as such must achieve an acceptable compromise between output impedance and ripple voltage.

FIG. 1 illustrates an example of a known UFTPS circuit using a standard clocked pulse width modulator and a proportional-integral-derivative compensator (PWM/PID) voltage-mode control scheme. Such known solutions are based on having a signal that is external to the control loop ($V_{Carrier}$) generating the high-frequency dynamics necessary to make the control loop switch output voltage levels.

For these types of solution, it is necessary to limit the control loop bandwidth, or more precisely the crossover frequency, in order to avoid instabilities caused when the slope of ripple on the PWM input exceeds the slope of the carrier. Typically, a loop crossover frequency of less than a quarter of the switching frequency is necessary to avoid this form of instability.

Typically the control loop bandwidth is required to be limited to between three to ten times less than the switching frequency. Since the control loop is instrumental in reducing the output impedance of the UFTPS, as well as providing a fast response, this limitation of control loop bandwidth results in increased output impedance and/or response speed of the power supply. This is particularly the case when the switching frequency is outside of the control loop bandwidth.

FIG. 2 illustrates a different class of known control system, in which the UFTPS uses a hysteretic self-oscillating PID voltage-mode control scheme. In this solution, no external signal is required to produce the switching. It is noteworthy that Vcarrier now refers to the output of the compensation circuitry, reflecting the common notion that 'a hysteretic controller generates its own carrier signal'. Instead, a purposefully introduced instability in the control loop is used. This fundamentally (according to the well-established Barkhausen criteria for oscillation) leads to a

control loop bandwidth (crossover frequency) that is equal to the switching frequency. In the hysteretic self-oscillating controller, the instability is caused by the presence of hysteresis, as also exploited in common triangle-wave oscillator circuits. In this manner, the loop gain can be increased by a factor of between three to ten times over traditional solutions, such as that illustrated in FIG. 1.

A problem with the type of solution illustrated in FIG. 2 is that the switching (oscillation) frequency will vary with the duty ratio of the generated PWM signal, resulting in a variable ripple voltage at the output of the UFTPS. Since the UFTPS will generally be required to maintain a maximum output ripple voltage, the variation in the switching frequency is undesirable, and is particularly problematic when the UFTPS is fitted with a higher-order output filter. This problem is primarily due to the attenuation of a higher-order filter changing dramatically with frequency (compared to a second-order filter). As an example, a UFTPS with a 4^{th} order filter would have its ripple increase by 24dB (a factor of around '16') if the switching frequency were halved. This would commonly happen for a normal hysteretic controller in the UFTPS application, where the output voltage range is large.

Thus, there exists a need for power supply controller circuitry, an integrated circuit and a communication unit, which addresses at least some of the shortcomings of past and present power supply controller circuits.

BRIEF DESCRIPTION OF THE FIGURES

The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views, which together with the detailed description below are incorporated in and form part of the specification and serve to further illustrate various embodiments of concepts that include the claimed invention, and to explain various principles and advantages of those embodiments.

FIG. 1 illustrates an example of a known UFTPS control system.

FIG. 2 illustrates an alternative example of a known UFTPS control system.

FIG. 3 illustrates a power supply controller circuit according to some embodiments.

FIG. 4 illustrates an example of a power supply controller circuit in accordance with the embodiment of FIG. 3.

FIG. 5 illustrates feed-forward block according to an embodiment.

FIG. 6 illustrates feed-forward block according to an alternative embodiment.

FIG. 7 illustrates feed-forward block according to a further alternative embodiment.

FIG. 8 illustrates feed-forward block according to a still further alternative embodiment.

FIG. 9 illustrates a power supply controller circuit according to an alternative embodiment.

FIG. 10 illustrates an example of a power supply controller circuit in accordance with the embodiment of FIG. 9.

FIG. 11 illustrates a power supply controller circuit according to an alternative embodiment.

FIG. 12 illustrates an example of a power supply controller circuit in accordance with the embodiment of FIG. 11.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of various embodiments. In addition, the description and drawings do not necessarily require the order illustrated. Apparatus and method components have been represented where appropriate by conventional symbols in the drawings, showing only those specific details that are pertinent to understanding the various embodiments so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein. Thus, it will be appreciated that for simplicity and clarity of illustration, common and well-understood elements that are useful or necessary in a commercially feasible embodiment may not be depicted in order to facilitate a less obstructed view of these various embodiments.

DETAILED DESCRIPTION

Generally speaking, pursuant to the various embodiments, there is provided a power supply controller circuit comprising oscillation circuitry, compensation circuitry arranged to provide a compensated control signal to the oscillation circuitry, and power converter circuitry operably coupled to an output of the oscillation

circuitry. The power supply controller circuitry further comprises switching frequency controller logic, arranged to control the switching frequency of the power supply controller circuitry based on at least switching frequency feedback from the output of the oscillation circuitry.

In this manner, a known problem of a varying output ripple voltage, caused by the switching frequency varying with a duty ratio of an output of the oscillation circuitry, may be substantially alleviated, whilst providing increased control loop bandwidth afforded by a self-oscillating switch-mode power supply controller.

Those skilled in the art will realise that the above recognised advantages and other advantages described herein are merely illustrative and are not meant to be a complete rendering of all of the advantages of the various embodiments.

Referring now to the drawings, and in particular FIG. 3, power supply controller circuitry in accordance with some embodiments is shown and indicated generally at 300. The power supply controller circuitry 300 comprises oscillation circuitry 310, compensation circuitry 320 arranged to provide a compensated control signal to the oscillation circuitry 310, and power converter circuitry 330 operably coupled to an output of the oscillation circuitry 310. For the illustrated embodiment, the oscillation circuitry 310 comprises a hysteretic self-oscillating comparator.

Those skilled in the art, however, will recognise and appreciate that the specifics of this example are merely illustrative of some embodiments and that the teachings set forth herein are applicable in a variety of alternative settings. For example, since the teachings described do not depend on a hysteretic self-oscillating control scheme, they can be applied to any type of oscillating control scheme, although a hysteretic self-oscillating control scheme is shown in this embodiment. As such, other alternative implementations using different types of oscillation circuitry are contemplated and are considered to be within the scope of the various teachings described. For example, in a phase-shift self-oscillating controller, the phase shift network may be made variable, similarly providing control over the switching frequency. This is because the phase-shift self-oscillating control loop will oscillate at the point where the total phase lag through the entire loop is -360°.

For the embodiment illustrated in FIG. 3, the compensation circuitry 320 comprises controllable gain compensation circuitry, and receives as an input a required output envelope voltage signal (V_{env}), and control loop feedback from the

output of the power converter circuitry 330, via control loop feedback circuitry 350. The required output envelope voltage signal (V_{env}) and the control loop feedback may be added together, or otherwise processed, to produce an error signal.

The compensation circuitry 320 is operably coupled to the output of the oscillation circuitry 310 via switching frequency controller logic 340. The switching frequency controller logic 340 generates a switching frequency control signal ($V_{sw\ frq}$), based on the output of the oscillation circuitry 310 and, for the illustrated embodiment, a reference signal (Ref). This switching frequency control signal ($V_{sw\ frq}$) is provided to the compensation circuitry 320. For clarity, the switching frequency refers to the oscillating frequency of the output signal from the oscillation circuitry 310.

The compensation circuitry 320 generates the compensated control signal based on the error signal, from the required output envelope voltage signal (V_{env}) and the control loop feedback, and the switching frequency control signal ($V_{sw\ frq}$). In particular, the compensated control signal is generated to compensate for any discrepancy between the required output and the actual output from the power converter circuitry, whilst also compensating for variation of switching frequency, such that the switching (oscillating) frequency of the output signal from the oscillation circuitry 310 remains substantially constant, or at least within a predetermined range.

As will be appreciated by a skilled artisan, the oscillation circuitry 310 provides a switching signal to the power converter circuitry 330, based on the compensated control signal from the compensation circuitry 320 and the switching signal driving the power converter circuitry 330. Accordingly, by compensating for a variation of switching frequency in the aforementioned manner, and thereby maintaining a substantially constant switching signal, or at least a switching signal with a frequency within a predetermined range, output voltage ripple from the power converter circuit 330 remains substantially constant, or at least within a predetermined range. In this manner, the output voltage ripple of the power supply controller circuit 300 may be maintained below a maximum level, as defined by, for example, design considerations of a load to which power is to be supplied by the power supply controller circuit 300.

Referring now to FIG. 4, there is illustrated an example of a power supply controller circuit 400 in accordance with the embodiment of FIG. 3. The power

supply controller circuit 400 comprises oscillation circuitry, in a form of hysteretic comparator 410, compensation circuitry 420 arranged to provide a compensated control signal to comparator 410, and power converter circuitry 330 operably coupled to an output of hysteretic self-oscillating comparator 410.

For the embodiment illustrated in FIG. 4, the compensation circuitry 420 comprises Proportional-Integral-Derivative (PID) controller circuitry 425 and feed-forward block 460. The PID controller circuitry 425 receives, as an input, a required output envelope voltage signal (V_{env}), and control loop feedback from the output of the power converter circuitry 430, via control loop feedback circuitry 450. The PID controller circuitry 425 produces an error signal from the required output envelope voltage signal (V_{env}) and the control loop feedback, which is provided to the feed-forward block 460.

The compensation circuitry 420, and more particularly for the illustrated embodiment the feed-forward block 460, is operably coupled to the output of the hysteretic self-oscillating comparator 410, via switching frequency controller logic 440. The switching frequency controller logic 440 comprises frequency-to-voltage conversion logic 445, which receives the output signal from the comparator 410, and converts the switching (oscillating) frequency of the received signal into a voltage value representing the switching frequency. The voltage value is then provided to switching frequency compensation circuitry 447, along with a switching frequency reference signal (V_{ref}). In response thereto, the switching frequency compensation circuitry 447 generates a switching frequency control signal (V_{sw_frq}), which is provided to the compensation circuitry 420, and more particularly for the illustrated embodiment the feed-forward block 460.

The feed-forward block 460 generates the compensated control signal based on the error signal from the PID controller circuitry 425 and the switching frequency control signal ($V_{sw\ frq}$). The compensated control signal is provided to the hysteretic self-oscillating comparator 410. The hysteretic self-oscillating comparator 410 provides a switching signal to the power converter circuitry 430, based on the compensated control signal from the compensation circuitry 420, the switching signal driving the power converter circuitry 430.

For the embodiment illustrated in FIG. 4, the power converter circuitry 430 comprises a switched mode power converter, such as a buck converter power stage

435, which generates a Pulse Width Modulated (PWM) signal (V_{PWM}). The power converter circuitry further comprises an output LC filter, and in one embodiment a 2nd or higher order LC filter, for example a low-pass 4th order LC filter, which filters the PWM signal to produce an output signal (V_{out}) for the power supply controller circuitry 400.

Referring now to FIG. 5, there is illustrated feed-forward block 500 according to an embodiment. The feed-forward block 500 comprises a transistor, such as a junction gate field effect transistor (JFET) 510, which functions as a voltage-controlled resistor. The JFET 510 is operably coupled in series between a resistor 520 and ground, and as such forms a part of a voltage divider circuit with the resistor 520. Feed-forward block 500 further comprises a capacitor 530, operably coupled in parallel with the JFET 510. As will be appreciated by a skilled artisan, varying V_{sw_frq} produces a variable voltage division ratio across the resistor 520 and JFET 510, as well as a variable pole location, since the circuit time constant is set by the parallel value of the resistances of the JFET 510 and resistor 520 and the value of capacitor 530.

Referring now to FIG. 6, there is illustrated feed-forward block 600 according to an alternative embodiment. As will be appreciated by a skilled artisan, the feed-forward block 600 of FIG. 6 is a simplified version of the feed-forward block of FIG. 5, comprising a JFET 610 operably coupled in series between a resistor 620 and ground.

Referring now to FIG. 7, there is illustrated feed-forward block 700 according to a further alternative embodiment. The feed-forward block 700 comprises a PID compensator 710. A JFET 720, functioning as a voltage-controlled resistor, is provided in series with a capacitor 730 to produce a zero at a variable frequency. Functionally, this means that the high-frequency gain of the block can be controlled via the JFET gate. This, in turn (in a hysteretic self-oscillating controller), provides control over the carrier signal slope and, thus, the switching frequency of the loop.

Referring now to FIG. 8, there is illustrated feed-forward block 800 according to a still further alternative embodiment. The feed-forward block 800 comprises a PID compensator 810. A JFET 820, functioning as a voltage-controlled resistor, is provided as an input resistor for the PID compensator 810, thereby producing a variable gain for the PID compensator 810.

Referring now to FIG. 9, there is illustrated a power supply controller circuit 900 according to an alternative embodiment. The power supply controller circuit 900 comprises oscillation circuitry 910, in a form of a hysteretic self-oscillating comparator. The power supply controller circuit 900 further comprises compensation circuitry 920, and power converter circuitry 930 operably coupled to an output of the hysteretic self-oscillating circuitry 910.

The compensation circuitry 920 comprises gain compensation circuitry, and receives as an input a required output envelope voltage signal (V_{env}), and control loop feedback from an output of the power converter circuitry 930, via control loop feedback circuitry 950. The required output envelope voltage signal (V_{env}) and the control loop feedback may be added together, or otherwise processed, to produce an error signal.

The power supply controller circuit 900 further comprises switching frequency controller logic 940, arranged to control the switching frequency of the power supply controller circuitry 900 based on switching frequency feedback from the output of the hysteretic self-oscillating circuitry 910. In particular, the switching frequency compensation circuitry 940 generates a switching frequency control signal (sw_frq), based on an output of the hysteretic self-oscillating circuitry 910 and a reference signal (Ref). For the embodiment illustrated in FIG. 9, the switching frequency controller logic 940 provides the switching frequency control signal (sw_frq) to the hysteretic self-oscillating circuitry 910.

In this manner, the hysteretic self-oscillating circuitry 910 provides a switching signal to the power converter circuitry 930, based on the compensated control signal from the compensation circuitry 920, and having a switching (oscillating) frequency based on the switching frequency control signal (sw_frq) from the switching frequency controller logic 940.

Referring now to FIG. 10, there is illustrated an example of power supply controller circuit 1000 in accordance with the embodiment of FIG. 9. The power supply controller circuit 1000 comprises oscillation circuitry, again in a form of hysteretic self-oscillating comparator 1010, compensation circuitry 1020 arranged to provide a compensated control signal to hysteretic self-oscillating comparator 1010, and power converter circuitry 1030 operably coupled to an output of hysteretic self-oscillating comparator 1010.

For the embodiment illustrated in FIG. 10, the compensation circuitry 1020 comprises PID controller circuitry 1025. The PID controller circuitry 1025 receives as an input a required output envelope voltage signal (V_{env}), and control loop feedback from the output of the power converter circuitry 1030, via control loop feedback circuit 1050. The PID controller circuitry 1025 produces an error signal from the required output envelope voltage signal (V_{env}) and the control loop feedback, which is provided to the hysteretic self-oscillating comparator 1010.

The power supply controller circuit 1000 further comprises switching frequency controller logic 1040, operably coupled to the output of the hysteretic self-oscillating comparator 1010. The switching frequency controller logic 1040 comprises a Monostable Multi-Vibrator (MMV) 1042, which receives, as an input, the output signal from the hysteretic self-oscillating comparator 1010. The MMV 1042 generates a square or rectangular wave signal representative of the switching frequency of the output of the hysteretic self-oscillating comparator 1010. The square or rectangular wave signal generated by the MMV 1042 is provided to an integrator 1045, along with a switching frequency reference signal (V_{ref}). The integrator 1045 generates a hysteretic and switching frequency control signal, which for the illustrated embodiment is provided to a first hysteretic input ($-V_{hyst}$) of comparator 1010. The hysteretic and switching frequency control signal is also inverted, by inverter 1047, and provided to a second hysteretic input ($+V_{hyst}$).

Functionally, this circuit ensures a hysteresis window where the positive and negative hysteresis thresholds change symmetrically (substantially avoiding errors being forced into the carrier signal DC operating point). The integrator ensures that the under steady-state conditions are substantially no different between the switching frequency reference signal (V_{ref}) and the average of the MMV output. Since the average MMV output is proportional to the actual switching frequency, this means that the converter switching frequency is determined by V_{ref}.

Referring now to FIG. 11, there is illustrated a power supply controller circuit 1100 according to an alternative embodiment. The power supply controller circuitry 1100 comprises oscillation circuit 1110, compensation circuitry 1120 arranged to provide a compensated control signal to the oscillation circuitry 1110, and power converter circuitry 1130 operably coupled to an output of the oscillation circuitry

1110. For the embodiment illustrated in FIG. 11, the oscillation circuitry 1110 comprises a comparator.

The compensation circuitry 1120 comprises controllable phase-shift compensation circuitry, and receives, as an input, a required output envelope voltage signal (V_{env}), and control loop feedback from the output of the power converter circuitry 1130, via control loop feedback circuitry 1150. The required output envelope voltage signal (V_{env}) and the control loop feedback may be added together, or otherwise processed, to produce an error signal.

The compensation circuitry 1120 is operably coupled to an output of the phase-shift-type self-oscillating circuitry 1110 via switching frequency controller logic 1140. The switching frequency controller logic 1140 generates a switching frequency control signal (V_{sw_frq}), based on the output of the phase-shift-type self-oscillating circuitry 1110 and, for the illustrated embodiment, a reference signal (Ref). This switching frequency control signal ($V_{sw\ frq}$) is provided to the compensation circuitry 1120.

The compensation circuitry 1120 generates the compensated control signal based on the error signal, from the required output envelope voltage signal (V_{env}) and the control loop feedback, and the switching frequency control signal ($V_{sw\ frq}$). In particular, the compensated control signal is generated to compensate for any discrepancy between the required output and the actual output from the power converter circuitry, whilst also compensating for a variation of switching frequency, such that the switching (oscillating) frequency of the output signal from the phase-shift-type self-oscillating circuitry 1110 remains substantially constant, or at least within a predetermined range.

Referring now to FIG. 12, there is illustrated an example of power supply controller circuit 1200 in accordance with the embodiment of FIG. 11. The power supply controller circuit 1200 comprises oscillation circuitry, in a form of a comparator 1210, compensation circuitry 1220 arranged to provide a compensated control signal to the comparator 1210, and power converter circuitry 1230 operably coupled to an output of the comparator 1210.

For the embodiment illustrated in FIG. 12, the compensation circuitry 1220 comprises PID controller circuitry 1225 and feed-forward block 1260. The PID controller circuitry 1225 receives, as an input, a required output envelope voltage

signal (V_{env}), and control loop feedback from an output of the power converter circuitry 1230, via control loop feedback circuitry 1250. The PID controller circuitry 1225 produces an error signal from the required output envelope voltage signal (V_{env}) and the control loop feedback, which is provided to the feed-forward block 1260.

The compensation circuitry 1220, and more particularly for the illustrated embodiment the feed-forward block 1260, is operably coupled to an output of the comparator 1210, via switching frequency controller logic 1240. The switching frequency controller logic 1240 comprises frequency-to-voltage conversion logic 1245, which receives the output signal from the comparator 1210, and converts the switching (oscillating) frequency of the received signal into a voltage value representing the switching frequency. The voltage value is then provided to the switching frequency compensation circuitry 1247, along with a switching frequency reference signal (V_{ref}). The switching frequency compensation circuitry 1247 generates a switching frequency control signal ($V_{sw\ frq}$), which is provided to the compensation circuitry 1220, and more particularly for the illustrated embodiment the feed-forward block 1260.

The feed-forward block 1260 generates the compensated control signal based on the error signal from the PID controller circuitry 1225 and the switching frequency control signal (V_{sw_frq}). The compensated control signal is provided to the comparator 1210. The comparator 1210 provides a switching signal to the power converter circuitry 1230, based on the compensated control signal from the compensation circuitry 1220 and the switching signal driving the power converter circuitry 1230.

The power supply controller circuits described herein, in accordance with various embodiments of the present invention, allow the switching frequency of self-oscillating power converters to be controlled, thereby substantially removing the inherent disadvantage of a variable switching frequency associated with known self-oscillating control solutions. Furthermore, the power supply controller circuits allow a simpler implementation of the hysteretic comparator, when compared to prior art solutions.

Referring now to FIG. 13, there is illustrated an example of a switching frequency reference signal (V_{ref}) source, for example a source suitable for the embodiment of FIG. 12. The V_{ref} source comprises a Phase Locked Loop (PLL) based frequency control, which for the example illustrated in FIG. 13, consists of a Phase-

Frequency Detector (PFD) 1310 and a PLL compensator 1320. As will be appreciated by a skilled artisan, a PFD is a device that compares the phase of two input signals, which for the illustrated embodiment is in a form of an output of the comparator 1210 and an external clock signal. An output of the PDF 1310 is provided to the PLL compensator 1320, which generates V_{ref}. The PLL compensator 1320 may comprise a PI compensator.

Referring now to FIG. 14, there is illustrated an example of the power supply controller circuit 1200 of FIG. 12 comprising an alternative switching frequency controller logic 1440. For the embodiment illustrated in FIG. 14, the frequency controller logic 1440 comprises a Phase Locked Loop (PLL) based frequency control, which consists of a Phase-Frequency Detector (PFD) 1410 and a PLL compensator 1420. The inputs of the PFD 1410 comprise the output of the comparator 1210 and an external clock signal. An output of the PDF 1410 is provided to the PLL compensator 1320, which generates V_{ref}. The PLL compensator 1320 may comprise a PI compensator.

For each of the embodiments of FIG's. 13 and 14, the PLL based frequency control synchronises the sensed switching frequency of the UFTPS (the output of the comparator 1210) with an externally provided reference clock. In particular, for the embodiment illustrated in FIG. 13, a nested frequency locked loop allows phase-accurate locking of the switching action of the self-oscillating converter to an external clock. As will be appreciated by a skilled artisan, the sensed switching frequency may be taken from other locations within the UFTPS, such as the PWM signal output of the power stage (Vpwm).

In the foregoing specification, specific embodiments have been described. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the invention as set forth in the claims below.

By way of example, switching frequency controller logic may comprise a digital signal processor or a phase locked loop circuit to phase-lock the PWM signal to an external clock. Furthermore, the power converter circuitry and compensation circuitry are not limited to those illustrated in the accompanying drawings or as described herein. For example, the power supply controller circuitry may comprise a power topology with a 4^{th} order LC filter, and a more elaborate feedback network.

Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present teachings. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. The invention is defined solely by the appended claims.

The power supply controller circuit as defined in the claims and as illustrated by the embodiments described herein may be may comprise a switched mode power converter such as a buck converter power stage.

The power supply controller circuit as defined in the claims and as illustrated by the embodiments described herein may be comprised in an integrated circuit.

CLAIMS

1. A power supply controller circuit comprising oscillation circuitry, compensation circuitry arranged to provide a compensated control signal to the oscillation circuitry, and power converter circuitry operably coupled to an output of the oscillation circuitry;

wherein the power supply controller circuit is characterised by switching frequency controller logic operably coupled to the compensation circuitry and arranged to control a switching frequency of the power supply controller circuit based on at least a switching frequency feedback signal from an output of the oscillation circuitry.

2. The power supply controller circuit of Claim 1 further characterised by the switching frequency controller logic being arranged to generate a switching frequency control signal, based on at least the output of the oscillation circuitry.

3. The power supply controller circuit of Claim 2 further characterised by the switching frequency controller logic being arranged to generate the switching frequency control signal based further on a reference signal.

4. The power supply controller circuit of Claim 3 further characterised by the switching frequency control signal being provided to the compensation circuitry, and the compensation circuitry generating the compensated control signal based at least on an error signal and the switching frequency control signal.

5. The power supply controller circuitry of Claim 4 further characterised by the compensation circuitry comprising feed-forward block arranged to generate the compensated control signal based on at least the switching frequency control signal.

6. The power supply controller circuit of Claim 5 further characterised in that the feed-forward block generates the compensated control signal based further on an error signal, the error signal being produced by the compensation circuitry from an output envelope voltage signal and control loop feedback.

7. The power supply controller circuit of Claim 5 or Claim 6 further characterised by the feed-forward block comprising a transistor arranged to function as a voltage-controlled resistor, and forming part of a voltage divider circuit.

8. The power supply controller circuit of Claim 5 or Claim 6 further characterised by the feed-forward block comprising a Proportional-Integral-Derivative compensator, and a transistor arranged to function as a voltage-controlled resistor, the transistor being provided in series with a capacitor to produce a zero at a variable frequency for the Proportional-Integral-Derivative compensator.

9. The power supply controller circuit of Claim 5 or Claim 6 further characterised by the feed-forward block comprising a Proportional-Integral-Derivative compensator, and a transistor arranged to function as a voltage-controlled resistor, the transistor being provided as an input resistor for the Proportional-Integral-Derivative compensator.

10. The power supply controller circuit of Claim 3 further characterised by the switching frequency control signal being provided to the oscillation circuitry, and the oscillation circuitry arranged to provide a switching signal to the power converter circuitry, based on the compensated control signal from the compensation circuitry.

11. The power supply controller circuit of any preceding claim further characterised by the switching frequency controller logic comprising frequency-to-voltage conversion logic and switching compensation circuitry.

12. The power supply controller circuit of Claim 11 wherein the frequency-to-voltage conversion logic receives the output signal from the oscillation circuitry and converts the switching frequency of the received signal into a voltage value representing the switching frequency.

13. The power supply controller circuit of Claim 12 wherein the voltage value is provided to the switching frequency compensation circuitry, together with a switching

frequency reference signal, which together generate a switching frequency control signal.

14. The power supply controller circuit of any preceding claim further characterised by the switching frequency controller logic comprising a Monostable Multi-Vibrator and a comparator.

15. The power supply controller circuit of Claim 14 wherein the Monostable Multi-Vibrator receives as an input an output signal from the oscillation circuitry and generates in response thereto a signal representative of a switching frequency of an output of the oscillation circuitry.

16. The power supply controller circuit of Claim 15 wherein the signal is provided to the comparator, along with a switching frequency reference signal such that the comparator generates a switching frequency control signal.

17. The power supply controller circuit of any preceding claim further characterised by the switching frequency controller logic comprising a digital signal processor.

18. The power supply controller circuit of any preceding claim further characterised by the switching frequency controller logic comprising a phase locked loop circuit.

19. The power supply controller circuit of Claim 14, Claim 15 or 16 further characterised by the comparator being arranged to generate a hysteretic and switching frequency control signal.

20. The power supply controller circuit of any preceding claim further characterised by the oscillation circuitry comprising a hysteretic self-oscillating comparator.

21. The power supply controller circuit of any preceding claim further characterised by the compensation circuitry comprising gain compensation circuitry.

22. The power supply controller circuit of any preceding claim further characterised by the compensation circuitry comprising Proportional-Integral-Derivative controller circuitry.

23. The power supply controller circuit of any preceding claim further characterised by the compensation circuitry comprising a comparator.

24. The power supply controller circuit of any preceding claim further characterised by the compensation circuitry comprising phase-shift compensation circuitry.

25. The power supply controller circuit of any preceding claim further characterised by the power converter circuitry comprising a switched mode power converter.

26. The power supply controller circuit of Claim 25 further characterised by the power converter circuitry comprising a buck converter power stage.

27. The power supply controller circuit of any preceding Claim further characterised by the power supply converter circuitry comprising an output LC filter of 2nd or higher order.

28. The power supply controller circuit of Claim 27 further characterised by the output LC filter comprising a low-pass 4th order LC filter.

29. An integrated circuit comprising the power supply controller circuit of any preceding claim.

30. A wireless communication unit comprising the power supply controller circuit of any of preceding Claims 1 to 28.

31. The wireless communication unit of claim 30 wherein the wireless communication unit is arranged to support Terrestrial Trunked Radio (TETRA) Radio communication.

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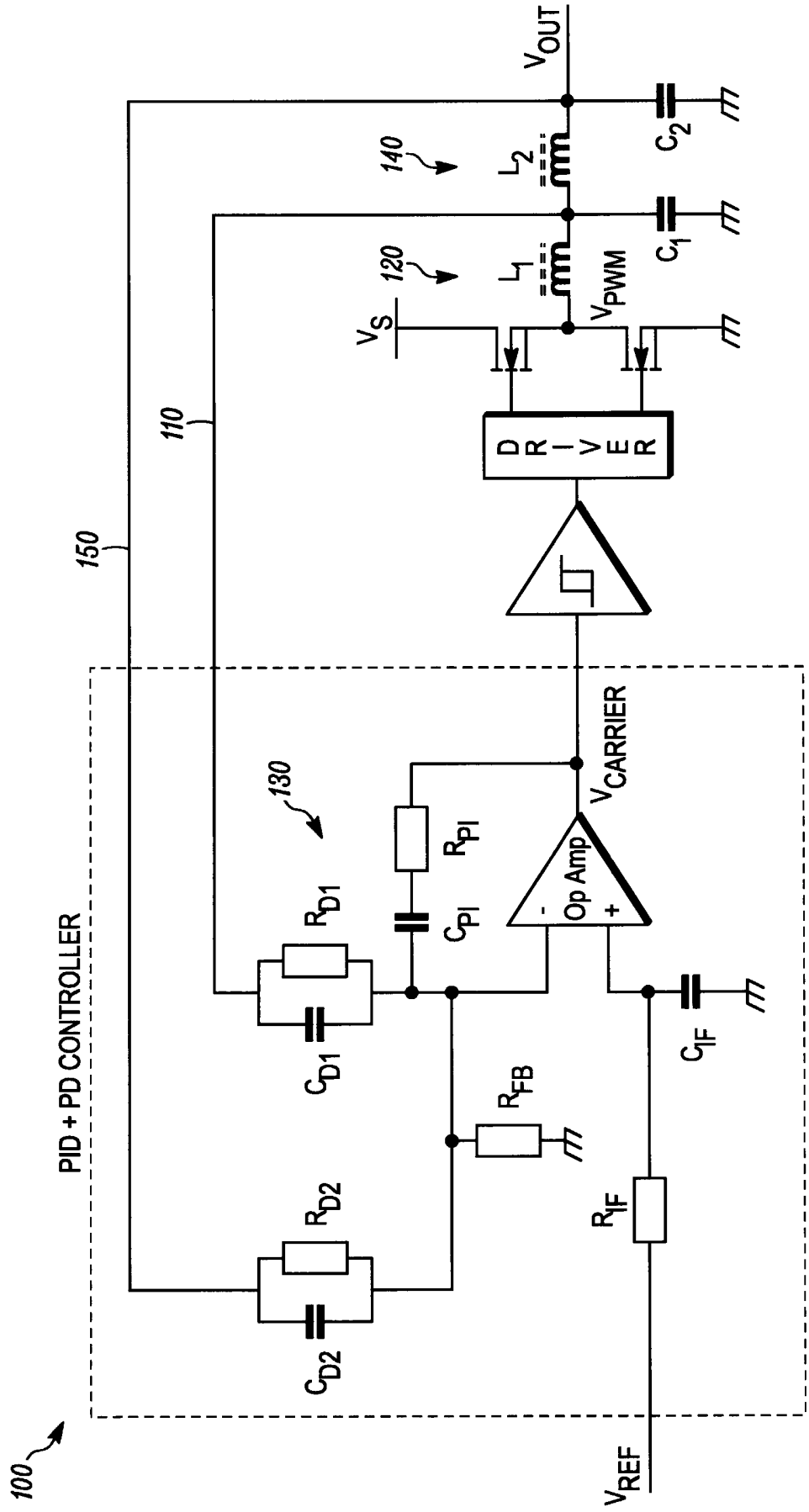

(PRIOR ART)

FIG. 1

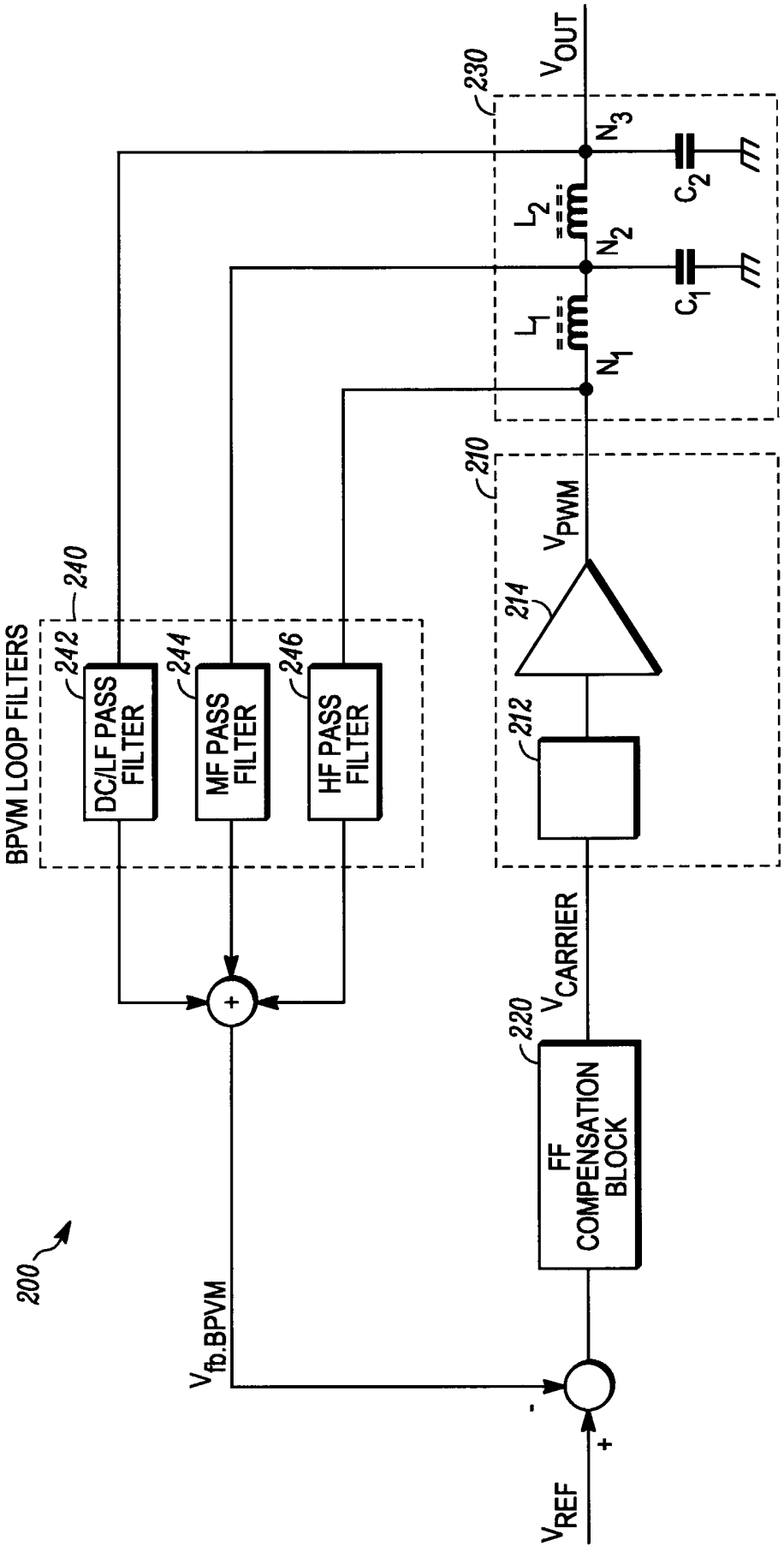
200
BPVM LOOP FILTERS
240
242
DC/LF PASS FILTER
244
MF PASS FILTER
246
HF PASS FILTER
210
214
212
220
FF COMPENSATION BLOCK
230
V_{OUT}
V_{PWM}
$V_{CARRIER}$
$V_{fb.BPVM}$
V_{REF}
N_1
N_2
N_3
L_1
L_2
C_1
C_2
+
-

FIG. 2

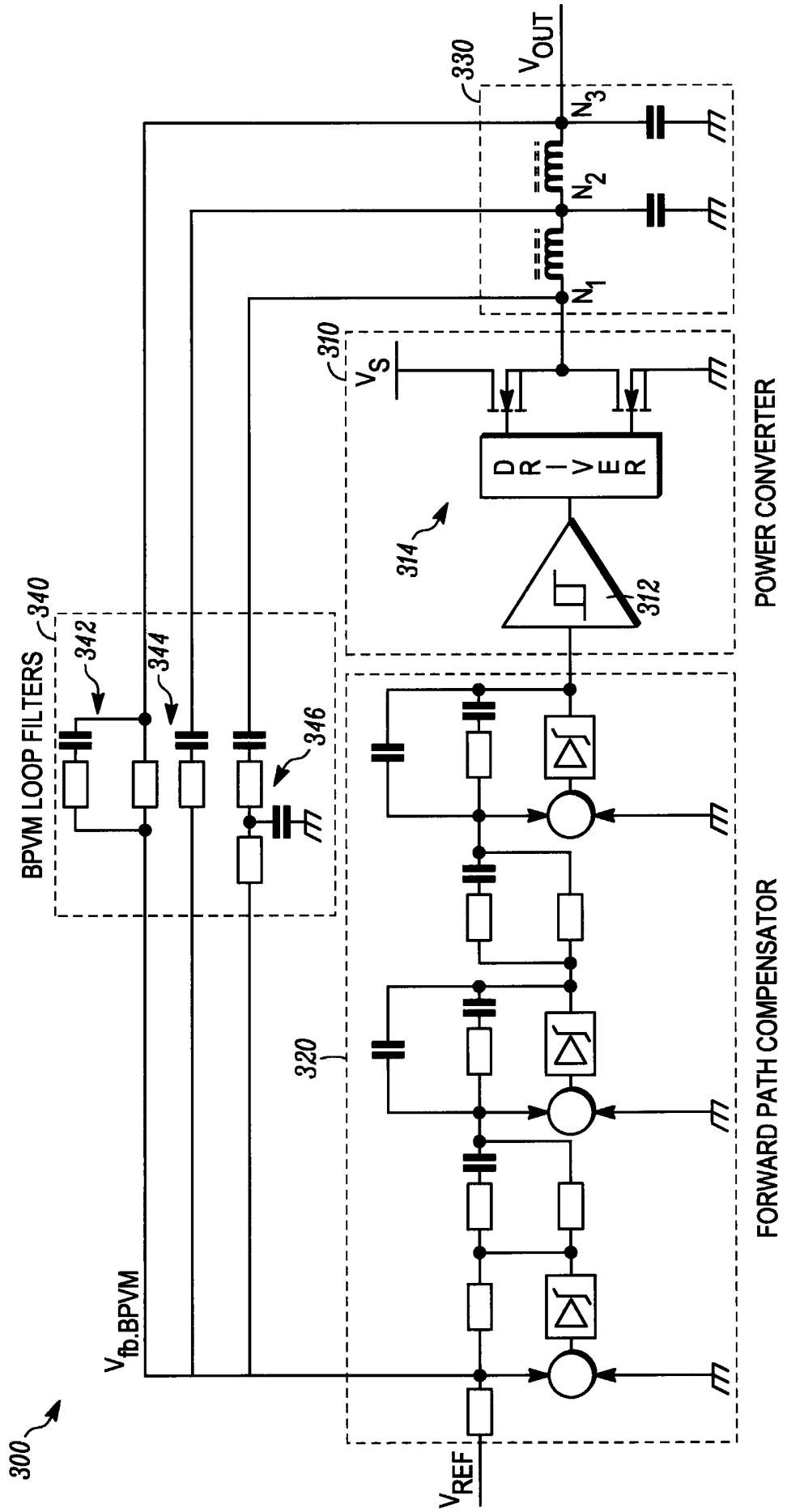
300
$V_{fb.BPVM}$
BPVM LOOP FILTERS
340
342
344
346
320
FORWARD PATH COMPENSATOR
310
V_S
DRIVER
314
312
POWER CONVERTER
330
V_{OUT}
N_3
N_2
N_1
V_{REF}

FIG. 3

APPARATUS FOR POWER SUPPLY CONTROL AND WIRELESS COMMUNICATION UNIT THEREFOR

TECHNICAL FIELD

The technical field relates generally to apparatus for power supply control, and more particularly to apparatus for controlling a switch-mode power supply.

BACKGROUND

In the field of digital radio systems, for example the TErrestrial Trunked Radio (TETRA) system, developed by the European Telecommunications Standards Institute (ETSI), and defined by a plurality of ETSI standards, including the ETS 300-39x technical specification series, and the more recent TETRA-2 system defined in the draft for release 2 of the TETRA specifications., it is desirable to control a power supply to a TETRA transmitter's Power Amplifier (PA) such that the output power level of the PA may be adjusted to correspond more closely to a required instantaneous output power level in order to maximise the PA efficiency.

To this end, it is known to use a switch-mode power supply, such as an Ultra-Fast Tracking Power Supply (UFTPS), for generating a rapidly varying PA supply voltage, whilst not wasting power itself. The requirements for such a UFTPS include:

(i) UFTPS power losses should be low enough to enable an overall system power saving to be achieved, and, as such, must use switch-mode technology.

(ii) The output voltage must respond quickly to reference changes (ideally at a rate equivalent to the transmitted radio frequency (RF) signal bandwidth, for example 25-150kHz according to TETRA 2 preliminary specifications).

(iii) The output ripple voltage, which is a feature of switch-mode power converters, must be low enough to avoid RF pollution when it is inter-modulated with the transmitted RF signal (for example in a range of 5 – 50mVpp).

(iv) Electromagnetic fields emitted from the UFTPS should not interfere with the PA output spectrum.

(v) the output impedance of the UFTPS must be low, in the range from Direct Current (DC) to the RF bandwidth, since the UFTPS is required to maintain a desired output voltage in spite of load current variations (for example, in a region of 10 – 100mΩ for high power systems).

In effect, the UFTPS is required to act as a low-dissipation, controllable voltage source from DC to the desired RF bandwidth.

Existing solutions are based, in one form or another, on a buck (or step-down) switching power converter, and some form of control solution used to control the power converter in order to provide the desired output voltage with minimum delay.

One known control solution comprises a pulse width modulator and a proportional-integral-derivative compensator (PWM/PID) output voltage control solution. A disadvantage with this solution is that a high switching frequency is required, due to a poor ratio (typically around '3-10') between the control bandwidth and the switching frequency for fixed-frequency voltage control. Furthermore, this solution comprises only a moderate output impedance due to moderate bandwidth voltage control, and typically produces a poor low ripple voltage due to a second order output filter.

An alternative known control solution comprises a (peak-) current-mode control solution. This solution suffers from the same disadvantages as the PWM/PID output voltage control solution, with the exception of a higher output impedance, and potentially a 'better' transient response due to the current feedback.

A further alternative known control solution comprises a 'hysteretic' voltage control solution. This is a very fast, low-impedance solution operating at moderate switching frequencies. However, a disadvantage of this solution is that it comprises a high ripple voltage due to its reliance on the Equivalent Series Resistance (ESR) in the output filter capacitor.

Another known control solution comprises a Global Loop Integrating Modulator (GLIM) hysteretic voltage control. This is also a fast, low-impedance control solution, with potential for quite low (although not nearly low enough) ripple voltage. Very low ripple voltages require excessive switching frequencies, which are not easily realisable without using a dedicated control ASIC.

In general, these control solutions share a common problem of too high a ripple voltage. Furthermore, the hysteretic solutions, which are the most attractive solutions in terms of performance, additionally suffer from a variable switching frequency due to their self-oscillating nature.

Three solutions are known for reducing the problem of too high a ripple voltage. These solutions can be summarised as follows:

(i) Use a series or parallel linear power stage to 'clean up' after the switching converter.

(ii) Switch at an extremely high frequency.

(iii) Use an extra LC output filter stage on the switching power converter.

The use of a series or parallel linear power state to clean up after the switching converter has the disadvantage of reducing the efficiency of the UFTPS, and accordingly is an undesirable solution. Switching at an extremely high frequency has the disadvantage of either reducing the efficiency of the UFTPS, or of significantly increased component count (when high frequency is obtained by interleaving multiple buck converters). Consequently, the use of an extra LC output filter is typically considered as the most attractive solution.

However, known solutions that use an extra LC output filter stage on the switching power converter present output impedance and control system design problems. The extra LC section introduces a pole pair, and if this is included in the feedback system, a considerable phase boost has to be provided to maintain closed-loop stability. If the extra LC section is left outside of the control system, then it significantly increases the output impedance of the UFTPS, making it more difficult to maintain the desired voltage across a load of variable nature. FIG. 1 illustrates an example of such a known UFTPS 100 using an extra LC output filter stage.

The UFTPS 100 comprises an inner, self-oscillating control loop 110, coupling the output of a first LC filter stage 120 to a GLIM 130, enabling the inner control loop 110 to be (almost) as fast as is physically possible. This is due to the inner filter cut-off frequency being made fairly high, to allow good control of the second stage, and the very good dynamic properties inherent to the GLIM.

However, the addition of a second LC output filter stage 140 and a second non-self-oscillating control loop 150 increases the output impedance of the UFTPS. This is due to the fact that a self-oscillating control loop has a crossover frequency equal to the switching frequency, in order to provide the fastest possible control solution. However, in order to maintain the fast control solution provided by the self-oscillating control loop, the second control loop cannot be allowed to participate in the oscillation process. Consequently, the frequency response of the second control loop is required to roll off well below this switching frequency, making this a comparatively slow and ineffective control loop. Additionally, the second control loop

has no significant loop gain outside the area of resonance for the second filter stage, making it very ineffective at reducing the contribution of this filter stage to the overall UFTPS output impedance. As a result, the second filter stage tends to dominate the closed-loop output impedance of the power converter.

Thus, there exists a need for a method and apparatus for controlling a power supply, which addresses at least some of the shortcomings of past and present power supply control techniques and mechanisms.

BRIEF DESCRIPTION OF THE FIGURES

The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views, which together with the detailed description below are incorporated in and form part of the specification and serve to further illustrate various embodiments of concepts that include the claimed invention, and to explain various principles and advantages of those embodiments.

FIG. 1 illustrates an example of a known ultra fast tracking power supply.

FIG. 2 illustrates power control circuitry in accordance with an embodiment of the invention.

FIG. 3 illustrates power control circuitry in accordance with an embodiment of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of various embodiments of the invention. In addition, the description and drawings do not necessarily require the order illustrated. Apparatus and method components have been represented where appropriate by conventional symbols in the drawings, showing only those specific details that are pertinent to understanding the various embodiments of the invention so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein. Thus, it will be appreciated that for simplicity and clarity of illustration, common and well-understood elements that are useful or necessary in a commercially feasible embodiment may not be depicted in order to facilitate a less obstructed view of these various embodiments.

DETAILED DESCRIPTION

Generally speaking, pursuant to the various embodiments of the invention, there is provided apparatus for controlling a power supply comprising power converter circuitry, compensation circuitry arranged to provide a compensated control signal to the power converter circuitry, and output filter circuitry operably coupled to an output of the power converter circuitry. The apparatus further comprises frequency selective feedback circuitry for providing feedback from a plurality of nodes within the output filter circuitry to the compensation circuitry.

The provision of frequency selective feedback circuitry enables the implementation of a power control solution in which the problem of too high a ripple voltage may be substantially reduced, whilst maintaining high efficiency and low output impedance, and without a significantly increased component count.

Those skilled in the art will realise that the above recognised advantages and other advantages described herein are merely illustrative and are not meant to be a complete rendering of all of the advantages of the various embodiments.

Referring now to the drawings, and in particular FIG. 2, power supply control circuitry in accordance with some embodiments of the invention is shown and indicated generally at 200. Those skilled in the art, however, will recognise and appreciate that the specifics of this example are merely illustrative of some embodiments of the invention and that the teachings set forth herein are applicable in a variety of alternative settings. For example, since the teachings described do not depend on a particular form of power converter circuitry, they can be applied to any type of power converter circuitry, although power converter circuitry 210 comprising an oscillation element 212 and a buck converter power stage 214 is shown in this embodiment. As such, other alternative implementations of using different types of power converter circuitry are contemplated and are within the scope of the various teachings described.

The power supply control circuitry 200 illustrated in FIG. 2 further comprises compensation circuitry 220 arranged to provide a compensated control signal ($V_{Carrier}$) to the power converter circuitry 210, output filter circuitry 230 operably coupled to an output (V_{PWM}) of the power converter circuitry 210, and frequency selective feedback circuitry 240 for providing feedback from a plurality of nodes within the output filter circuitry 230 to the compensation circuitry 220.

For the illustrated embodiment, the output filter circuitry 230 comprises a first output filter, comprising inductor L_1 and capacitor C_1, and a second output filter, comprising inductor L_2 and capacitor C_2. Accordingly, frequency selective feedback circuitry 240 provides feedback from a first node N_1, located generally at an input of the output filter circuitry 230, a second node N_2, located generally between the two output filters of the output filter circuitry 230, and a third node N_3, located generally at an output of the output filter circuitry 230.

The frequency selective feedback circuitry 240 comprises a plurality of filters, one coupled to each of the nodes within the output filter circuitry 230. Accordingly, for the illustrated embodiment, the frequency selective feedback circuitry 240 comprises three selective filter circuits 242, 244, 246, one coupled to each of the nodes N_1, N_2, N. respectively.

Each selective filter circuit is arranged to substantially filter out received signal components outside of a specific frequency band. For example, for the embodiment illustrated in FIG. 2, the first selective filter circuit 242, coupled to node N_1, is arranged to substantially filter out signal components other then direct current (DC) and low frequency (LF) signal components. The second selective filter circuit 244, coupled to node N_2, is arranged to substantially filter out signal components other than mid-frequency (MF) signal components. The third selective filter circuit 246, coupled to node N_3, is arranged to substantially filter out signal components other than high frequency (HF) signal components.

In this manner, the feedback from each node within the output filter circuitry 230, provided by the frequency selective feedback circuitry 240, substantially only relates to a selected frequency band. In particular, the frequency selective feedback circuitry 240 for the illustrated embodiment filters the feedback from the plurality of nodes within the output filter circuitry 230 such that the majority, if not substantially all, of the DC and LF feedback comes from the output of the filter circuitry 230, node N_3. As a result, substantially only the voltage at the output node, N_3, is fed back at DC/LF, and consequently this will be the only parameter that the compensation circuitry 220 attempts to compensate for. Thus, the loop gain acts substantially directly towards reducing the output impedance of the power supply control circuitry 200. If the inner feedback loops, e.g. those coupled to nodes N_1 and N_2, were to contribute significantly to the DC/LF feedback, the compensation circuitry 220 would

attempt to compensate for the weighted sum of DC/LF feedback, as opposed to only from the output of the filter circuitry 230. This would result in an increase in the output impedance of the power supply control circuitry 200.

At higher frequencies, the inner feedback loops progressively contribute to the feedback as the frequency increases, increasing the output impedance and resulting in the output closed-loop impedance progressively converging towards the open-loop impedance. As will be appreciated by a skilled artisan, open-loop output impedance for a given control loop refers to the output impedance (impedance seen looking into a given node, usually the output node in a power converter of UFTPS) of the controlled system without the loop closed. Closed-loop output impedance correspondingly refers to the output impedance of the controlled system after the control loop in question has been closed.

Accordingly, low output impedance may only be obtained whilst the feedback from the output node N_3 dominates. It is therefore desirable for the output voltage feedback to be made to dominate over the frequency range of interest (which may be given by an radio frequency signal bandwidth of a device comprising the power supply control circuitry) in the UFTPS application. In the band pass voltage mode scheme described herein, this is achieved by placing the transition from the DC/LF feedback of N_3 to the mid-frequency feedback of N_2 above the frequency range of interest.

The, or each, inner feedback loop, which for the illustrated embodiment is/are coupled to nodes N_1 and N_2, provide a means for obtaining part of the considerable phase lead needed to feed back the output of the 4^{th} order filter. Since the hysteresis-based feedback loop generally requires the total phase lag from the output of the power stage 214 (PWM) to the input of the oscillation element 212 to be -90° in a vicinity of the switching frequency, around +270° has to be added by the control circuitry. By bypassing the LC sections (using the inner feedback loops) at frequencies above the frequency range of interest for low output impedance, some of the required phase lead is obtained easily. In particular, feeding back mostly the PWM signal at frequencies close to the switching frequency, -360° of phase lag produced by the 4^{th} order filter is effectively bypassed.

It is envisaged that this principle may be used for alternative order filters, for example 2^{nd}, 4^{th}, 6^{th}, etc. order filters. The 4^{th}-order filter offers a good compromise

between ripple reduction and complexity of the control system. Additionally, each added LC section generally increases the span required between the pass-bands, which is determined by the required and the switching frequency.

In order to make the transition smoothly between frequency bands, for example between DC/LF and HF, the feedback signals should be designed not to be out of phase at the transition between frequency bands, for example resulting from a near 180 degrees phase difference as provided by an LC filter section. This effect is primarily due to complex zero pairs with low damping that result from near-out-phasing during transitions having undesirable effects on the final closed-loop response. In order to obtain phase differences less than 180° during transitions, the feedback loop filters may be designed as follows, for a 4th order output filter:

- Outer filter (DC/LF) provides phase lead to reduce phase difference at a crossover between the outer feedback path and the middle feedback path.
- Middle filter (MF) provides phase lead at a higher frequency to reduce phase difference at a crossover between the middle feedback path and the inner feedback path. DC feedback path is blocked.
- Inner filter (HF) provides phase lag at high frequencies to reduce phase difference with middle feedback path. Additionally, the DC feedback path is blocked.

Accordingly, for the illustrated embodiment, the mid-frequency feedback loop, coupled to node N_2, may be provided to enable a smooth transition between the DC/LF feedback from the output node N_3 and the HF feedback from node N_1.

Furthermore, phase lead is added to aid the transition, since the DC/LC filter circuit 242 comprises a phase lead. In this manner, out-phasing at the transition may be substantially avoided, reducing unwanted oscillatory action to the closed-loop response.

The filtered feedback signals from the nodes within the output filter circuitry 230 are then combined together to generate a feedback signal ($V_{fb,BPVM}$). This feedback signal is then subtracted from a reference signal (V_{ref}), such as a required voltage input signal, to produce an error signal, which is provided to the compensation circuitry 220.

For the illustrated embodiment, the compensation circuitry 220 comprises a feed-forward compensation block providing Proportional and Integral (PI) corrective actions to remove steady-state errors. The feed-forward compensation logic block also provides sufficient phase lead at higher frequencies to allow the system to oscillate properly, in a case of a self oscillating power control solution, or to provide adequate phase margin, in a clocked pulse width modulation (PWM) solution. For example, a total phase lag of around 90 degrees may be required in a vicinity of the switching frequency to ensure correct hysteretic-type oscillation.

As previously mentioned, the compensation circuitry 220 provides a compensated control signal ($V_{Carrier}$) to the power converter circuitry 210. The power converter circuitry 210 receives the compensated control signal as an input, and generates, for example, a PWM output voltage signal (V_{PWM}), based on the received compensated control signal. The PWM output voltage signal is subsequently filtered by the output filter circuitry 230, to provide an output voltage (V_{out}), to be provided to, and to control, for example, an RF power amplifier (not shown).

Referring now to FIG. 3, there is illustrated power supply control circuitry 300 according to an embodiment of the invention. The power supply control circuitry 300 comprises compensation circuitry 320 arranged to provide a compensated control signal to power converter circuitry 310, output filter circuitry 330 operably coupled to an output of the power converter circuitry 310, and frequency selective feedback circuitry 340 for providing feedback from a plurality of nodes N_1, N_2, N_3 within the output filter circuitry 330 to the compensation circuitry 320.

For the embodiment illustrated in FIG. 3, the frequency selective feedback circuitry 340 comprises a plurality of filters, one coupled to each of the nodes within the output filter circuitry 330. Accordingly, for the illustrated embodiment, the frequency selective feedback circuitry 340 comprises three filter circuits 342, 344, 346, one coupled to each of the nodes N_1, N_2, N_3. In the same manner as for the frequency selective feedback circuitry of FIG. 2, each filter circuit of the frequency selective feedback circuitry 340 is arranged to substantially filter out received signal components outside of a specific frequency band. For example, for the embodiment illustrated in FIG. 3, the first filter circuit 342, coupled to node N_1, is arranged to substantially filter out signal components other than direct current (DC) and low frequency (LF) signal components, i.e. it operates as a low pass filter. The second

filter circuit 344, coupled to node N_2, is arranged to substantially filter out signal components other than mid-frequency (MF) signal components, i.e. it operates as a band pass filter. The third filter circuit 346, coupled to node N_3, is arranged to substantially filter out signal components other than high frequency (HF) signal components, i.e. it operates as a high pass filter. For the illustrated embodiment, each filter circuit comprises a simple resistor/capacitor (RC) network of two to four components, where it is assumed that the filters are independent due to a virtual ground provided by the compensation circuitry 320. It is envisaged that in alternative embodiments of the invention, active filter circuits or passive circuits may be used. Furthermore, it is envisaged that any number of R-C networks may be used to implement the filter.

The compensation circuitry 320 for the embodiment of the invention illustrated in FIG. 3 comprises a difference/summation logic block for generating the error between the frequency selective feedback voltage, which for the illustrated embodiment comprises band pass voltage mode (BPVM) feedback voltage, and the reference voltage, followed at least one PI-lead compensator. For the illustrated embodiment, the compensation circuitry comprises two cascaded PI-lead compensators, providing a boost of low-frequency loop gain as well as the remaining high-frequency phase lead not obtained from the BPVM structure.

The output of the compensation circuitry 320 is provided to the power converter circuitry 310, which for the embodiment illustrated in FIG. 3 comprises a schmitt trigger 312 performing a role of a comparator with hysteresis (not shown). In alternative embodiments of the invention, the schmitt trigger 312 may be replaced by a set of high-frequency poles and a comparator, leading to a phase-shift self-oscillating controller, or a PWM implementation using a comparator and an external carrier signal. In effect the schmitt trigger 312 provides a switching signal to a power converter stage 314. The power converter stage 314 may comprise a switched mode power converter, such as a buck converter power stage.

As previously mentioned, the provision of frequency selective feedback circuitry facilitates an implementation of a high-performance power control solution, in particular for 4^{th} (or higher) –order filtered DC/DC converters, in which the problem of too high a ripple voltage may be substantially reduced, for example by way of the output filter comprising a second LC filter, whilst maintaining high

efficiency and low output impedance, and without a significantly increased component count.

For an ordinary buck converter switching at the frequency f_{sw} producing a PWM signal with amplitude $V_{PWM,pp}$, and fitted with a standard 2nd order output filter with cut-off frequency f_{filter}, the output ripple voltage $\Delta V_{out,pp}$ will be approximately:

$$\Delta V_{out,pp} \approx \frac{4}{\pi} \frac{V_{PWM,pp} \cdot f_{filter}^2}{f_{sw}^2} \qquad [1]$$

For a PWM amplitude of 40V, a filter cut-off frequency of 50kHz and a 1MHz switching frequency, the output ripple voltage will be 127mVpp.

With a 4th-order filter with cut-offs f_{p1} and f_{p2}, the ripple will similarly be given by:

$$\Delta V_{out,pp} \approx \frac{4}{\pi} \frac{V_{PWM,pp} \cdot f_{p1}^2 \cdot f_{p2}^2}{f_{sw}^4} \qquad [2]$$

For a reasonable choice of cut-off frequencies at 50kHz and 375kHz, the ripple voltage is only 18mVpp for the same 1MHz switching frequency, clearly illustrating ripple reducing benefits of the 4th order filter.

In the foregoing specification, specific embodiments have been described. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present teachings. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as critical, required, or essential features or elements of any or all the claims. The invention is defined solely by the appended claims.

CLAIMS

1. Apparatus for controlling a power supply comprising power converter circuitry, compensation circuitry arranged to provide a compensated control signal to the power converter circuitry, and output filter circuitry operably coupled to an output of the power converter circuitry; wherein the apparatus further comprises frequency selective feedback circuitry including a plurality of filter circuits for providing to the compensation circuitry feedback from each of a plurality of nodes within the output filter circuitry, in such a way that in operation low frequency feedback is derived from an output node of the output filter circuitry and higher frequency feedback is derived from another node of the output filter circuitry.

2. The apparatus of claim 1 wherein the selective feedback circuitry is such that in operation feedback which is successively higher in frequency than the low frequency feedback is derived from nodes of the output filter circuit which are successively further from the output node and nearer the input node of the output filter circuitry.

3. The apparatus of Claim 1 or Claim 2 further characterised in that each of the plurality of filter circuits is arranged to filter out received signal components outside of a specific frequency band.

4. The apparatus of Claim 3 further characterised by the frequency selective feedback circuitry comprising three filter circuits: a first filter circuit being arranged to filter out signal components other than direct current and low frequency signal components; a second filter circuit being arranged to filter out signal components other than mid-frequency signal components; and a third filter circuit being arranged to substantially filter out signal components other than high frequency signal components.

5. The apparatus of Claim 4 further characterised by the first filter circuit being arranged to provide direct current and low frequency feedback, the second filter circuit being arranged to provide mid-frequency feedback and the third filter circuit arranged to provide high frequency feedback.

6. The apparatus of Claim 5 further characterised by the transition from the direct current and low frequency feedback and the mid-frequency feedback being above a frequency range.

7. The apparatus of Claim 6 further characterised by the frequency range being a radio frequency signal bandwidth of a device comprising the apparatus.

8. The apparatus of Claim 6 or Claim 7 further characterised by the first filter circuit providing a phase lead to reduce phase difference at a crossover between the first filter circuit feedback and second filter circuit feedback.

9. The apparatus of Claim 6 or Claim 7 or Claim 8 further characterised by the second filter circuit providing a phase lead at a higher frequency than that of the first filter circuit to reduce a phase difference at a crossover between the second filter circuit feedback and third filter circuit feedback.

10. The apparatus of any of preceding Claims 6 to 9 further characterised by the third filter circuit providing phase lag at high frequencies to reduce phase difference with second filter circuit feedback.

11. The apparatus of any of preceding Claims 4 to 10 further characterised by the first filter circuit being coupled to a node within the output filter circuitry located generally at an output of the output filter circuitry.

12. The apparatus of Claim 11 further characterised in that the third filter circuit, is coupled to a node within the output filter circuitry located generally at an input of the output filter circuitry.

13. The apparatus of any of preceding Claims 3 to 12 further characterised in that each filter circuit of the frequency selective feedback circuitry comprises a passive resistor/capacitor (RC) network.

14. The apparatus of any preceding Claim further characterised by the output filter circuitry comprising a first output filter and a second output filter, and the frequency selective feedback circuitry provides feedback from a first node, located generally at an input of the output filter circuitry, a second node, located generally between the two output filters of the output filter circuitry, and a third node, located generally at an output of the output filter circuitry.

15. The apparatus of Claim 14 further characterised by each output filter of the output filter circuitry comprising an inductor-capacitor arrangement.

16. The apparatus of any preceding Claim further characterised by filtered feedback signals from the nodes within the output filter circuitry being combined together to generate a feedback signal.

17. The apparatus of Claim 16 further characterised by the feedback signal being subtracted from a reference signal to produce an error signal, which is provided to the compensation circuitry.

18. The apparatus of any preceding Claim further characterised in that the compensation circuitry comprises a feed-forward compensation circuit providing proportional and integral corrective actions.

19. The apparatus of Claim 18 further characterised by the compensation circuitry comprising a difference/summation logic block for generating an error between the frequency selective feedback voltage and a reference voltage.

20. The apparatus of Claim 19 further characterised by the compensation circuitry further comprising at least one Proportional and Integral (PI)–lead compensator.

21. The apparatus of Claim 20 further characterised by the compensation circuitry comprising two PI-lead compensators.

22. The apparatus of any preceding Claim further characterised by a power converter stage comprising a switched-mode power converter.

23. The apparatus of Claim 22 further characterised by the power converter stage comprising a buck converter power stage.

24. A wireless communication unit comprising an apparatus according to any of the preceding Claims.

25. The wireless communication unit of Claim 24 wherein the wireless communication unit is arranged to support TETRA-2 communication.

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